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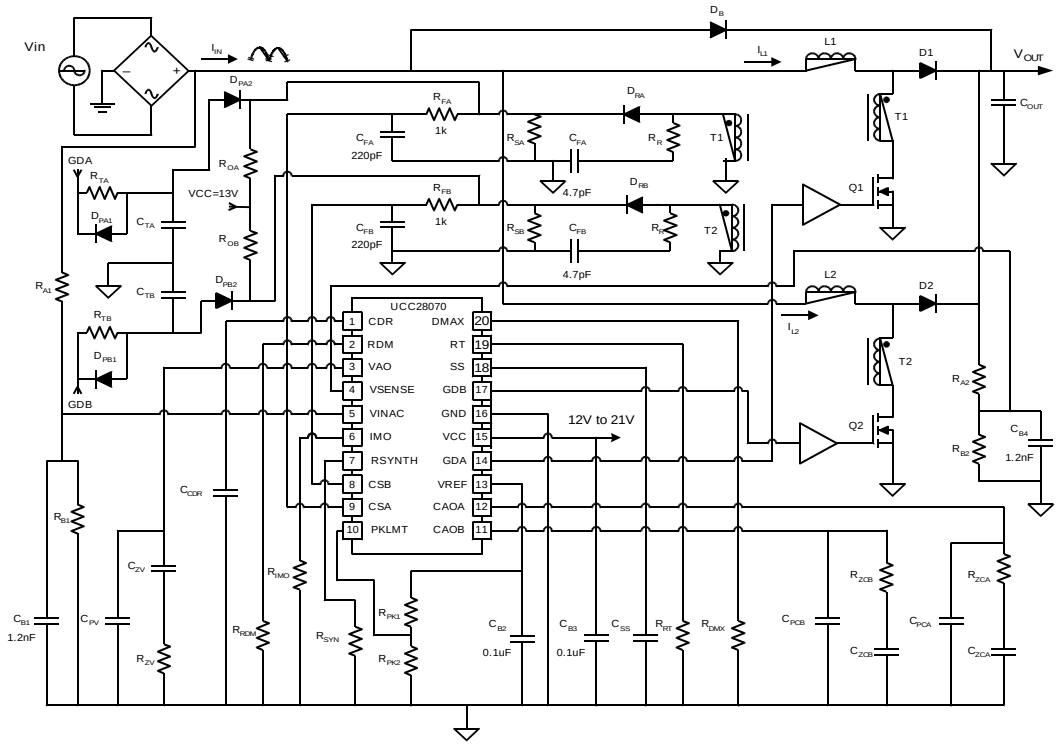
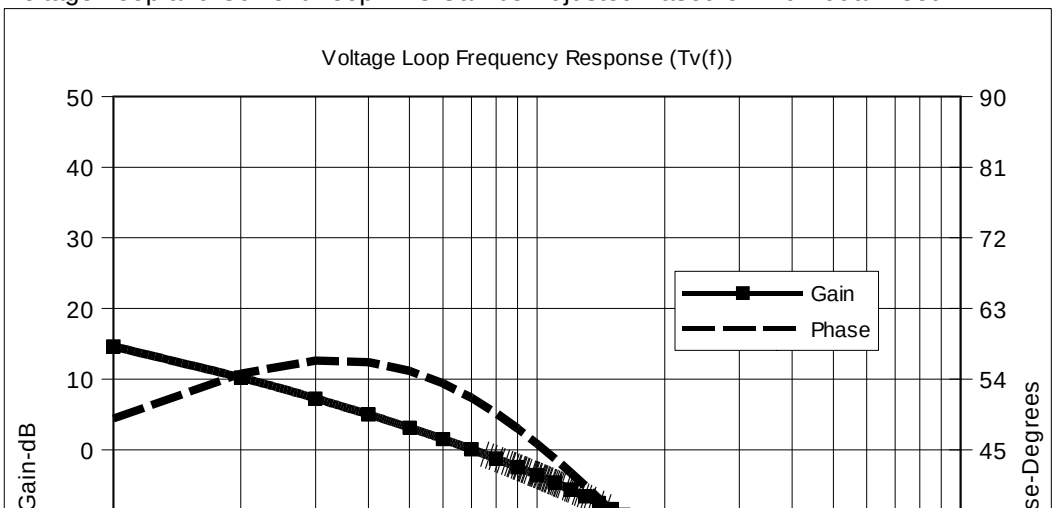
|---|---|---|---|
| **UCC28070 Controller Setup Tool** | 15/08/2008 | | |
| **Preliminary** | | | |
| **Notes:** | | | |
| **This design tool is designed to work with the UCC28070 Application Note SLUA479** | | | |
| **This design tool is optimized for a Universal Input and can be used for designs were the input voltage is anywhere between 85V to 265V RMS.** | | | |
| **Please enter design parameters into the** | **shaded** | **cells;** | |
| **Calculated results will be in GRAY** | | | |
| **Design Parameters:** | **Variable Names** | | Units |
| Minimum RMS Input Voltage | $V_{IN\_MIN}$ | 85 | V |
| Maximum RMS Input Voltage | $V_{IN\_MAX}$ | 265 | V |
| Minimum Line Frequency | $f_{LINE}$ | 47 | Hz |
| Maximum Line Frequency | | 63 | Hz |
| Maximum Output Power | $P_{OUT}$ | 1900 | W |
| Full Load Efficiency (Must be less than 0.99) | $\eta$ | 0,90 | |
| Switching Frequency | $f_S$ | 4,00E+04 | Hz |
| Output Voltage | $V_{OUT}$ | 390 | V |
| Maximum Duty Cycle | $D_{MAX}$ | 0,97 | |
| Soft Start Time | $t_{SS}$ | 0,50 | s |
| Optional Frequency Dither Magnitude (Total $\Delta$fs) | $f_{DM}$ | 0,00E+00 | Hz |
| Optional Frequency Dither Rate | $f_{DR}$ | 0,00E+00 | Hz |
| VCC | VCC | 12 | V |
| **Component Selection, Trip Points and Calculated Values from the UCC28070 Design Example** | | | |
| Duty Cycle at the Peak the Peak of Low Line Input | $D_{PLL}$ | 0,69 | |
| Inductor Ripple Current Cancellation at the Peak of Low Line | $K(D_{PLL})$ | 0,55 | |
| Inductor Ripple Current | $\Delta I_{L1}$ | 19,01 | |
| Calculated Boost Inductors $L_{1\_MIN}$, $L_{2\_MIN}$ | $L_{1\_MIN,}$ $L_{2\_MIN}$ | 1,09E-04 | H |
| Enter the Lowest Inductance Value of the Real Inductor | $L_{1\_MIN,}$ $L_{2\_MIN}$ | 1,00E-04 | H |
| Enter the Highest Inductance Value of the Real Inductor | $L_{1\_MAX,}$ $L_{2\_MAX}$ | 3,50E-04 | H |
| Average Inductance Value | $L_{1\_AVG,}$ $L_{2\_AVG}$ | 2,25E-04 | H |
| Inductor RMS Current | $I_{L1\_RMS,}$ $I_{L2\_RMS}$ | 13,223 | A |
| Output Capacitance Calculated Based on Holdup Time | $C_{OUT}$ | 1,22E-03 | F |
| Output Capacitance Selected | $C_{OUT}$ | 1,41E-03 | F |
| Output Ripple Voltage | $V_{RIPPLE}$ | 13,0 | V |
| Low Frequency Output Capacitor RMS Current | $I_{COUT\_LF}$ | 3,828 | A |
| High Frequency Output Capacitor RMS Current | $I_{COUT\_HF}$ | 6,505 | A |
| Peak Diode and FET Current | $I_{PEAK}$ | 32,478 | A |
| FET RMS Current (Q1 and Q2) | $I_{DS}$ | 10,671 | A |
| Diode Average Current (D1 and D2) | $I_D$ | 2,436 | A |
| Calculated Current Sense Transformer Turns Ratio | $N_{CT}=N_S/N_P$ | 325 | |

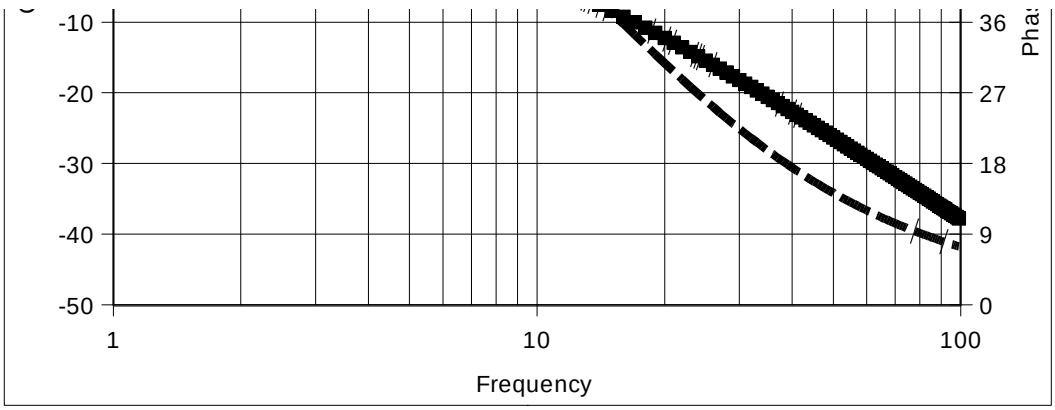
| | | | |
|---|---|---|---|
| Enter Current Sense Transformer Turns Ratio | $N_{CT}=N_S/N_P$ | 100 | |
| Minimum Magnetizing Inductance of the Current Sense Transforme | $L_M$ | 9,85E-03 | H |
| Select Current Sense Peak Voltage | $V_S$ | 3,70 | V |
| Calculated Current Sense Resistor | $R_{SA} = R_{SB}$ | 10,3 | ohm |
| Select Standard Current Sense Resistor | $R_{SA} = R_{SB}$ | 10 | ohm |
| CalculatedReset Resistor | $R_R$ | 3,E+02 | ohm |
| Select a Standard Value | $R_R$ | 3,30E+02 | ohm |
| Calculated Maximum DR Reverse Voltage | $V_R$ | 107 | V |
| Current Sense Offset Desired | $V_{OFF}$ | 0,20 | V |
| Program Offset Bias Current to be added to $R_S$ | $R_{OA}=R_{OB}$ | 5,90E+02 | ohm |
| Select a Standard Value | $R_{OA}=R_{OB}$ | 5,90E+02 | ohm |
| Program Current Sense PWM Ramp Resistor | $R_{TA}=R_{TB}$ | 7,31E+02 | ohm |
| Select Standard Values | $R_{TA}=R_{TB}$ | 7,30E+02 | ohm |
| Program Current Sense PWM Ramp Timing Capacitor | $C_{TA}=C_{TB}$ | 8,33E-07 | F |
| Select Standard Values | $C_{TA}=C_{TB}$ | 1,00E-06 | F |
| Select High Side Resistor on Peak Current Limit Divider | $R_{PK1}$ | 3,65E+03 | ohm |
| Calculated Low Side Resistor on Peak Current Limit Divider | $R_{PK2}$ | 5,87E+03 | ohm |
| Select Low Side Resistor on Peak Current Limit Divider | $R_{PK2}$ | 5,87E+03 | ohm |
| Calculated Timing Resistor | $R_{RT}$ | 1,88E+05 | ohm |
| Select Timing Resistor | $R_{RT}$ | 2,00E+05 | ohm |
| Calculated Programmable Duty Cycle Limit Resistor | $R_{DMX}$ | 1,88E+05 | ohm |
| Select Programmable Duty Cycle Limit Resistor | $R_{DMX}$ | 1,86E+05 | ohm |
| Select High Side Resistor for VSENSE Voltage Divider | $R_A$ | 3,20E+06 | ohm |
| Calculated Low Side Resistor on VSENSE voltage Divider | $R_B$ | 2,48E+04 | ohm |
| Select Low Side Resistor on VSENSE voltage Divider | $R_B$ | 2,49E+04 | ohm |
| Calculated Nominal Over Voltage Trip Point | $V_{OVP}$ | 412 | V |
| Voltage Divider Gain | H | 7,72E-03 | |
| Voltage Amplifier Output Impedance at double $f_{LINE}$ | $Z_O$ | 1,37E+04 | ohm |
| Calculated Pole Capacitance for the Voltage Loop | $C_{PV}$ | 1,24E-07 | F |
| Select a Standard Value | $C_{PV}$ | 1,22E-07 | F |
| Calculated Voltage Loop Crossover Frequency | $f_{VC}$ | 11,6 | Hz |
| Calculated Voltage Loop Zero Compensation Resistor | $R_{ZV}$ | 1,13E+05 | ohm |
| Select a Standard Value | $R_{ZV}$ | 1,00E+05 | ohm |
| Calculated Voltage Loop Zero Compensation Capacitor | $C_{ZV}$ | 1,37E-06 | F |
| Select a Standard Value | $C_{ZV}$ | 1,22E-06 | F |
| Calculated Current Synthesis Programmable Resistor | $R_{SYN}$ | 2,70E+05 | ohm |
| Select a Standard Value | $R_{SYN}$ | 2,83E+05 | ohm |
| Voltage Calculation for Selecting Multiplier Resistor | $V_1$ | 69,601 | V |
| Voltage Calculation for Selecting Multiplier Resistor | $V_2$ | 2,359 | V |
| Multiplier Resistor | $R_{IMO}$ | 1,81E+04 | ohm |
| Select a Standard Value | $R_{IMO}$ | 1,82E+04 | ohm |

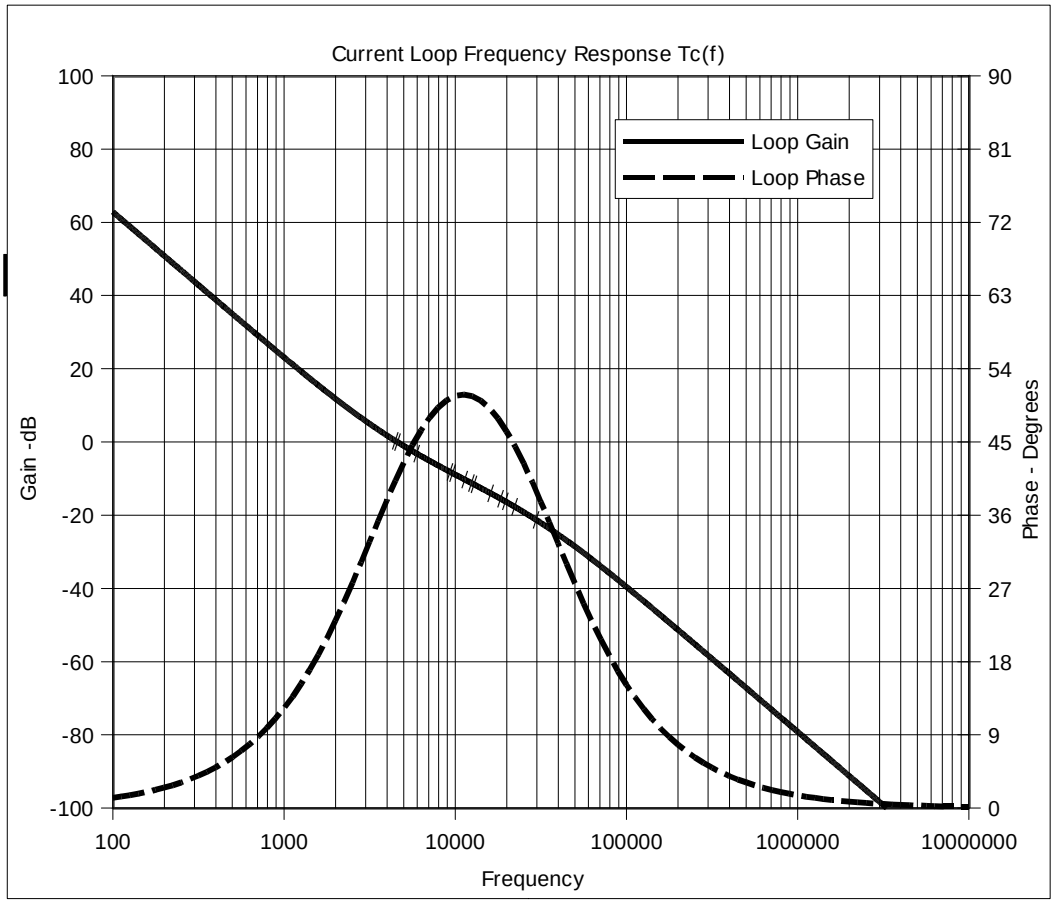
| | | | |
|---|---|---|---|
| Current Loop Power Stage Gain at Loop Crossover | $G_{PSC}$ | 1,724 | |
| Current Loop Zero Resistor | $R_{ZC1}=R_{ZC2}$ | 5,80E+03 | ohm |
| Select a Standard Value | $R_{ZC1}=R_{ZC2}$ | 5,80E+03 | ohm |
| Current Loop Zero Capacitor | $C_{ZC1}=C_{ZC2}$ | 6,86E-09 | F |
| Select a Standard Value | $C_{ZC1}=C_{ZC2}$ | 6,90E-09 | F |
| Current Loop Pole Capacitor | $C_{PC1}=C_{PC2}$ | 1,37E-09 | F |
| Select a Standard Value | $C_{PC1}=C_{PC2}$ | 1,00E-09 | F |
| Calculated Soft Start Capacitor (Be sure $C_{SS}$ > or = $C_{ZV}$) | $C_{SS}$ | 2,2222222E-006 | F |
| Select a Standard Value (Be sure $C_{SS}$ > or = $C_{ZV}$) | $C_{SS}$ | 2,20E-06 | F |
| Program Dither Magnitude Resistor | $R_{RDM}$ | #DIV/0! | ohm |
| Select a Standard Value | $R_{RDM}$ | 0,00E+00 | ohm |
| Program Dither Rate Capacitor | $C_{CDR}$ | #DIV/0! | F |
| Select a Standard Value | $C_{CDR}$ | 0,00E+00 | F |
| Disclaimer | | | |




Voltage Loop and Current Loop Axis Can be Adjusted Based on Individual Need




-10
-20
-30
-40
-50
36
27
18
9
0
1
10
100
Frequency


Current Loop Frequency Response Tc(f)
Loop Gain
Loop Phase
Gain -dB
Phase - Degrees
100
80
60
40
20
0
-20
-40
-60
-80
-100
90
81
72
63
54
45
36
27
18
9
0
100
1000
10000
100000
1000000
10000000
Frequency