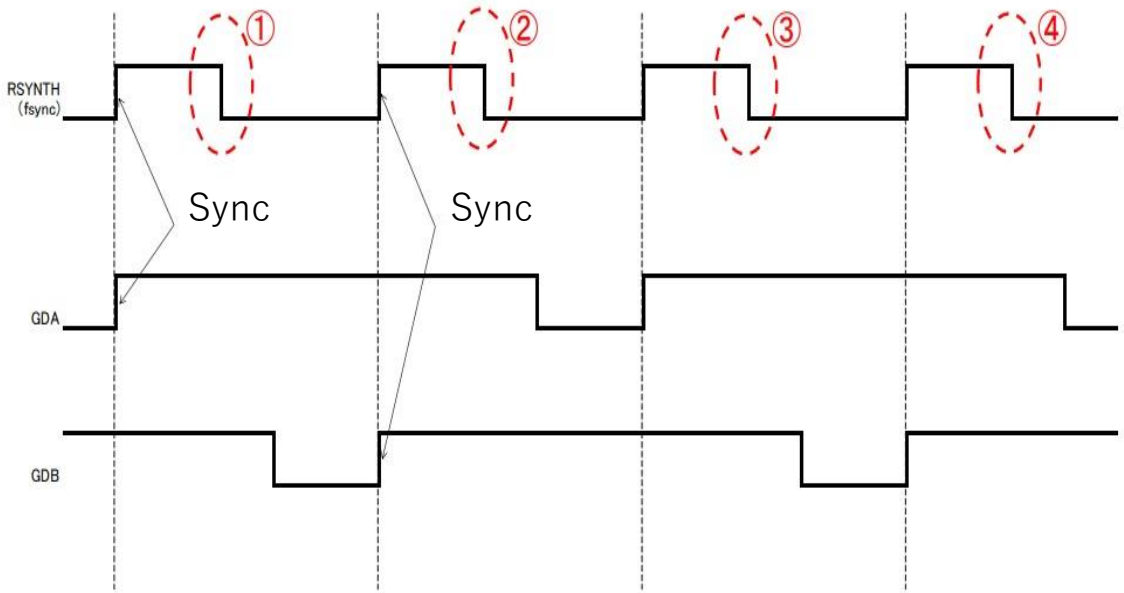

Question

UCC 28070 data sheet The following statement in section 7.3.4
It must also be noted that the maximum duty-cycle clamp programmability is affected during external synchronization. The internal timing circuitry responsible for setting the maximum duty cycle is initiated on the falling edge of the synchronization pulse. Therefore, the selection of RDMX becomes dependent on the synchronization pulse width (tSYNC).

How does the falling edge relate to the maximum duty?
What kind of operation does the IC do?

Look at the waveform on the left.
It is a waveform diagram of external pulse and GDA, GDB.
Please explain the timing at which GDA and GDB determine the maximum duty for the 1 to 4 falling edges.