Application Report SLUA424A

PFC Pre-Regulator Frequency Dithering Circuit

4 Internal PWM Timing

Figure 3 shows a functional block diagram of the internal circuitry that generates the oscillator signal of the PWM controller in Figure 1. The timing is set up by an R and C and a comparator. RT sets the charging current in the timing capacitor (CT) through the current mirror formed by Q1 and Q2. An internal comparator with hysteresis will control when CT will charge and discharge forming the PWM timing. To dither the switching frequency of the PWM, circuitry will be added to the converter to modulate CT's charging current.

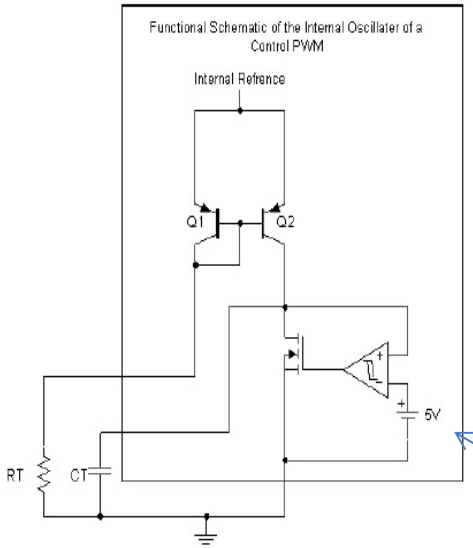

Figure 3. PWM Oscillator Timing Circuitry

the CT pin threshold.

The CT threshold is 1V.（answer)

OSCILLATOR SECTION					
Initial accuracy	T_A = 25°C	85	100	115	kHz
Voltage stability	VCC = 10.8 to 15 V	–1%		1%	
Total variation	Line, temp	80		120	kHz
Ramp peak voltage		4.5	5	5.5	V
Ramp amplitude voltage (peak to peak)		3.5	4	4.5	V

Q1

Can I think that the variation of CTpin is this value?

Q2

How is this 5V variation?　　±2%?