UCC2818D FUNCTIONING ISSUE

We are currently using the UCC2818D in order to implement the PF correction block in the system.
The circuit is fed with a three-phase line without Neutral reference.
The PFC block of the circuit is dimensioned in order to obtain a 350Vdc output; to obtain this, an active six-switch boost-type PFC rectifier has been implemented.
Input phases have range 158VAC L-L up to 230VAC L-L, frequency from 400Hz to 800Hz.

The target is PF ≥ 0.98.

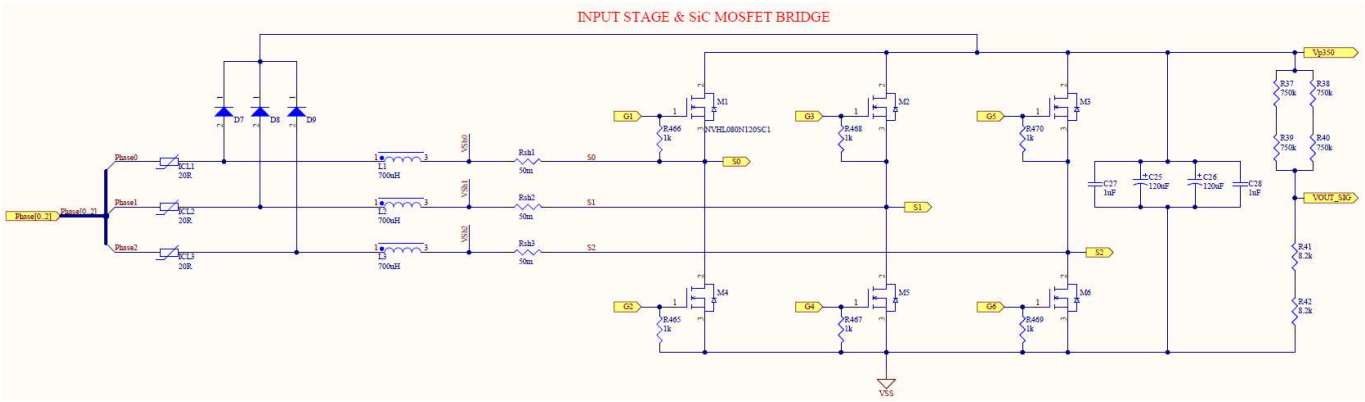

Figure 1

For each couple of MOS (M1-M4, M2-M5, M3-M6) is provided a dedicated feedback line that provides each gate signal (G1, G2, G3, G4, G5, G6).
At this point of the tests, we have identified critical issues in the compensation networks inbound to the three IC.
Before to proceed, we are currently enabling only Mosfets M1 and M4 (so, only one phase is "working").
The network components around the UCC2818D are highlighted in the following figure:

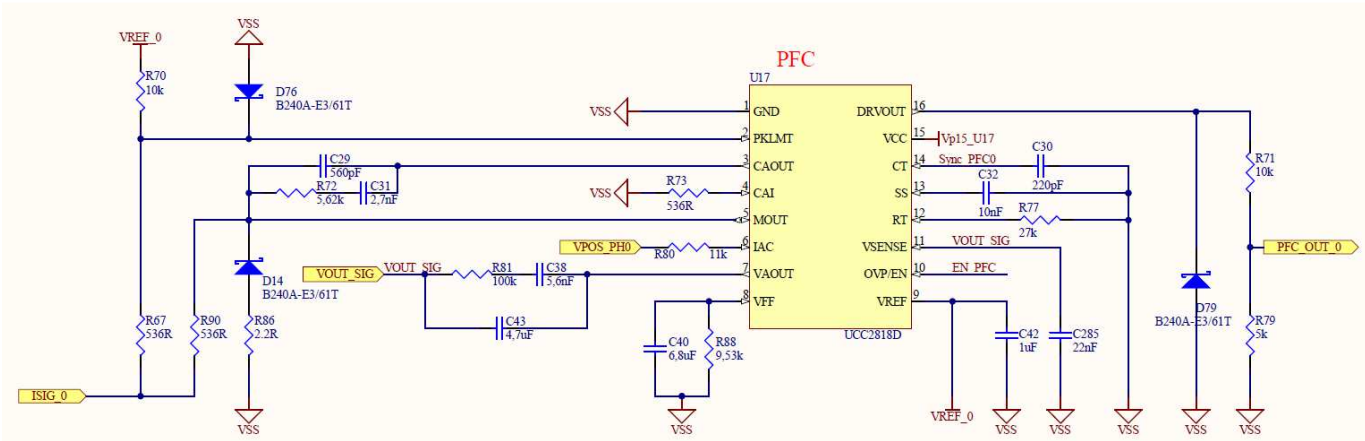

Figure 2

Where signal **ISIG_0** is the current feedback (obtained by means of a shunt resistor, placed in series with the input inductor L1 and then treated throw an operational amplifiers chain to obtain an equivalent negative signal. This implies that, if the input current sinusoid portion is negative, then

ISIG_0 will remain negative; instead if the current sinusoid is positive, an equivalent one is created but with a 180 degrees rotation). **VPOS_PH0** is the rectified input phase (referred to VSS).
VOUT_SIG is the scaled output voltage and when Vp350 (Vout) reaches 350Vdc, VOUT_SIG should be 7.5V.
The following figures have been obtained after an attempt to adjust the compensation net on pin 7 of UCC2818D (the voltage feedback compensation). In particular, C43 = 2.8nF, C38 = 1.5nF, R81 = 300k and C40 = 470nF:

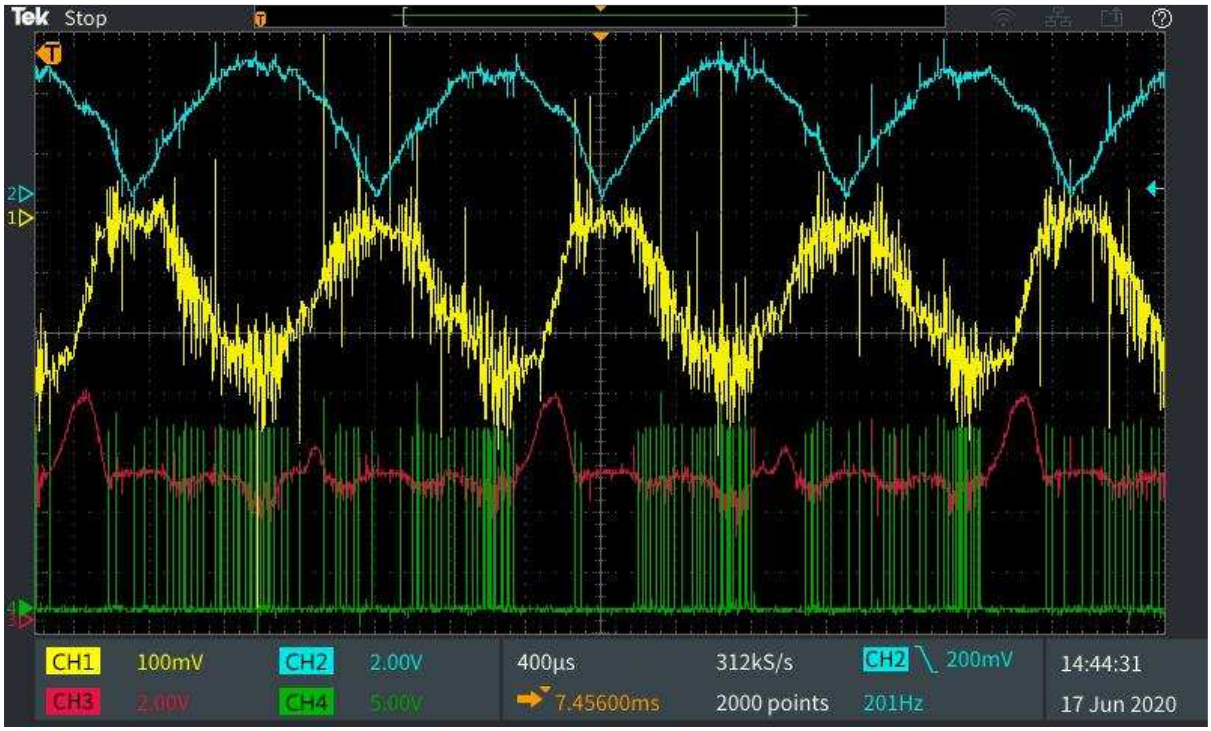

Figure 3

Where the blue signal is **VPOS_PH0**, yellow signal is **ISIG_0**, green signal is pin 16 of UCC2818D and purple one is CAOUT (pin 3 of UCC2818D). The following figure is a zoomed version of *Figure 3*:

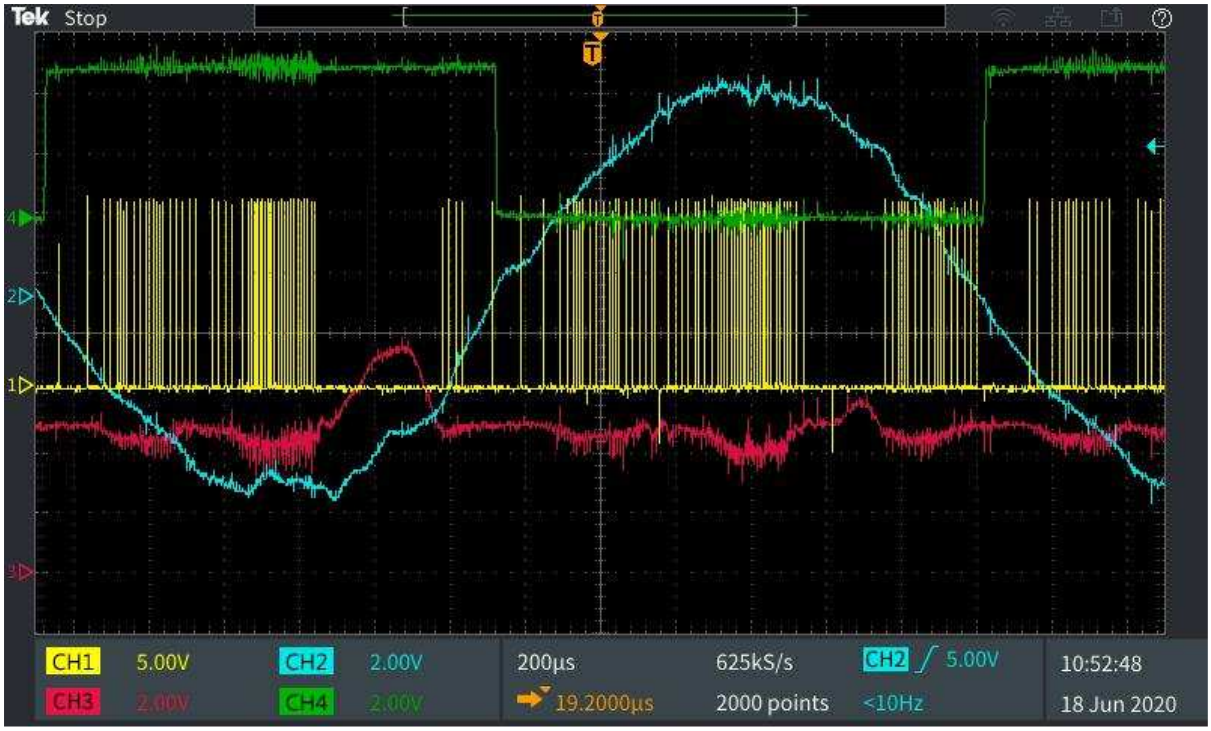

Figure 4

where green waveform is VSIDE_0, a “digitalized version” of the input phase (low level correspond to the positive part of the sinusoid, while the high one correspond to the negative portion), yellow waveform is pin 16 of UCC2818D, purple waveform one is CAOUT (pin 3 of UCC2818D) and the blue one is the input sinusoid referred to VSS.

In these conditions, the output voltage Vp350 does not reach 350Vdc, but it starts to about 265V and then goes to about 275V. The output of the UCC2818D (pin 16) seems not to “pumping”, because the duty cycle is very tight. The only correspondence we have noticed is the CAOUT behaviour: it seems to have a CAOUT absolute peak when a ISIG_0 negative absolute peak is verified.
In this condition, input Phase0 and current have the following behaviour (input phase current = yellow line, input phase voltage = blue line):

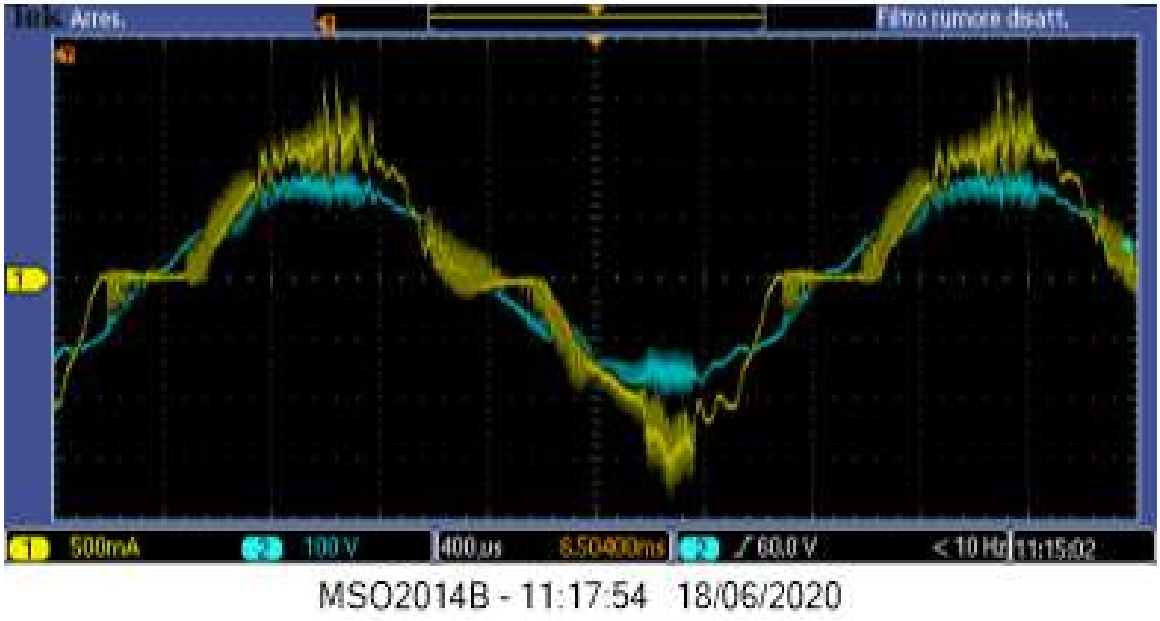

Figure 5

Next step was to try to modify the compensation net between pins 3 and 5 (the current feedback compensation). In particular, we chose R73 = R90 = 2.4k, R72 = 24k, C29 = 120pF, C31 = 680pF. In this condition, pin 16 of UCC2818D seems not to work. It completely turns off M1 and M4:

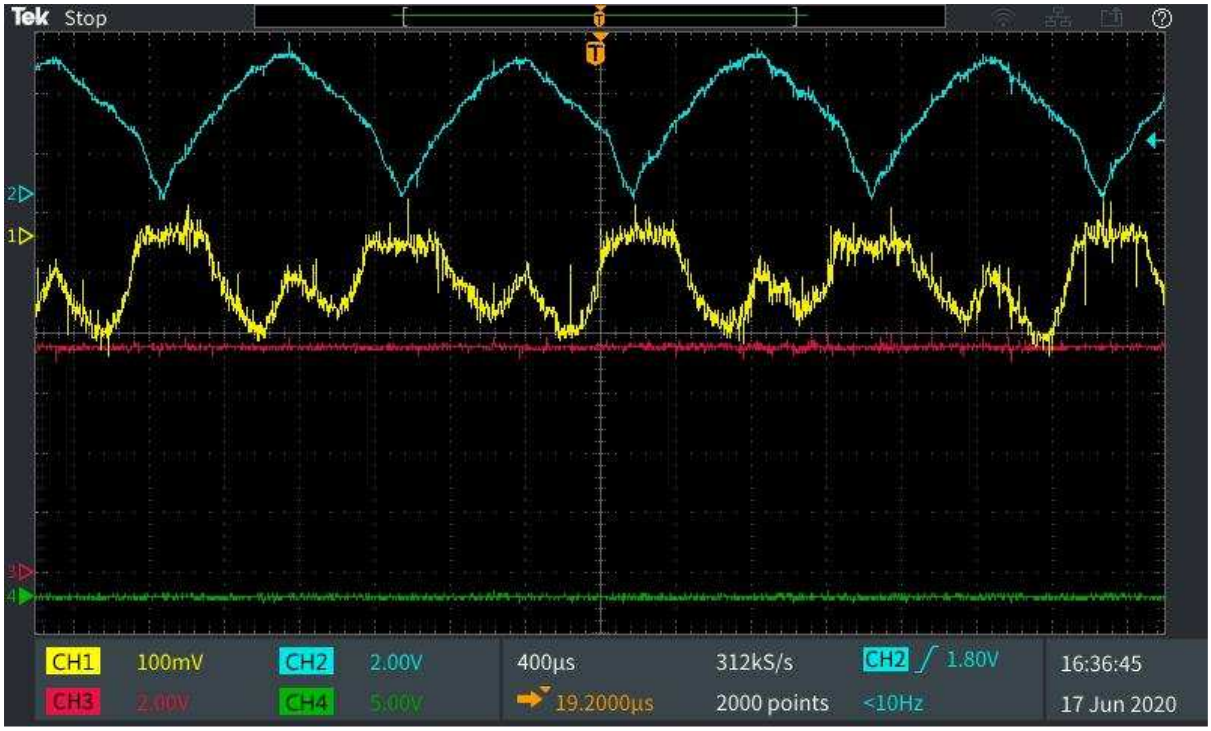

Figure 6

where the blue signal is **VPOS_PH0**, yellow signal is **ISIG_0**, green signal is pin 16 of UCC2818D and purple one is CAOUT (pin 3 of UCC2818D).

The correspondent input Phase0 voltage and current are:

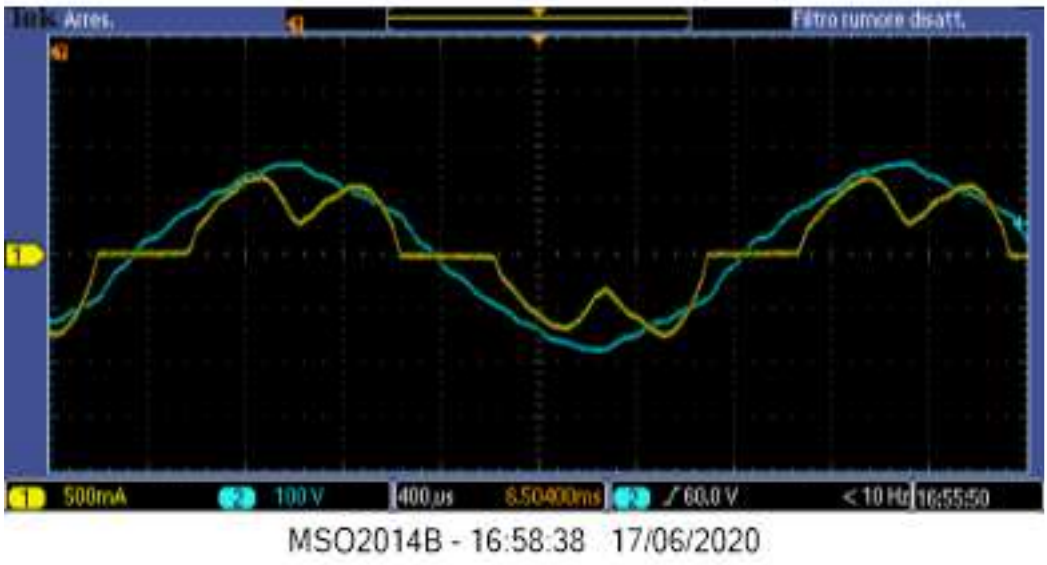

Figure 7

What do you think about the results shown here?

Could you provide us any feedback to perform a correct compensation nets dimensioning in order to obtain a correct behaviour of UCC2818D?