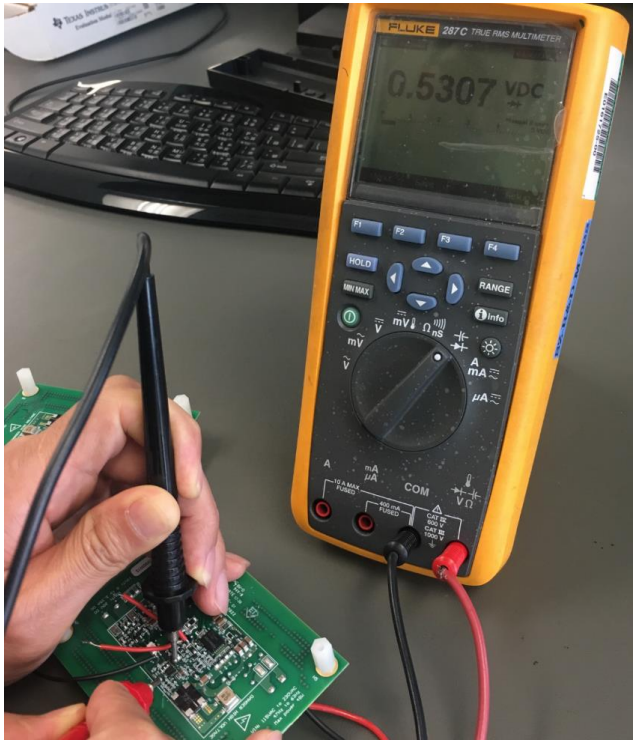
UCC28780 Debug Guide and Common Issues

Contents

- How to power up your board
- How to distinguish the protection
- Common issues and solutions
- Optimize your design

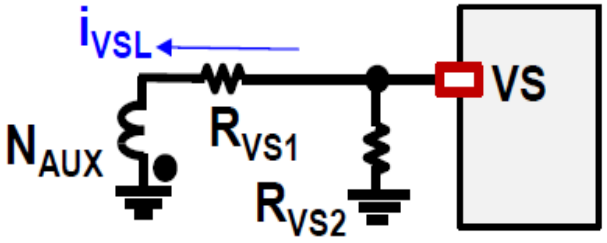
Before Power on : Check soldering



Specially for QFN package

- Use multi-meter “Diode” setting.
- “Red” probe → GND, “Black” probe → each Pin of IC.
- Presents a 0.5~0.7V voltage = normal.
- If not , Check soldering of pin.

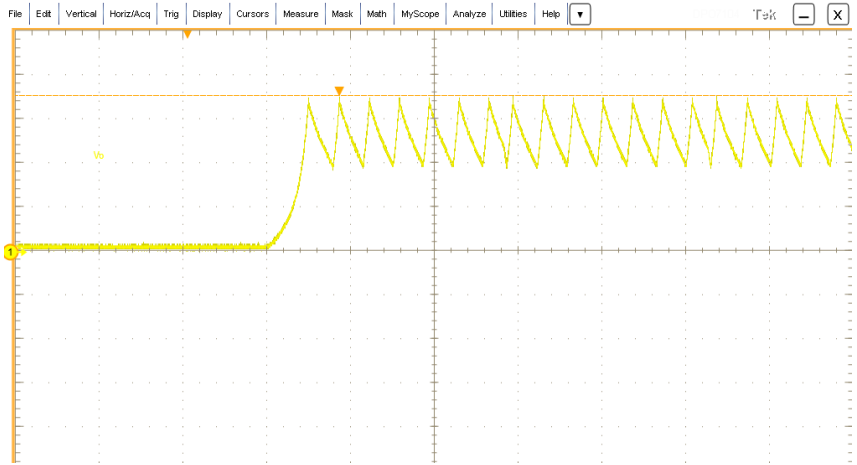
Before Power on : Setting Brown-in voltage



- $I_{VSL(Brown\text{-}in)}$ is start-up threshold current at VS pin
- N_{AUX} and N_P are the turns of AUX and Pri. windings
- $V_{bulk(Brown\text{-}in)}$ is DC voltage on bulk at start-up
- 75Vac /106Vdc is preferred start point of Brown-in
- Large different from preferred will affect OPP curve
- Calculate R_{VS1} , then program it

$$i_{VSL(Brown-in)} = 353\mu A \approx \frac{(N_{AUX} / N_P)V_{bulk(Brown-in)}}{R_{VS1}}$$

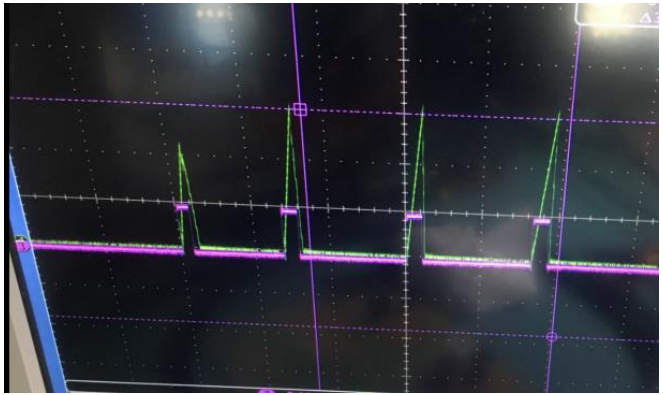
Low AC_IN Power on : Check VDD HV start



CH1 (Yellow) : VDD

- AC input voltage = 20Vac or little more
- Capture the VDD voltage
- VDD presents a Triangle wave
- The peak ~ 17.5V , valley ~9.8V , HV start normal

Low AC_IN Power on : Check low-side pulse



- Gradually increase AC input to a little lower than Brown-in
- Zoom in to low side driver pulse
- CH3 Purple : Low-side driver ,CH4 Green : VDD
- 4 pulses is normal
- CH3 Purple : Low-side driver
- CH4 Green : XFMR Ipri.

If above steps are normal, you can power up your board to next step

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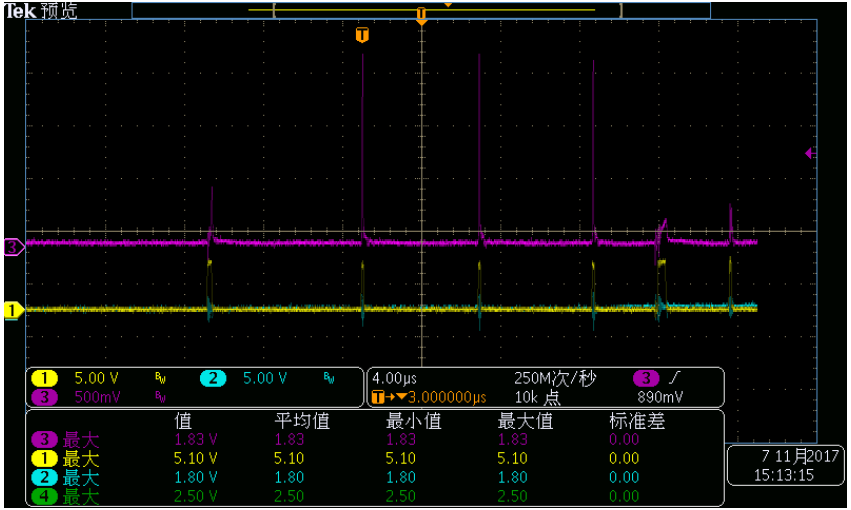
Protection Features of UCC28780

Protection	Sensing	Threshold	Delay to Action	Action
VDD UVLO	V_{DD}	$V_{DD(on)}$=17.5V $V_{DD(off)}$=10.5V	no	V_{DD} restart
Over Power protection (OPP)	CS	$V_{CST} \geq V_{CST(OPP)}$	1 160ms	1.44s restart
Peak current limit (PCL)	CS	$V_{CST(max)}$=0.8V	160ms	1.44s restart
Over current protection (OCP)	CS	$V_{CST} \geq 1.2V$	3 PWML pulses	1.44s restart
Short circuit protection (SCP)	CS, VS, VDD	(1) $V_{DD}=V_{DD(off)}$ & $V_{CS} \geq V_{CS(OPP)}$ (2) $V_{DD}=V_{DD(off)}$ & VS≤0.6V	≤160ms	2 1.44s restart
Over voltage protection (OVP)	VS	VS≥4.6V	3 PWML pulses	1.44s restart
Brown-in detection	VS	I_{VSL}<353μA	3 PWML pulses	V_{DD} restart
Brown-out detection	VS	I_{VSL}<320μA	60ms	V_{DD} restart
Over temp. protection (OTP)	NTC	$R_{NTC} \leq 10k\Omega$	3 PWML pulses	V_{DD} restart until $R_{NTC} \geq 22.5k\Omega$
Thermal shutdown	Die	T_{die}>125°C	3 PWML pulses	V_{DD} restart

Note : Specially check “Delay to Action” and “Action” in your waveform
To identify which protection occur

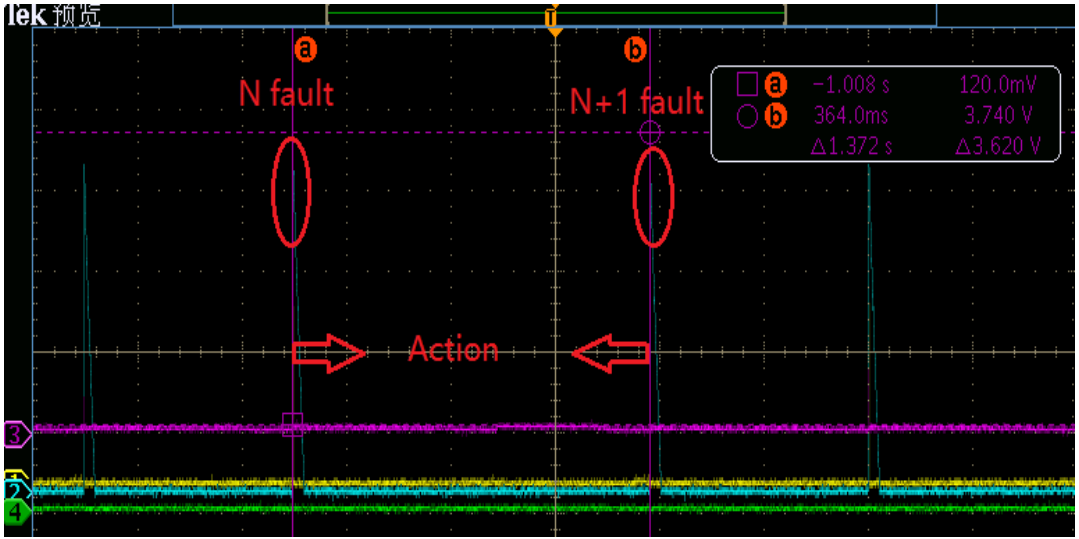
How to identify “Delay to Action”

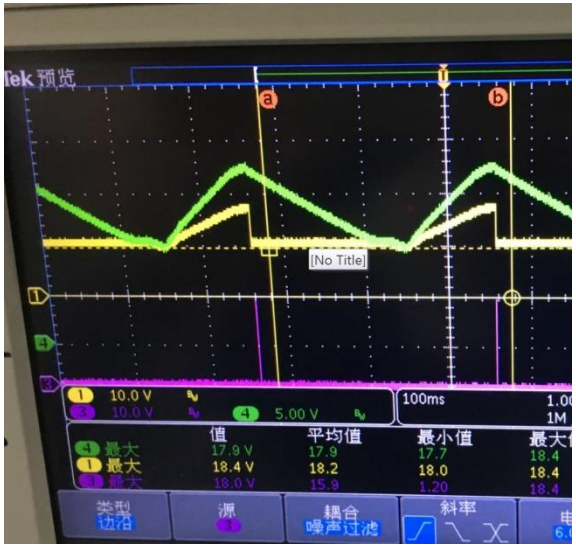


CH3 (purple): Vcs
CH1 (Yellow): PWML

Ex: 3 pulse trigger OCP 1.2V “Delay to Action”

How to identify “Action”





The interval time of adjacent fault is “Action”
Ex: 1.44s restart of OVP , CH2: Vout

CH4 Green VDD hiccup
Ex: VDD restart

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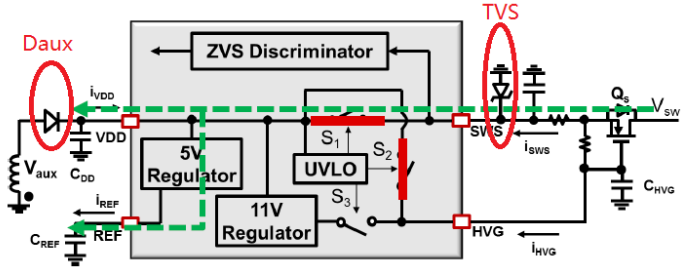
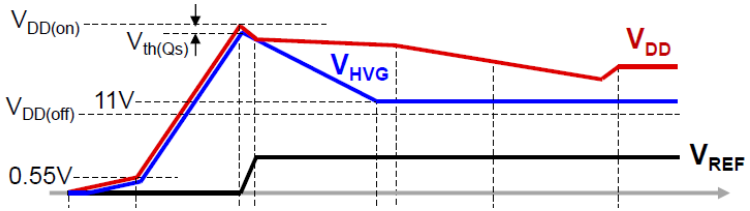
VDD UVLO: VDD is clamped too low to start

- **HV Startup Mode**
  - S1 and S2 on, S3 off,
  - S1 limits the charge current tens or hundreds uA



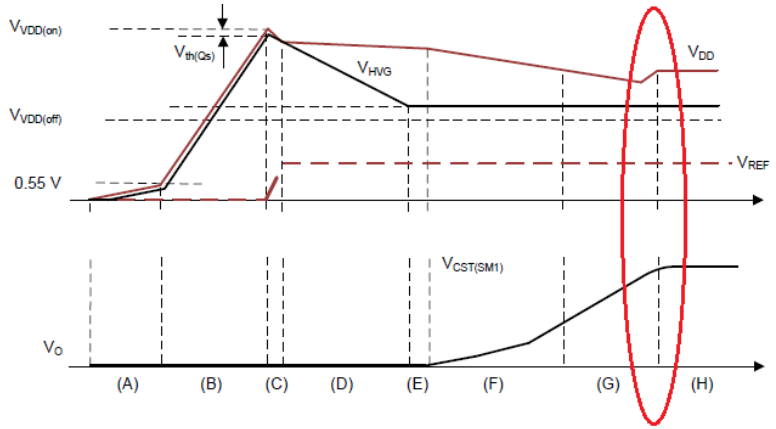
- **Normal VDD start up waveform**
  - VDD(on) =17.5V,
  - V_{REF}=5V,



- **Common issues**
  - VDD clamped to such as 9V,----Potential reason is AUX winding rectify diode reverse current exceed S1 charge current tens or hundreds uA . Solution: Replace Daux and check reverse current.
  - VDD be clamped to such as15V, ----Potential reason is the TVS on SWS pin used low voltage TVS, Solution: suggest use 18V~20V TVS.

VDD UVLO: AUX didn't take over VDD supply

- **VDD drop to UVLO**
  - After Vo settle, the auxiliary winding should take Over VDD supply. →
  - If not ,VDD will drop to UVLO.

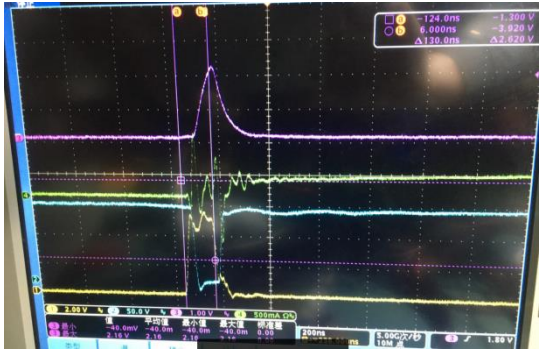


- **Common issues**
  - Improper XFMR Turn ratio of Ns and Naux, Specially in PD design – Large Vo range
    ex: Ns:Naux =4:3, When Vo=20V, VDD=15V –ok, while Vo=9V, VDD=6.75V, UVLO.
  - If there are LDO or two AUX windings for VDD , check if normally operation .

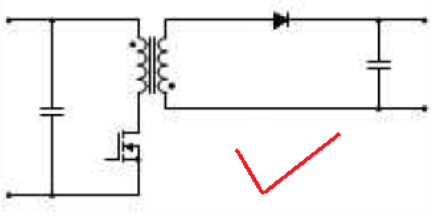
OCP: XFMR wrong polarity

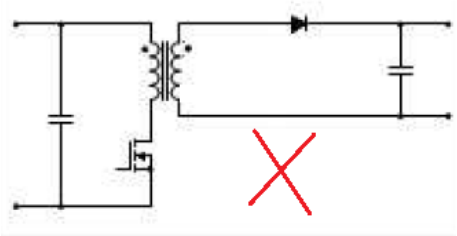
- **Identify if it's OCP**
  - "Delay to Action" -- 3 PWML pulses
  - "Action" –1.44s restart.
  - Zoom in one pulse , peak value > 1.2V

- **Common issue**
  - Wrong polarity of XFMR winding,
  - Wrong assembly or XFMR design,



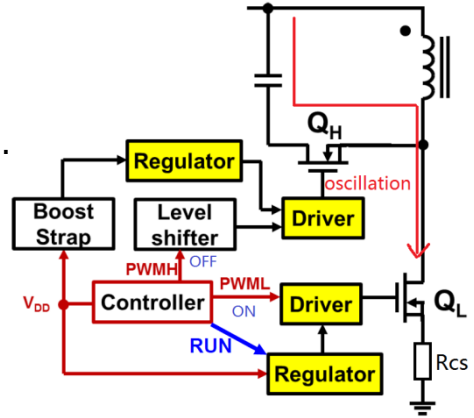
Purple : Vcs, Yellow : PWML

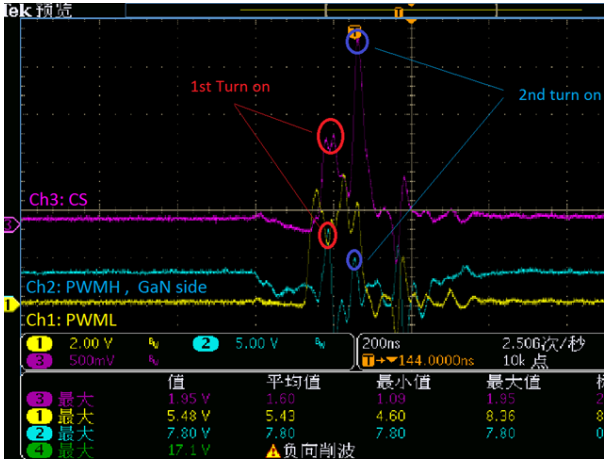




OCP: Shoot through of High&Low side FETs

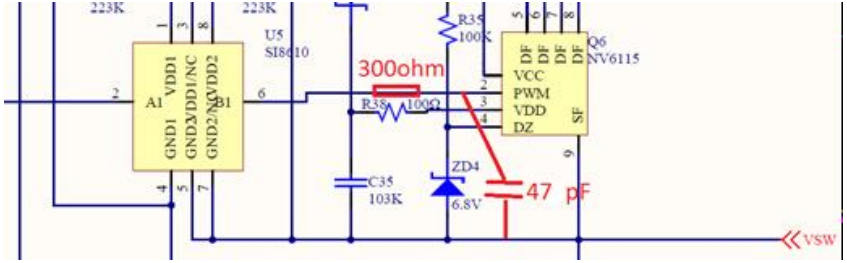
- **Shoot through at Burst mode**
  - PWML on, PWMH off --UCC28780 .
  - Oscillation found at isolator driver side.
  - The oscillation voltage trigger high Side GaN turn on





- **Possible reason and solution**
  - Large switching noise at burst mode,
  - Bad PCB layout ---large high side driver loop,

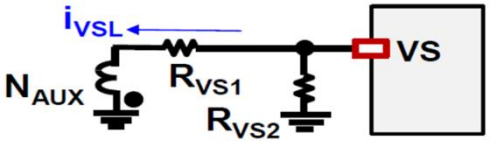
Solution: Add RC filter to suppress the oscillation



OVP: Bad loop compensation and setting

➢ **Identify if it's OVP**

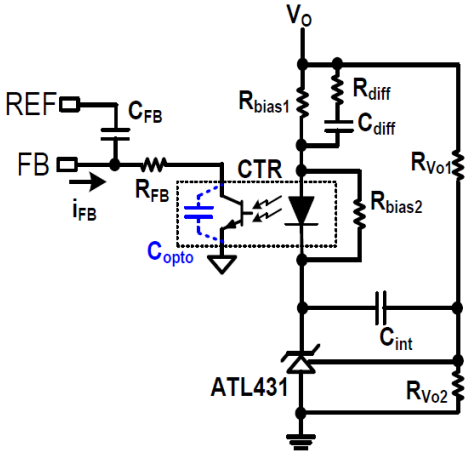
- "Delay to Action" -- 3 PWML pulses
- "Action" –1.44s restart.
- Capture Vout, Check if > Setting value



$$V_{VS(OVP)} = 4.5V \approx \frac{(N_{AUX} / N_S) V_{o(OVP)} \cdot R_{VS2}}{R_{VS1} + R_{VS2}}$$

➢ **Possible reasons and solution**

- Wrong setting V_{OVP}, --Correct it
- 431 not working, --Rbias2 limits required Min. I_{KA} Decrease Rbias2
- Too large $R_{FB.}$ – suggest 20K ~ 39K.
- Too small CTR of opto-coupler. – Use better
- Other components failure lead to open-loop.



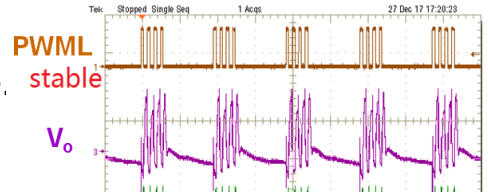
Other protection: Open and Short of Pins

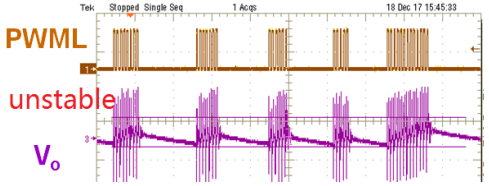
PROTECTION	SENSING	CONDITION	DELAY TO ACTION	ACTION
CS pin short	PWML on-time @ first PWML pulse only	> 2 µs (SET = 5 V)	none	UVLO reset
		> 2 µs (SET = 0 V, R_{RDM} ≥ 55 kΩ)		
		> 1 µs (SET = 0V, R_{RDM} < 55 kΩ)		
CS pin open	CS voltage	V_{CS} > 1.2 V	3 PWML pulses	t_{FDR} restart (1.5 s)
HVG pin open	HVG voltage @ $UVLO_{ON}$	V_{HVG} < or =12 V in less than 10 µs after V_{VDD} reaches $V_{VDD(on)}$	none	UVLO reset
HVG pin high	HVG voltage	V_{HVG} > 14 V	none	UVLO reset
RDM pin short	RDM current @ $UVLO_{ON}$	V_{RDM} = 0 V, self-limited i_{RDM}	none	UVLO reset
RDM pin open	RDM current @ $UVLO_{ON}$	RDM = Open	none	UVLO reset
RTZ pin short	RDM current @ $UVLO_{ON}$	V_{RTZ} = 0 V, self-limited i_{RTZ}	none	UVLO reset
RTZ pin open	RDM current @ $UVLO_{ON}$	RTZ = Open	none	UVLO reset

If find only 1 pulse of PWML or no pulse , the possible reason is one critical Pin was open or short

Burst mode unstable (Passive compensation)

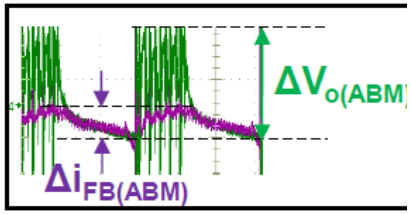
- **What is “unstable” ?**
  - In SBP,LPM,ABM mode , The count of pulse In a packet is from 2 to 9 as the load increase.
  - Inconsistent pulse will lead to large ripple And audible noise

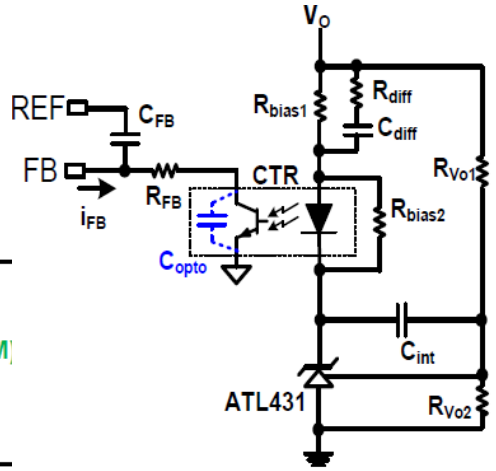




- **Solution**
  - Make i_{FB} in phase with Vo “burst” ripple
  - Proposed debug start point of parameters as shown in right table

Specially add Rdiff and Cdiff



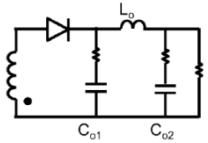


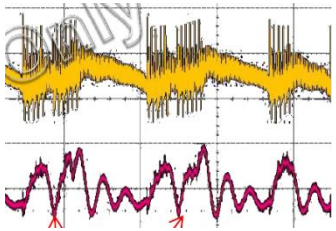
Location	Proposed
Rbias1	11K
Rdiff	**510ohm**
Cdiff	**4.7nF**
R_{FB}	22.1K
C_{FB}	100pF
Cint	10nF

Burst mode unstable (Active Ripple Compen.)

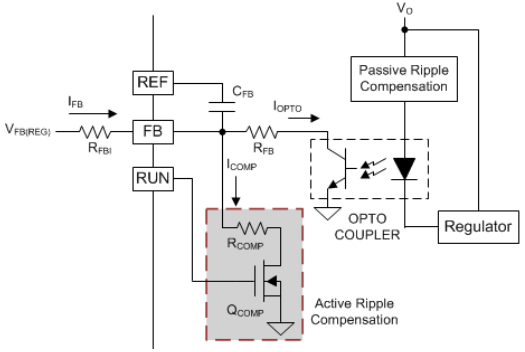
- **What application should use ARC ?**
  - When Output capacitor C_{o1} is polymer, and No Lo and C_{o2}
  - With CLC filter on output -- 2nd–order filter (Secondary Resonance C_{o1}(ceramic)<<C_{o2})

Lower ESR

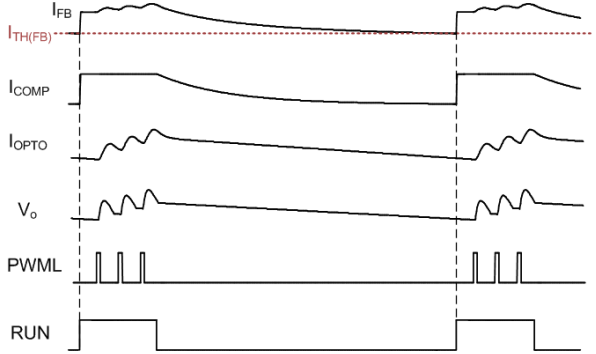




- **Solution :**
  - Active ripple compensation (R_{COMP} can be decreased but not less than 510K)



Q_{COMP}: 2N7002; R_{COMP}=1~2MΩ



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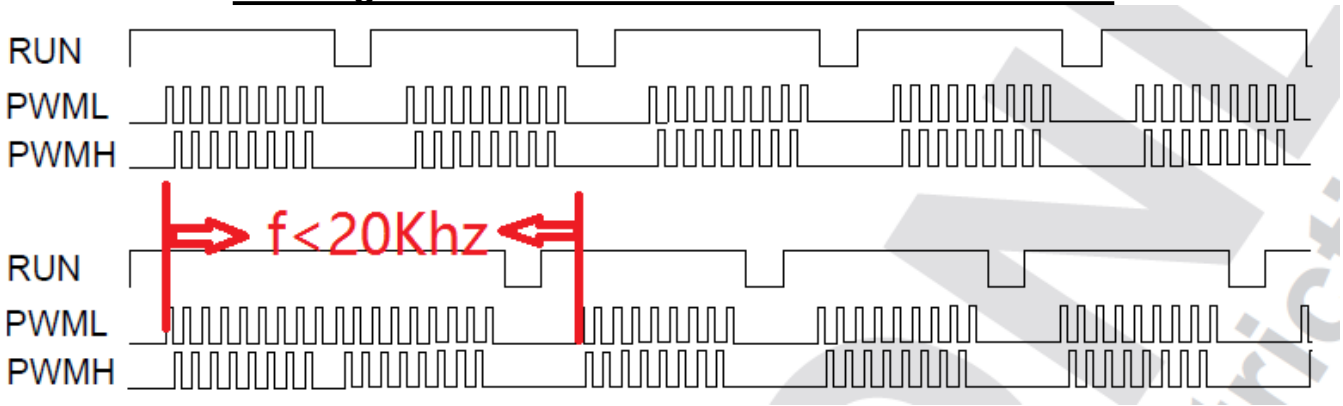
Audible noise reduction: ABM ➡AAM

Nsw higher than 9 for a smoother mode transition

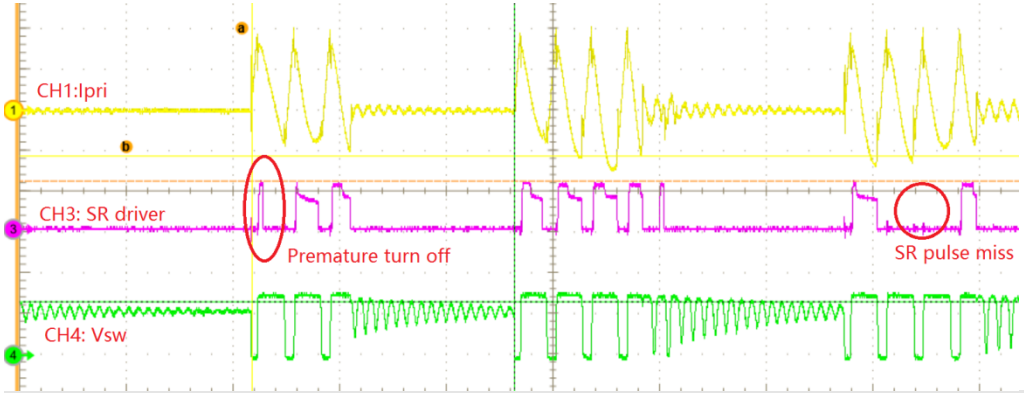


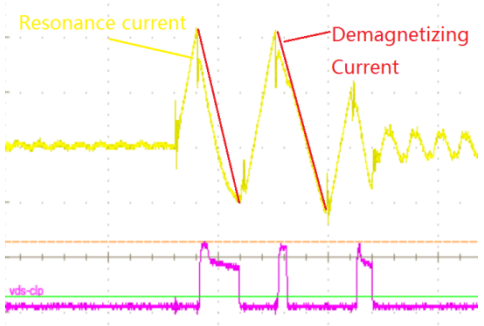
Solutions for white noise reduction:

- **Transformer dip varnishing**
- **Lower peak magnetizing current – Minor decrease V_{BUR}**
- **Other source of noise – MLCC capacitors of Cclamp or Sec._Reson. Caps**
  *** More quantity caps parallel to reduce noise**
- **Adjust ABM loop more stability– narrow i_{FB} range (enlarge Rbias1 page 18)**

SR driver missing pulse in burst

Reason: The resonance current touch demagnetizing current lead to SR current natural to zero





Solutions :

- **Higher peak magnetizing current – Increase V_{BUR}**
- **Increase value of Cclamp and decrease Sec. Resonance cap. -Co1**
- **Enlarge the resonant current “ dip”**
- *** Select smaller Coss nonlinearity of high side MOSFET --IPx60R385CP**
- *** Select higher Coss nonlinearity of SR MOSFET**
- *** Smaller Lk of transformer**

Efficiency improve: (Specially for Si-FET)

➢ **Transformer design considerations :**

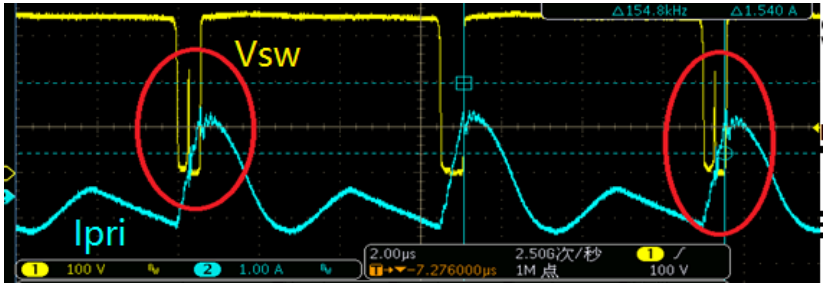
- Core material : TDK-N49, Ferroxcube-3F36
- Winding wire : Litz wire
- Delta B between 0.15~0.2T, < 0.1T more better

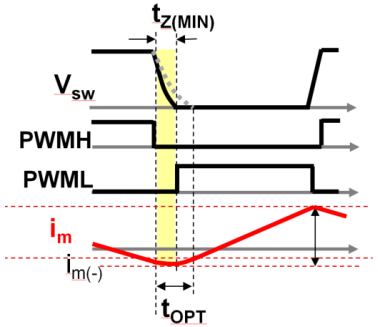
➢ **MOSFET selection:**

- High side : Smaller Coss, large Rdson is acceptable (Infineon CP series)
- Low side : Large Coss, smaller Rdson is prefer. (Infineon C7 series)

➢ **RTZ resistor setting:**

- High line input ,Increase RTZ until find Vsw ring back , then decrease a little

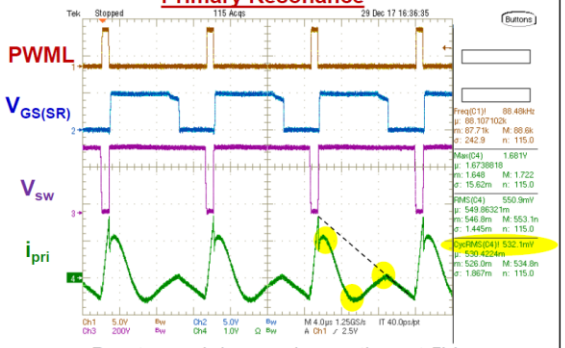




Secondary Resonance (Specially for PD design)

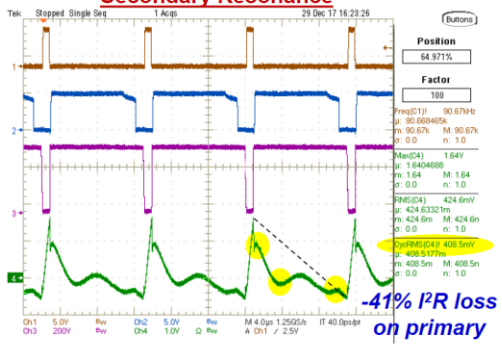
Condition: V_{bulk}=325V, V_o=5V, I_o=3A, C_{clamp}=0.44uF

Primary Resonance



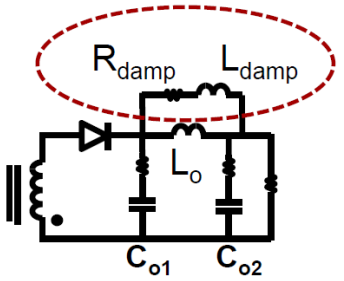
Due to much longer demag time at 5V, MUST use large C_{clamp} to maintain efficiency & proper SR operation

Secondary Resonance



I_o discharging C_{o1} every cycle allows resonance continuing even with long demagnetization time

- **Lower RMS loss on pri + sec side !!**
- **Better SR operation in AAM and ABM**



L_{damp}=680nH, R_{damp}=0.68Ω

Serial damping is needed

➢ Benefits of Secondary resonance

- Lowers conduction loss on primary side , results higher full load efficiency
- SR ZCS over wide output range, low turn off switching, also lower EMI
- Initial resonance current less than magnetizing current, easy SR operation
- Better for ripple

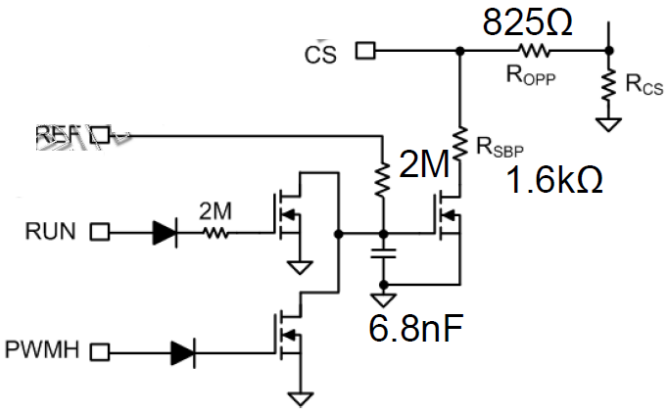
“Tiny load ” efficiency improve

➢ **Increasing Peak current**

1. Reducing sensing resistor

$$P = \frac{1}{2} L_m i_{m(+)}{}^2 f_{sw}$$

2. Active voltage divider on CS Pin



1. Effect on 20V/0.25W at V_{bulk}=325V

Rcs	Pin	Eff	f_{BUR}	f_{sw}	$I_{m(+)}$	OPP	$P_{O(OPP)}$
0.225	0.419W	59%	5.2K	686K	0.62A	120%	54W
0.192	0.406W	61%	4.4K	660K	0.68A	145%	65W

Gain 2% efficiency results in sacrificing OPP level

2-1. Effect on 20V/0.25W at V_{bulk}=325V

R_{SBP}	Pin	Eff	f_{BUR}	f_{sw}	$I_{m(+)}$
Open	0.419W	59%	5.2K	686K	0.62A
1.6K	0.385W	64%	3.3K	595K	0.94A

Gain 5% efficiency with same OPP level

2-2. Effect on 20V/0W at V_{bulk}=325V

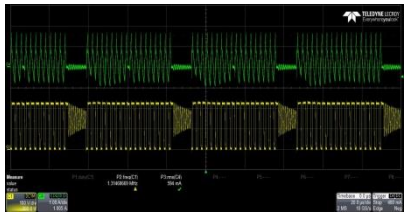
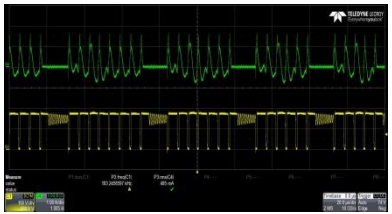
R_{SBP}	Pin	f_{BUR}	f_{sw}	$I_{m(+)}$
Open	55mW	790Hz	712K	0.54A
1.6K	46mW	430Hz	619K	0.74A

Gain 9mW standby power with same OPP level

PD design considerations

- **Balance 5V noise and 20V average efficiency**
  - Lower V_O results in lower f_{SW} operation
  - N_{SW} adjusts under lower f_{SW} case, f_{BUR} variation is larger
  - Larger f_{BUR} variation force ABM loop performing different Nsw Among adjacent burst packets –maybe lead to audible noise

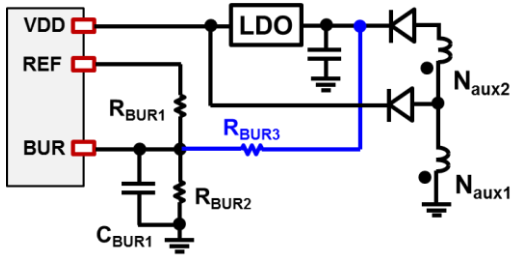
$$f_{BUR} = \frac{I_O}{I_{O(BUR)}} \frac{f_{SW}}{N_{SW}}$$

	Vo=20V (GaN)	Vo=5V (GaN)	Vo=5V (Silicon)
AAM-ABM Transition			
	N_{SW}>9	N_{SW}>5 (6-7-8-9)	N_{SW}>3 (3-4-5-6-7-8)

PD design considerations

- **Solution (Balance 5V noise and 20V average efficiency)**
  - V_o Feedforward Resistor to BUR Pin

V_o	V_{BUR}
20V	1.04V
5V	0.842V

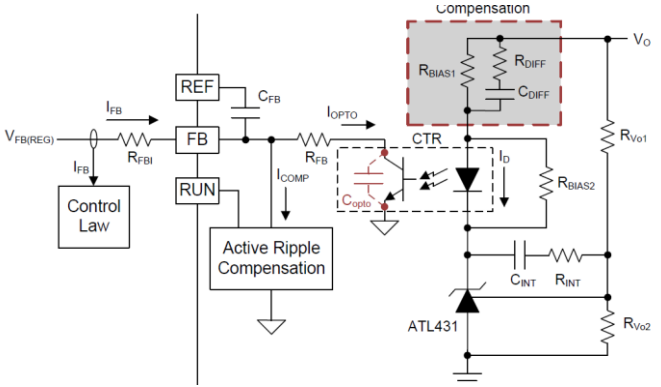


Reducing V_{BUR} at lower Vout mitigates audible noise but keeping high Vout average effi.

- **Another solution for mitigates 5V noise**
  - Narrow down ΔI_{FB} (Increase R_{BIAS1} ,Decrease C_{DIFF})

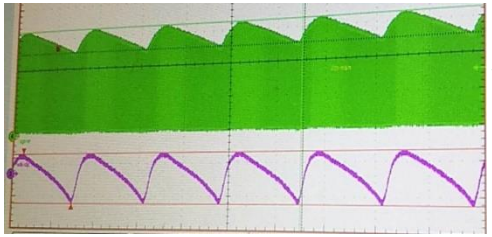
$$\Delta I_{FB} = K_{RIPPLE} \times \Delta V_{O(ABM)} \approx 10\mu A$$

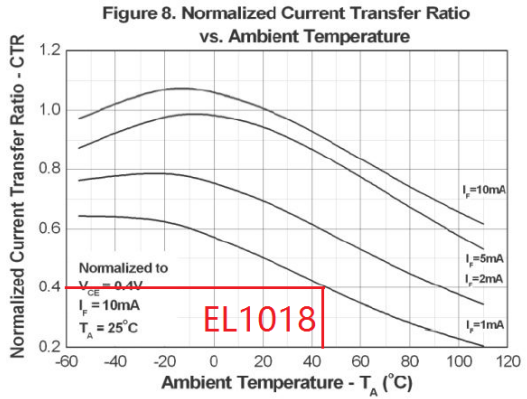
$$K_{RIPPLE} \equiv \frac{I_{FB}(s)}{V_o(s)}\bigg|_{20kHz<f<40kHz} \approx \frac{CTR}{R_{BIAS1}} \frac{\omega_{OPTO}}{\omega_{Z1}} = \frac{CTR}{R_{BIAS1}} \frac{(R_{DIFF} + R_{BIAS1})C_{DIFF}}{(R_{FB} + R_{FBI})C_{OPTO}}$$



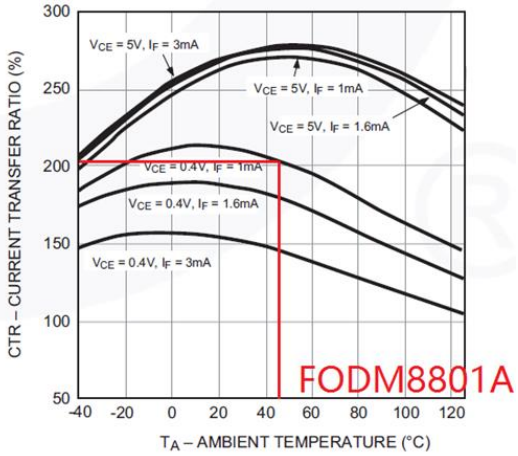
Large Vout AC ripple improvement

- **Choose appropriate optocoupler**
  - For lower standby power, UCC28780 iFB current designed to <0.1mA
  - The optocoupler with smaller iF current maybe have Lower CTR , Or poor performance as temperature variation .
  - Lead to lower low frequency gain to suppress the AC ripple .

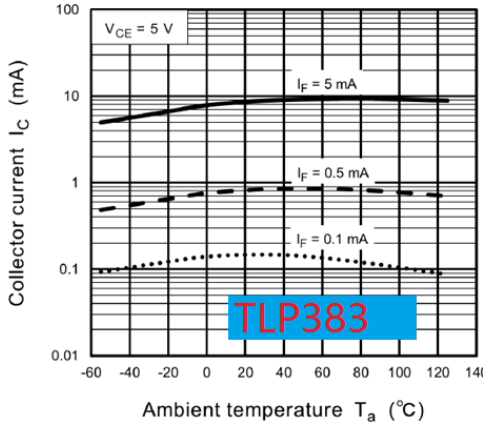




Not recommended



Proposed (5mm Creepage)



Proposed (8mm Creepage)