UCC28782 Introduction

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UCC28782 High-Frequency Active Clamp Flyback Controller

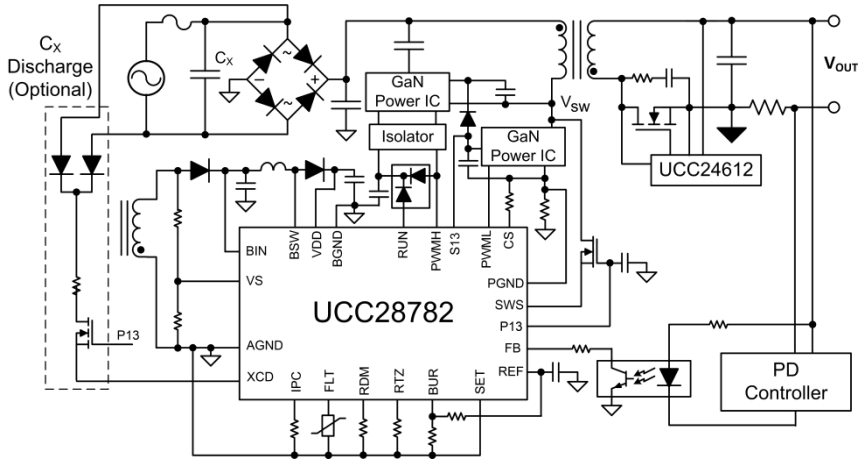
Features

- All features of UCC28780.
- Integrated bias power for efficient, dense, and single-winding V_{DD} regulation for wide V_{OUT} range.
- Driver and PFC power management for loss reduction.
- Frequency Dithering for low EMI and no audible noise.
- Active C_X discharge for low $P_{STANDBY}$, and with disable mode to eliminate line sensing components.
- New adaptive burst mode with auto-compensation and no audible noise for high average efficiency in wide V_{OUT} range.
- New deep light load mode for low $P_{STANDBY}$ and $P_{10\%\_LOAD}$.
- C_{CLAMP} auto-balancing in V_{OUT} scaling for low voltage stress.
- New protections: latch protections with fast reset, peak-power and over-power protections for wide V_{OUT}, and input line OVP.
- Low-side driving capability on PWML and PWMH.

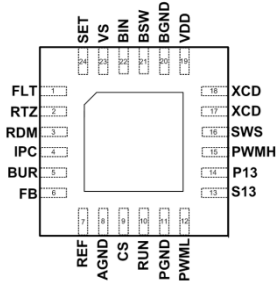
Applications

- High density and USB-PD adapters
- High efficiency AC/DC converter
- AC/DC or DC/DC auxiliary power supplies

Typical System Application (simplified)



Packaging



QFN 24-Pin; 4mm x 4mm

UCC28782: Auto-recovery

UCC28782L: Latch

SET to REF for Si device setting
SET to GND for GaN device setting

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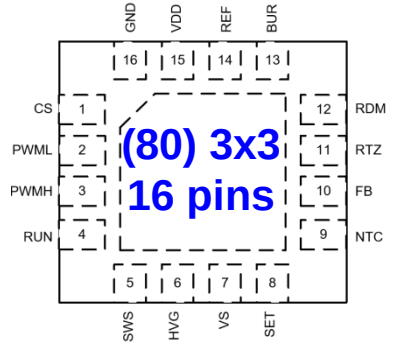
Response Options for Each Fault

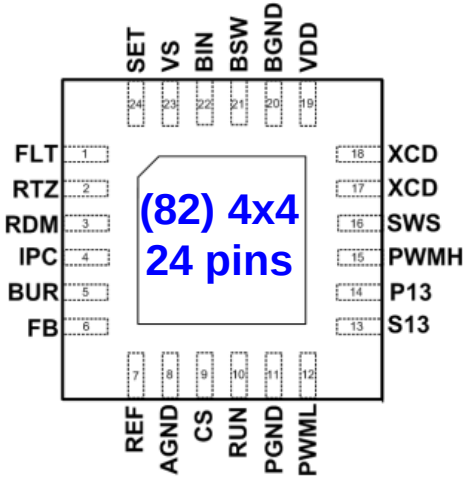
Fault Protections	Auto-Recovery Response (UCC28782)	Latch-off Group* (UCC28782L)
Output Over Voltage Protection (OVP)	✓ (1.5-s restart)	☑
Over Current Protection (OCP)	✓ (1.5-s restart)	
Output Short Circuit Protection (SCP)	✓ (1.5-s restart)	
Output Over Power Protection (OPP)	✓ (1.5-s restart)	
Output Peak Power Limit (PPL)	✓ (1.5-s restart)	
Over Temperature Protection (OTP) (on CS pin)	✓ (1.5-s restart)	
Over Temperature Protection (OTP) (on FLT pin)	✓ (VDD UVLO + V_{FLT} > 1.15V)	
Input Line OVP (LOVP) (on FLT pin)	✓ (VDD UVLO + V_{FLT} > 1.15V)	✘
VDD ULVO	✓ (VDD UVLO reset)	✘
Brown-in / Brown-out	✓ (VDD UVLO reset)	✘
Thermal Shutdown (internal T_J)	✓ (VDD UVLO reset)	✘
Open-Pin / Shorted-Pin	✓ (VDD UVLO reset)	✘

✓ = Standard in UCC28782 ☑ = Individual Option Available ☑ = Grouped Option Available ✘ = Option Not Available

*Latch reset method: V_{VDD} < 3.5V or line zero-crossing detect on XCD pin

Pin Comparison: 28782 vs. 28780





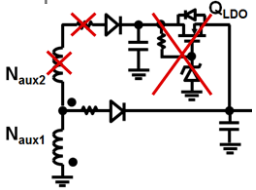
28782	28780	Description of Repurposed Pins
P13	HVG	P13 contains HVG & driver bias functions
FLT	NTC	FLT contains NTC OTP and line OVP sensing
AGND	GND	AGND = GND to differentiate other gnd pins

28782	Description of Additional Pins
PGND	Floating driver return ground (top of Rcs)
BGND	Source of the integrated boost MOSFET
BSW	Integrated boost MOSFET and switching control
BIN	Input voltage sense of the boost converter
IPC	Program light-load peak current and low-Vo compensation offset on CS pin
S13	Dynamic bias power management from P13
XCD	X cap discharge and/or fast latch-fault reset

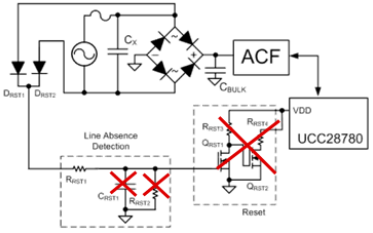
UCC28782 More Integration and Performance

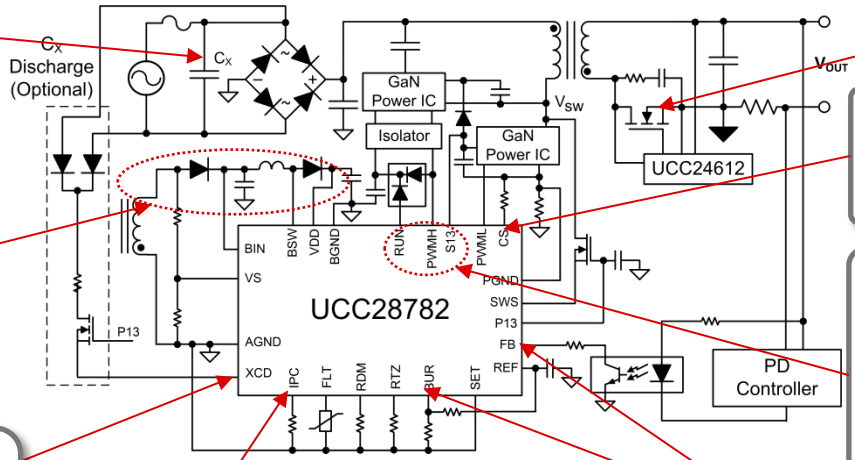
Smart EMI Dithering
Improve EMI by 7 dBµV

Integrated Bias Power
Lower bias power losses with wide output and 1 aux winding

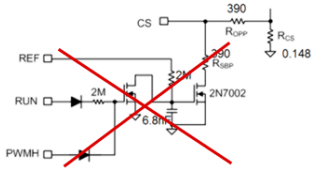


Active Cx Discharge + Fast Latch Reset
Removes bleed resistor loss; Reset latch fault < 2 Sec. from line removal





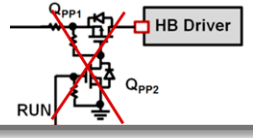
New Light Load Mode
Improves light load efficiency and standby power



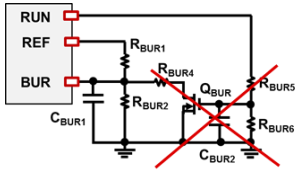
C_{clamp} Auto-Balancing
Reduces stress on SR FET

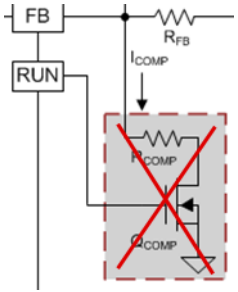
PD OPP & Ripple control
Optimize OPP level and minimize output ripple for wide Vo range

Driver Power Management
Reduce loss from gate drive, improve light efficiency and standby power

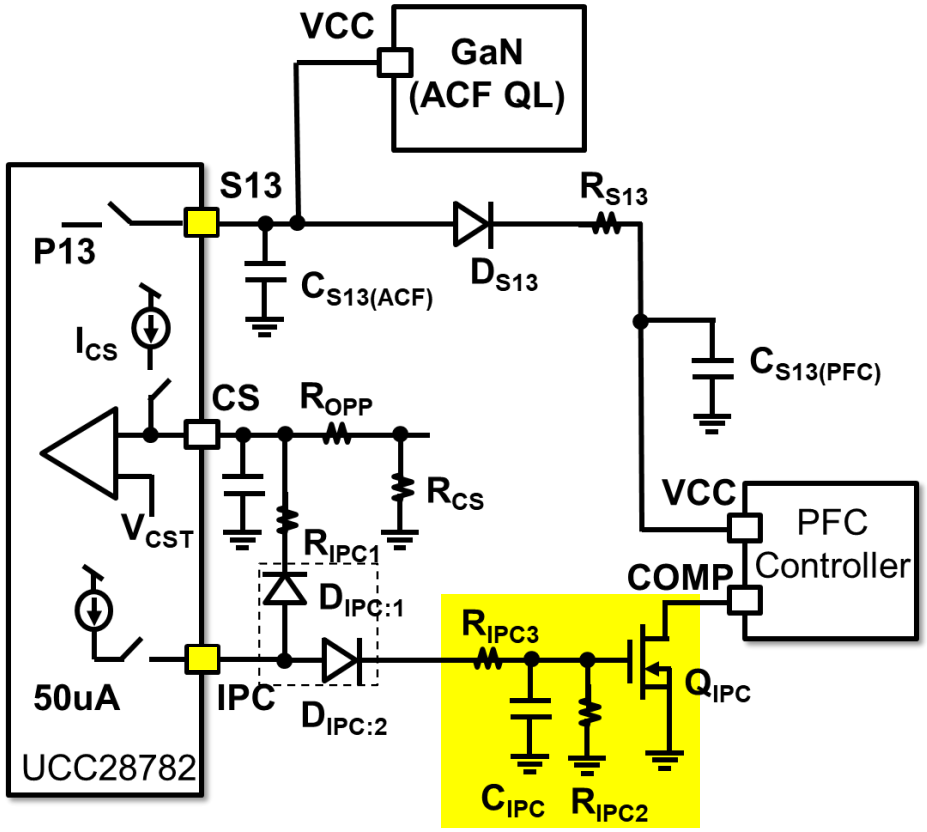


Burst Auto-Compensation
Stability between mode transition without external components





UCC28782 PFC Disable Control



Power management pins for PFC:

- S13: Disable PFC for deep light load and the low-side GaN driver of ACF
- IPC: Disable PFC for low Vo (V_{VS}<2.4V)

Performance Improvement:

- Significant low line efficiency gain due to low PFC output & PFC disable
- Moderate high line efficiency gain due to PFC disable

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