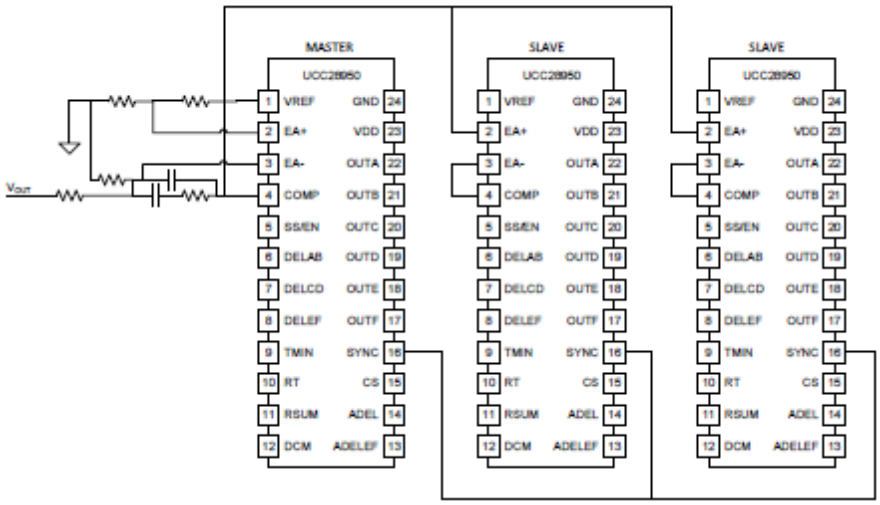
Good Morning,

I am glad the weekend is over. I have several questions regarding paralleling four UCC28951 IC's.

I found the following Figure 1 while in TI E2E forum regarding parallel systems. Appears to be pretty self-explanatory.

FIGURE 1)



If you have two UCC28950 power converters operating in parallel using peak current mode control with one feedback loop they should share current fairly well. The configuration you sent looks correct.

This works because one comp voltage controls the peak current level of both power stages. The level of the comp of the master controls both peak current limits of the slave as well. That is why the slave is setup in a voltage follower.

Now lets make it more interesting. I am paralleling qty 4 systems which means I need to us an external oscillator, correct? OK, I have worked that problem out using "*Synchronizing Three or More UCC28950 Phase-Shifted, Full-Bridge Controllers* SLUA609–September 2011". It works great as described in SUA609. I have all four sync signals ready to tie to pin 16 (Sync). Thanks TI.

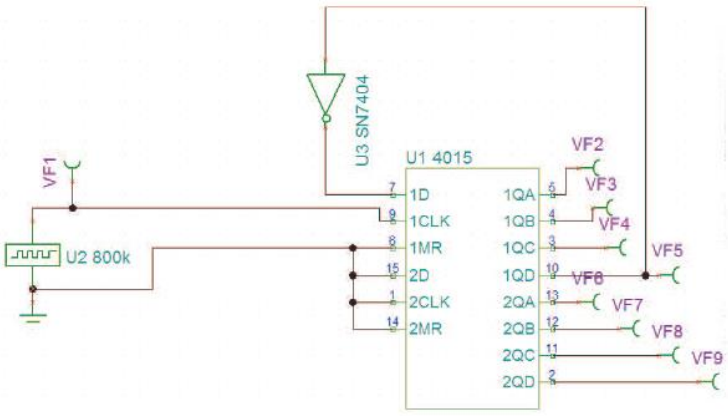
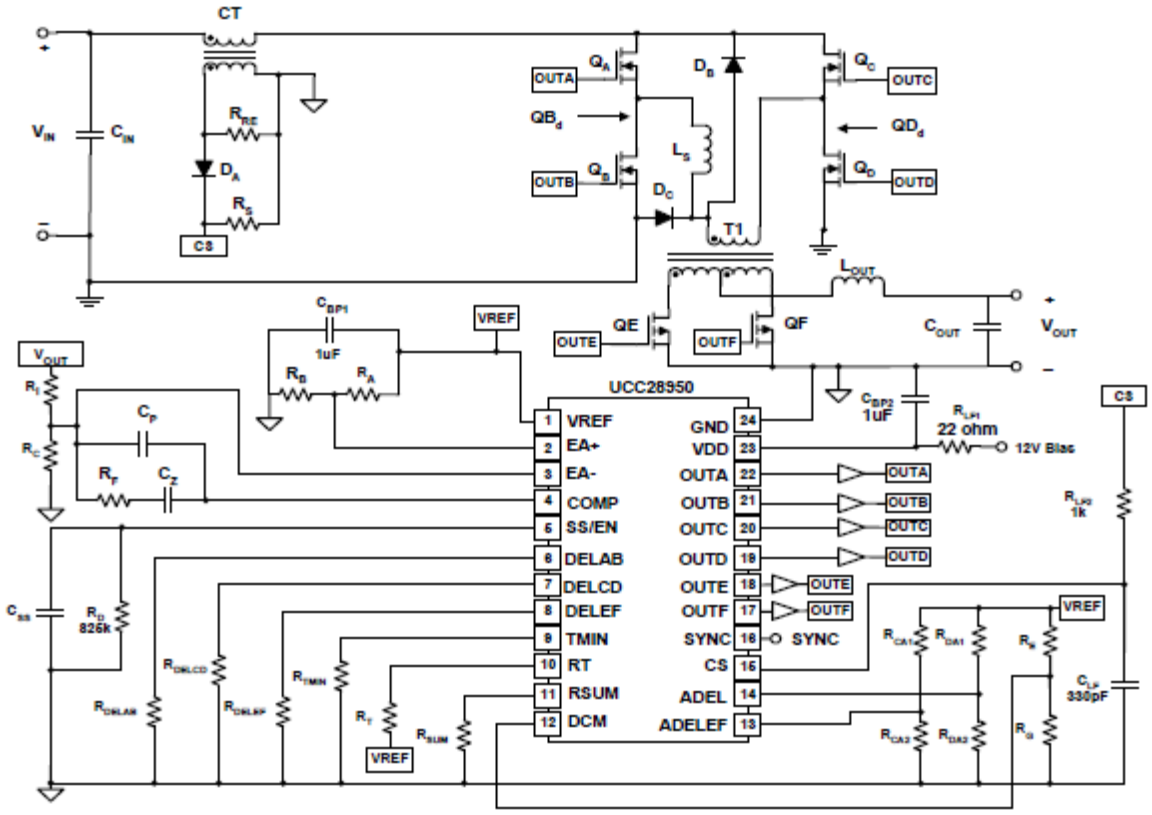


Figure 9. Four-Bit Shift-Register to Generate Four, Phase-shifted SYNC Signals From a Single Clock Source

The schematic below is the design that I used in conjunction with TI UCC28950 excel spreadsheet.

There are several questions as I mentioned earlier.

FIGURE 2) FUNCTIONAL SCHEMATIC



From what I understand that all four systems are sync'd from the external oscillator and the first system will have the Vsense control loop along with pin 1 and 2 according to figure 1. Also this first system will have the current sense transformer.

QUESTION 1) WILL THE OTHER THREE SYSTEMS BE REQUIRED TO ALSO HAVE CURRENT SENSE AND THAT THE CURRENT SENSE ON SYSTEM ONE WILL SENSE FULL CURRENT?

QUESTION 2) WILL PINS 5 THRU 12 REQUIRE ANY ALTERATIONS IN VALUE DUE TO THE EXTERNAL OSCILLATOR OTHER THAN SECTION 7.3.4 External clock synchronization as described below?

QUESTION 3) DO YOU HAVE ANY LITERATURE IN TI THAT I MIGHT ALSO REVIEW. I DID LOOK BUT DID NOT FIND ANYTHING.

Feature Description (continued)

7.3.4 External Clock Synchronization

The UCC28070 has also been designed to be easily synchronized to almost any external frequency source. By disabling frequency dithering (pulling CDR > 5 V), the SYNC circuitry is enabled permitting the internal oscillator to be synchronized with pulses presented on the RDM pin. To ensure a precise 180° phase shift is maintained between the GDA and GDB outputs, the frequency (f_{SYNC}) of the pulses presented at the RDM pin must be at twice the desired f_{PWM}. For example, if a 100-kHz switching frequency is desired, the f_{SYNC} should be 200 kHz.

$$f_{PWM} = \frac{f_{SYNC}}{2} \tag{7}$$

To ensure the internal oscillator does not interfere with the SYNC function, R_{RT} must be sized to set the internal oscillator frequency at least 10% below f_{SYNC}.

$$R_{RT}\left(k\Omega\right) = \frac{15000}{f_{SYNC}\left(kHz\right)} \times 1.1 \tag{8}$$

It must be noted that the PWM modulator gain is reduced by a factor equivalent to the scaled R_{RT} due to a direct correlation between the PWM ramp current and R_{RT}. Adjustments to the current loop gains should be made accordingly.

It must also be noted that the maximum duty-cycle clamp programmability is affected during external synchronization. The internal timing circuitry responsible for setting the maximum duty cycle is initiated on the falling edge of the synchronization pulse. Therefore, the selection of R_{DMX} becomes dependent on the synchronization pulse width (t_{SYNC}).

$$D_{SYNC} = t_{SYNC} \times f_{SYNC} \text{For use in } R_{DMX} \text{ equation immediately below.} \tag{9}$$

$$R_{DMX}\left(k\Omega\right) = \left(\frac{15000}{f_{SYNC}(kHz)}\right) \times \left(2 \times D_{MAX} - 1 - D_{SYNC}\right) \tag{10}$$

Consequently to minimize the impact of the t_{SYNC} it is clearly advantageous to use the smallest synchronization pulse width feasible.

NOTE

When external synchronization is used, a propagation delay of approximately 50 ns to 100 ns exists between internal timing circuits and the falling edge of the SYNC signal, which may result in reduced OFF-time at the highest of switching frequencies. Therefore, R_{DMX} should be adjusted downward slightly by (t_{SYNC} – 0.1 µs) / t_{SYNC} to compensate. At lower SYNC frequencies, this delay becomes an insignificant fraction of the PWM period, and can be neglected.
