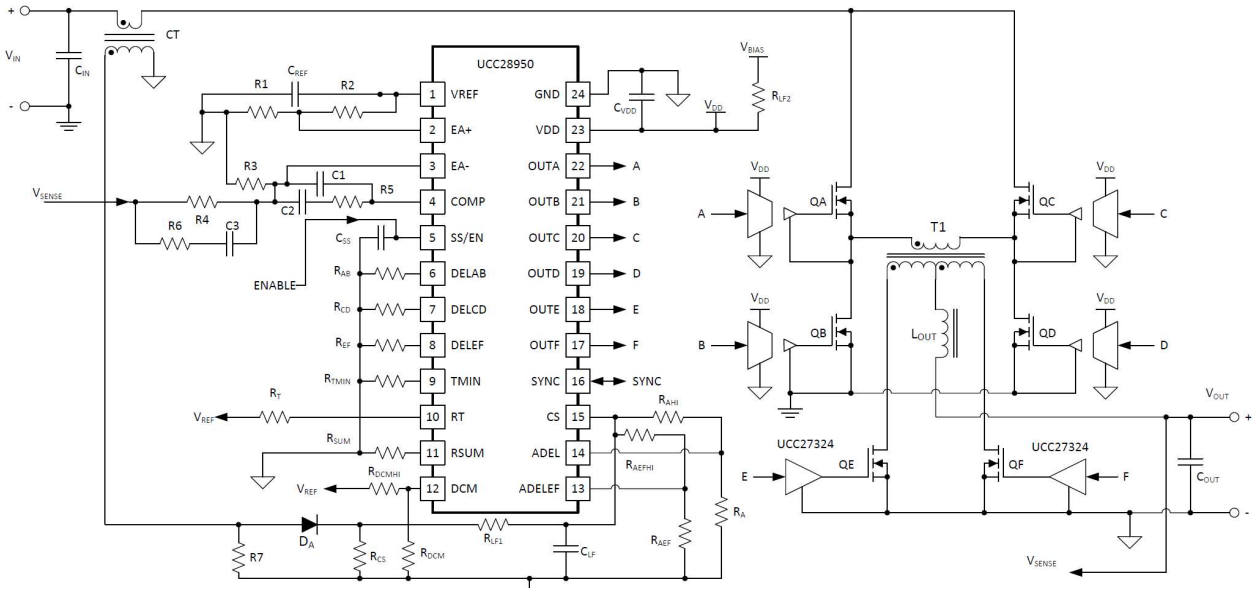
question

About dead time settings

UCC28950 Typical Application



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7.3.6 Adaptive Delay, (Delay between OUTA and OUTB, OUTC and OUTD (*DELAB, DELCD, ADEL*))

The resistor R_{AB} from the DELAB pin, DELAB to GND, along with the resistor divider R_{AHI} from CS pin to ADEL pin and R_A from ADEL pin to GND sets the delay T_{ABSET} between one of outputs OUTA or OUTB going low and the other output going high Figure 28. The total resistance of this resistor divider should be in the range between 10 kΩ and 20 kΩ

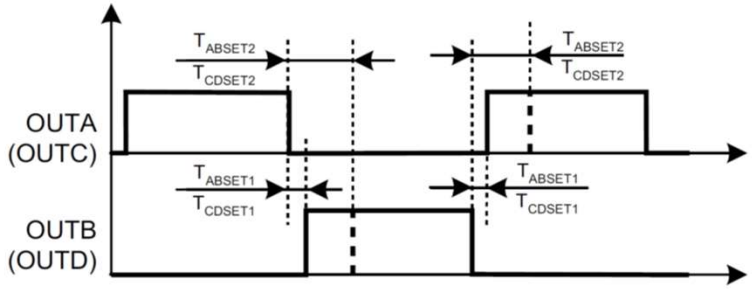

Figure 28. Delay Definitions Between OUTA and OUTB, OUTC and OUTD

This delay gradually increases as a function of the CS signal from T_{ABSET1}, which is measured at V_{CS} = 1.8 V, to T_{ABSET2}, which is measured at the V_{CS} = 0.2 V. This approach ensures there will be no shoot-through current during the high-side and low-side MOSFET switching and optimizes the delay for acheiving ZVS condition over a wide load current range. The ratio between the longest and shortest delays is set by the resistor divider R_{AHI} and R_A. The max ratio is achieved by tying the CS and ADEL pins together. If ADEL is connected to GND, then the delay is fixed, defined only by the resistor R_{AB} from DELAB to GND. The delay T_{CDSET1} and T_{CDSET2} settings and their behaviour for outputs OUTC and OUTD are very similar to the one described for OUTA and OUTB. The difference is that resistor R_{CD} connected between DELCD pin and GND sets the delay T_{CDSET}. The ratio between the longest and shortest delays is set by the resistor divider R_{AHI} and R_A.

The delay time T_{ABSET} is defined by the following Equation 3.

$$T_{ABSET} = \left(\frac{5 \times R_{AB}}{0.26\,V + CS \times K_A \times 1.3} \right) ns \quad (3)$$

The same equation is used to define the delay time T_{CDSET} in another leg except R_{AB} is replaced by R_{CD}.

$$T_{CDSET} = \left(\frac{5 \times R_{CD}}{0.26\,V + CS \times K_A \times 1.3} \right) ns \quad (4)$$

In these equations R_{AB} and R_{CD} are in kΩ and CS, the voltage at pin CS, is in volts and K_A is a numerical coefficient in the range from 0 to 1. The delay time T_{ABSET} and T_{CDSET} are in ns, and is measured at the IC pins. These equations are empirical and they are approximated from measured data. Thus, there is no unit agreement in the equations. As an example, assume R_{AB} = 15 kΩ, CS = 1 V and K_A = 0.5. Then the T_{ABSET} will be approximately 90 ns. In both Equation 3 and Equation 4, K_A is the same and is defined as:

$$K_A = \frac{R_A}{R_A + R_{AHI}} \quad (5)$$

K_A sets how the delay varies with the CS pin voltage as shown in Figure 29 and Figure 30.

Feature Description (continued)

It is recommended to start by setting K_A = 0 and set T_{ABSET} and T_{CDSET} relatively large using equations or plots in this data sheet to avoid hard switching or even shoot through current. The delay between outputs A, B and C, D set by resistors R_{AB} and R_{CS} accordingly. Program the optimal delays at light load first. Then by changing K_A set the optimal delay for the outputs A, B at maximum current. K_A for outputs C, D is the same as for A,D. Usually outputs C, D always have ZVS if sufficient delay is provided.

NOTE

The allowed resistor range on DELAB and DELCD, R_{AB} and R_{CD} is 13 kΩ to 90 kΩ.

R_A and R_{AHI} define the portion of voltage at pin CS applied to the pin ADEL (See Figure 48). K_A defines how significantly the delay time depends on CS voltage. K_A varies from 0, where ADEL pin is shorted to ground (R_A = 0) and the delay does not depend on CS voltage, to 1, where ADEL is tied to CS (R_{AHI} = 0). Setting K_A, R_{AB} and R_{CD} provides the ability to maintain optimal ZVS conditions of primary switches over load current because the voltage at CS pin includes the load current reflected to the primary side through the current sensing circuit. The plots in Figure 29 and Figure 30 show the delay time settings as a function of CS voltage and K_A for two different conditions: R_{AB} = R_{CD} = 13 kΩ (Figure 29) and R_{AB} = R_{CD} = 90 kΩ (Figure 30).

From the attached application materials,

As an example, assume R_{AB} = 15 kΩ, CS = 1 V and K_A = 0.5. In that case, it says T_{ABSET} will be about 90 ns. However, when Equation 3 is actually calculated, T_{ABSET} = 82.4 ns, which does not match.
Also, if R_{AB} = R_{CD} = 15 kΩ and pin ⑭ ADEL of this IC is connected to GND, K_A = 0, so calculating Equation 3 and Equation 4 yields T_{ABSET} = T_{CDSET} = 288.5 ns.
However, when this IC is operated and the delay time between OUTA and OUTB and between OUTC and OUTD is measured, T_{ABSET} = T_{CDSET} = 340 ns, which do not match.

Therefore, I would like to ask you the following questions, please answer them.

①Is the dead time calculation method correct for the application?

②If it is different, please let me know how to calculate it.

③If so, what is the reason for the difference between the calculated value and the measured value? Is it due to variations in parts?
In addition, the resistance value accuracy of the setting resistor is ±0.5%.

④How much variation should we assume for this IC itself with respect to dead time?

⑤I would like to receive information about IC variations, changes due to temperature fluctuations and aging deterioration.