Functional Safety Information

UCx84xA
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview 2
2 Functional Safety Failure In Time (FIT) Rates 3
2.1 SOIC (8) Package 3
2.2 PDIP (8) Package 4
3 Failure Mode Distribution (FMD) 5
4 Pin Failure Mode Analysis (Pin FMA) 6
4.1 SOIC (8) Package 6
4.2 PDIP (8) Package 9

Trademarks

1 Overview

This document contains information for the UCx84xA(including UC2842A, UC2843A, UC2844A, UC2845A, UC3842A, UC3843Am UC3844A, and UC3845A) (SOIC (8) and PDIP (8) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

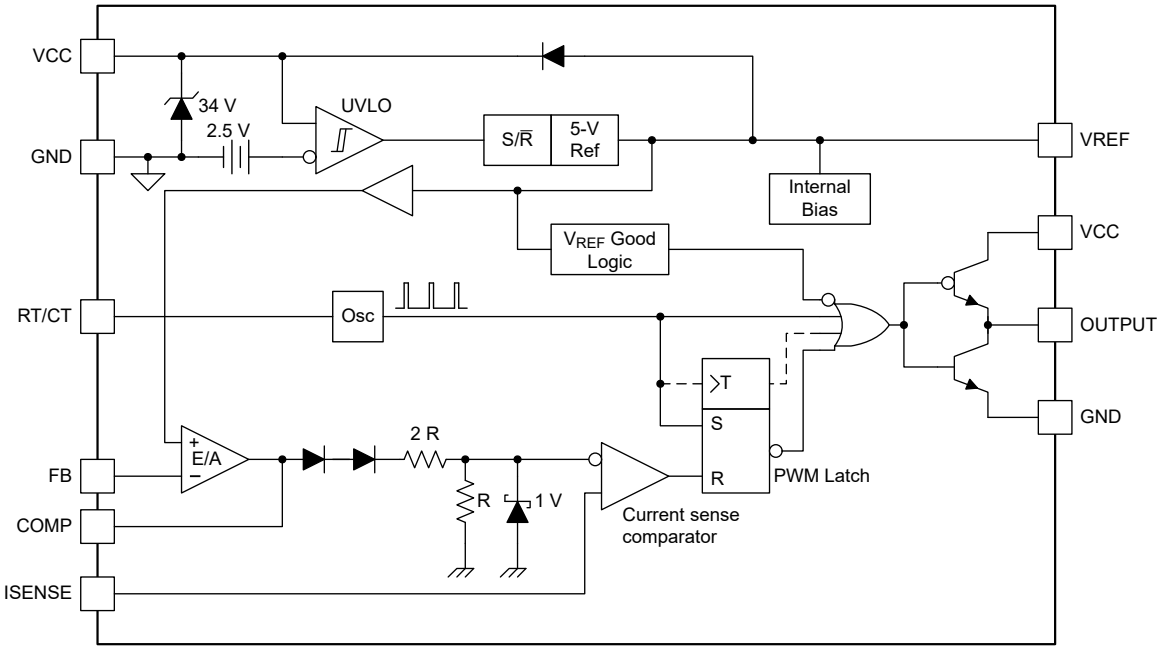

Figure 1-1. Functional Block Diagram

The UCx84xA was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC (8) Package

This section provides functional safety failure in time (FIT) rates for the SOIC (8) package of the UCx84xA based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate (100 mW, 200 mW, 500 mW)	10, 13, 20
Die FIT rate (100 mW, 200 mW, 500 mW)	3, 5, 12
Package FIT rate (100 mW, 200 mW, 500 mW)	7, 8, 8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 100, 200, 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Bipolar Op Amp, Comparators, Voltage Monitors	6 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 PDIP (8) Package

This section provides functional safety failure in time (FIT) rates for the PDIP (8) package of the UCx84xA based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate (100 mW, 300 mW, 700 mW)	22, 23, 29
Die FIT rate (100 mW, 300 mW, 700 mW)	3, 4, 8
Package FIT rate (100 mW, 300 mW, 700 mW)	19, 19, 21

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 100, 300, 700 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Bipolar Op Amp, Comparators, Voltage Monitors	6 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCx84xA in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTPUT stays low	36
OUTPUT stays high	16
Wrong OUTPUT pulse width	16
System is unstable	7
No effect	25

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCx84xA (SOIC (8) and PDIP (8) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VCC is considered as supply pin
- IC is connected as the typical application design example schematic shown in the datasheet Application and Implementation section

4.1 SOIC (8) Package

Figure 4-1 shows the UCx84xA pin diagram for the SOIC (8) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCx84xA data sheet.

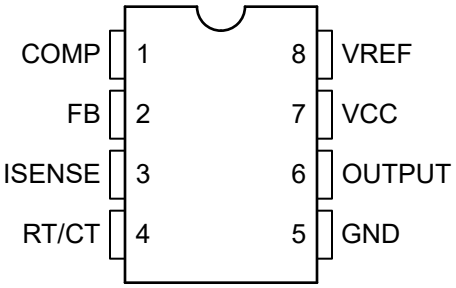

Figure 4-1. Pin Diagram (SOIC (8)) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	OUTPUT stays low. Converter has no output.	B
FB	2	Controller tries to demand maximum power. Converter operates with maximum peak current. Output loses regulation.	B
ISENSE	3	Controller has no current signal, demands maximum power. Power stage likely to be damaged. Once the power stage is damaged, controller will be damaged.	A
RT/CT	4	OUTPUT stays low. Converter has no output.	B
GND	5	No effect.	D
OUTPUT	6	OUTPUT stays low. Converter has no output. Controller damage is possible.	A
VCC	7	Controller is not biased. OUTPUT stays low. Converter has no output.	B
VREF	8	Controller stays off. Converter has no output. Possible IC damage.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	COMP is unstable. Converter output is unstable.	B
FB	2	OUTPUT stays low. Converter has no output.	B
ISENSE	3	OUTPUT stays low. Converter has no output.	B
RT/CT	4	OUTPUT stays low. Converter has no output.	B
GND	5	Controller behavior is unpredictable. Controller damage is possible.	A
OUTPUT	6	Converter has no output.	B
VCC	7	Controller is not biased. OUTPUT stays low. Converter has no output.	B
VREF	8	VREF is unstable. Converter output is unstable.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	FB	COMP stays at 2.5V. Converter output is unregulated.	B
FB	2	ISENSE	COMP stays at high. Converter output is unregulated.	B
ISENSE	3	RT/CT	Oscillator stops. OUTPUT stays low. Converter has no output.	B
RT/CT	4	N/A		D
GND	5	OUTPUT	OUTPUT stays low. Converter has no output. IC damage is possible.	A
OUTPUT	6	VCC	OUTPUT stays high. IC damage is possible. Converter has no output.	A
VCC	7	VREF	VREF voltage exceeds abs. max rating. IC damage. Converter has no output.	A
VREF	8	N/A		D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	COMP voltage exceeds abs. max rating. IC damage is possible. OUTPUT has maximum duty cycle. Converter output is unregulated.	A
FB	2	FB voltage excess abs. max rating. IC damage is possible. OUTPUT remains low. Converter has no output.	A
ISENSE	3	ISENSE voltage exceeds abs. max rating. IC damage is possible. OUTPUT remains low. Converter has no output.	A
RT/CT	4	RT/CT voltage exceeds abs. max rating. IC damage is possible. OUTPUT remains low. Converter has no output.	A
GND	5	IC is not biased. OUTPUT stays low. Converter has no output.	B
OUTPUT	6	OUTPUT stays high. IC damage is possible. Converter has no output.	A
VCC	7	No effect.	D
VREF	8	VREF voltage exceeds abs. max rating. IC damage is possible. Converter output is unregulated.	A

4.2 PDIP (8) Package

Figure 4-2 shows the UCx84xA pin diagram for the PDIP (8) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCx84xA data sheet.

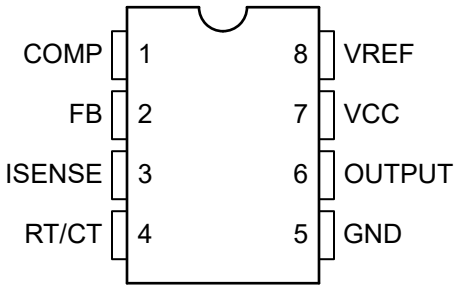

Figure 4-2. Pin Diagram (PDIP (8) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	OUTPUT stays low. Converter has no output.	B
FB	2	Controller tries to demand maximum power. Converter operates with maximum peak current. Output loses regulation.	B
ISENSE	3	Controller has no current signal, demands maximum power. Power stage likely to be damaged. Once the power stage is damaged, controller will be damaged.	A
RT/CT	4	OUTPUT stays low. Converter has no output.	B
GND	5	No effect.	D
OUTPUT	6	OUTPUT stays low. Converter has no output. Controller damage is possible.	A
VCC	7	Controller is not biased. OUTPUT stays low. Converter has no output.	B
VREF	8	Controller stays off. Converter has no output. Possible IC damage.	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	COMP is unstable. Converter output is unstable.	B
FB	2	OUTPUT stays low. Converter has no output.	B
ISENSE	3	OUTPUT stays low. Converter has no output.	B
RT/CT	4	OUTPUT stays low. Converter has no output.	B
GND	5	Controller behavior is unpredictable. Controller damage is possible.	A
OUTPUT	6	Converter has no output.	B
VCC	7	Controller is not biased. OUTPUT stays low. Converter has no output.	B
VREF	8	VREF is unstable. Converter output is unstable.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	FB	COMP stays at 2.5V. Converter output is unregulated.	B
FB	2	ISENSE	COMP stays at high. Converter output is unregulated.	B
ISENSE	3	RT/CT	Oscillator stops. OUTPUT stays low. Converter has no output.	B
RT/CT	4	N/A		D
GND	5	OUTPUT	OUTPUT stays low. Converter has no output. IC damage is possible.	A
OUTPUT	6	VCC	OUTPUT stays high. IC damage is possible. Converter has no output.	A
VCC	7	VREF	VREF voltage exceeds abs. max rating. IC damage. Converter has no output.	A
VREF	8	N/A		D

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	COMP voltage exceeds abs. max rating. IC damage is possible. OUTPUT has maximum duty cycle. Converter output is unregulated.	A
FB	2	FB voltage excess abs. max rating. IC damage is possible. OUTPUT remains low. Converter has no output.	A
ISENSE	3	ISENSE voltage exceeds abs. max rating. IC damage is possible. OUTPUT remains low. Converter has no output.	A
RT/CT	4	RT/CT voltage exceeds abs. max rating. IC damage is possible. OUTPUT remains low. Converter has no output.	A
GND	5	IC is not biased. OUTPUT stays low. Converter has no output.	B
OUTPUT	6	OUTPUT stays high. IC damage is possible. Converter has no output.	A
VCC	7	No effect.	D
VREF	8	VREF voltage exceeds abs. max rating. IC damage is possible. Converter output is unregulated.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265