Design Note, This negative regulator section is used only in the event LEDs are not driven pass threshold. TBD at default design review, placed here as a bypass option to header

TP8 TEST POINT

CD 10uF

U6 LM2664 (GND, Out, Cap+, Vc, Cap-, SD)

Cc 10uF

VCC_4v

U5 LP3984 (Vin, GRD, Ven, Vout, NC)

CA 1uF

CB 1uF

R34 300 D6 LDO6

R3 300 D7 LDO5

300 R13 D8 LDO7

J8 Led en

LDO-outputs 5-7

J9

TP26 GRD-turrent pin

TP24 LDO7_turret

TP23

TP25 LDO5_turret

LDO6_turret

C10 1uF C11 1uF C12 1uF

TP21 Turrent pin TP22 Turrent pin

J4 output

R4 R RS R

R10 R R11 R

C7 10uF C8 1.0uF

U7 LP3921 (LDO6, TX_EN, LDO5, VIN2, LDO7, OUT2, VDD, OUT-, IN+, GND, GND, LDO4, LDO3, LDO2, LDO1, RX_EN, ACOK_N, RESET_N, VSS, HF_PWR, TCXO_EN, PS_HOLD, IMON, PWR_ON, CHG_IN, BATT, SCL, SDA, GNDA, VIN1)

C6 10uF

J12 VIN_1, VDD_audio, VIN_2

VIN_input

C13 1uF C14 1uF C15 1uF C16 1uF

R6 R R7 R

TP19 Turrent pin TP20 Turrent pin

J6 input

C5 1uF

TP11 LDO3 TP18 LDO4 TP17 GRD

TP10 LDO2 TP7 LDO1

J5 LED EN

J7 LDO1-4- outputs

D17 LDO_4 D18 LDO_3 D13 LDO_2 D14 LDO_1

R32 300 R33 300 R28 300 R29 130

Default Voltages at startup
LDO1: 1.8V@300mA
LDO2: 3.0V @300mA
LDO3: 3.0V @80mA
LDO4: 3.0V @80mA
LDO5: 3.0V @150mA
LDO6: 3.0V @150mA
LDO7: 3.0V @150mA

Design Note, Decoupling caps for each LDO input/output are to be in close proximity of each output pin

Design Note: All LEDS are 1206 packages

R15 300 D9 Reset_N

TP6 SPARE_SOLDERpad

TP9 SPARE_solderpad

S1 EN_bank (TX_EN, RX_EN)

J13 Digital outputs (ACOK_N, Reset_N, PGM_N, IMON)

S2 SW DIP-4 (HF_PWR, TXCO_EN, PS_HOLD, PWR_ON)

R12 0

S3 PWR_EN momentary

J14 Wall adapter host input

TP5 Turrent pin

C9 10uF

TP15 Turrent pin TP14 Solder pad

J10

EXT_Batt

TP28 Turret Pin TP27 solderpad

SCL SDA

J11 COP8 ISOLATION EN

J15 COP8 Isolation EN

Design Note: D1 *may* be substituted with a R=<45 ohms pending version

Design Note: The 3.3v voltage supply,is isolated on a separate ground plane as to minimize the current contamination.

D1 IN914

L1 1uH L2 1uH

C1 10uF C2 100uF

U1 LP2981_3.3 (VIN, GRD, VOUT, NC, ON/OFF)

Design Note: 1206 sizes

Design Note: This is the +3.3v source for powering the logic devices.

VCC_3.3V

C3 100uF

J1 USB voltage selection

Design Note: This voltage selection jumper is to be used for selection between powering device directly from the USB port, or external PS/Battery

VCC_BATT

TP1 Batt

Design Note: This is the +5 volt USB line

R17 10K

VCC_3.3V

D10 DIODE SCHOTTKY

R18 10K

RESET_USB SW1

C21 10uF

J2 USB-B (5volt, Data-, Data+, Grd, Case_grd)

C17 47pf C18 47pf

R19 22 R20 22

24MHZ HC49_SMX

R21 1meg Q1 C27 15pf C28 15pf

U3 USBN9604 (CS_N, RD_N, WR_N/SK, INTR, DRQ, DACK_N, AO/ALE/SI, OO/ISO, D1, D2, D3, D4, D5, D6, CLKout, XOut, Xin, Mode 0, Mode 1, GRD2, Vcc, D-, D+, V3.3, AGRD, RESET_N, D7)

VCC3.3V

R22 10K

R24 10K

C30 0.1uF

R25 1.5K

COP8 flash pinouts
SO
SK
SI
GRD

J3 FlashPRG

U4 COP8 (Reset_N, G0, G1, G2, G3, G4, G5, G6, G7, CKI, L0, L1, L2, L3, L4, L5, L6, L7, B0, B1, B2, B3, B4, B5, D7, D6, D5, D4, D3, D2, D1, D0, A7, A6, A5, A4, A3, A2, A1, A0, Vcc, AVcc, NC2, NC1, AGRD, DGRD, B7, B6, RF_PWR, TCXO_EN, PS_HOLD, PWR_ON, TX_EN, RX_EN, IMON, LDO7, LDO1, LDO2, LDO3, LDO4, LDO5, LDO6)

SDA SCL

C32 0.1uF C33 0.1uF

VCC_3.3V

C31 1uF R26 10K R27 10K

SDA SCL

Design Note: I2C Active high drive pull ups

Design Note: For noise isolation from the digital IO and ESD latchup issues, this point is the only input entry point onto the power plane

Design Note: R13 is removed if U2 LM3658 is not stuffed

Design Note: U2 LM3658 is optional and is not stuffed if evaluation board is run either from an external PS or in demo mode via the USB port.

Design Note: Pin assignments for COP8 interface
LDO1 pin16 = B0 pin 19
LDO2 pin15= B1pin 20
LDO3 pin14 = B2 pin 21
LDO4 pin13= B3 pin 22
LDO5 pin3= B4 pin 23
LDO6 pin1 = B5 pin 24
LDO7 pin5 =B6 pin 25

SDA pin 19 = A7 pin 40
SCL pin 20= A6 pin 39
RX_EN pin32 =A0 pin33
TX_EN pin2 =A1 pin 34
PWR_ON pin23 =A2 pin 35
PS_HOLD pin 25=A3 pin 36
TCXO_EN pin 26=A4 pin 37
HF_PWR pin27= A5 pin 38

Design Note: All headers and LEDS must be labeled clearly

Design Note: All LEDS are 1206 packages

Design Note: Grd Plane will consist of guarded plane to direct electron flow for most quiet operation. Digital logic interface will have separate grd shield.

Design Note: Switcher components MUST be located as close to pins as possible. SEE LAYOUT DETAILS

Title	LP3921 PMU-audio USB Design by Sheldon Mah 408 721 3626		
Size D	Document Number: 6X5 package with datasheet 0.9 or greater pinout configuration	REVA5X5	Rev
Date: Tuesday, December 04, 2007	Sheet 1 of 1		