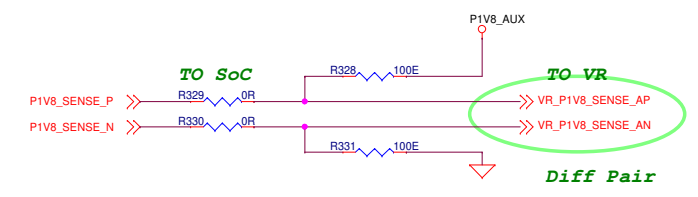


**CHANNEL-A**  
 VCCIN\_V1V8  
 VID- 1.8V  
 VBOOT- 1.8V  
 SVID\_RANGE- 1.5V to 2V  
 ICC\_TDC- 39A  
 ICC\_MAX- 102A  
 PHASE- 3  
 SVID- 0x00  
 DC\_TOLERANCE- 0.5%  
 RIPPLE- 6mV

**CHANNEL-B**  
 P1V8\_AUX  
 SVID\_RANGE- STATIC  
 ICC\_TDC- 1.6A  
 ICC\_MAX- 2A  
 PHASE- 1  
 SVID- 0x01  
 DC\_TOLERANCE- 0.5%  
 RIPPLE- 6mV

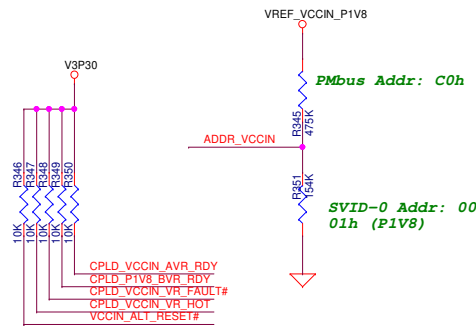
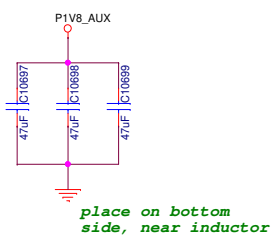


Thru OE:  
 Remote ref point  
 near sink

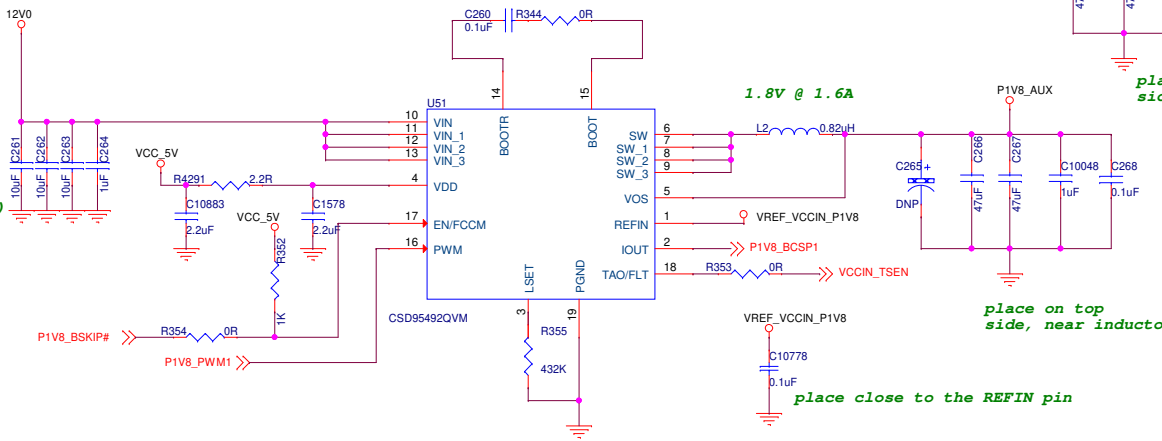
Thru 100E:  
 Local ref point  
 near inductor

SMBus:  
 Open drain, Pullup 3v3  
 common for all VR.  
 add buffer

TO SoC  
 TO VR  
 Diff Pair



PMBus Addr: C0h  
 SVID-0 Addr: 00h (VCCIN)  
 01h (P1V8)

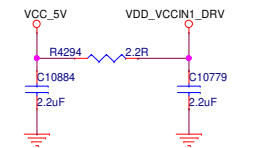


1.8V @ 1.6A

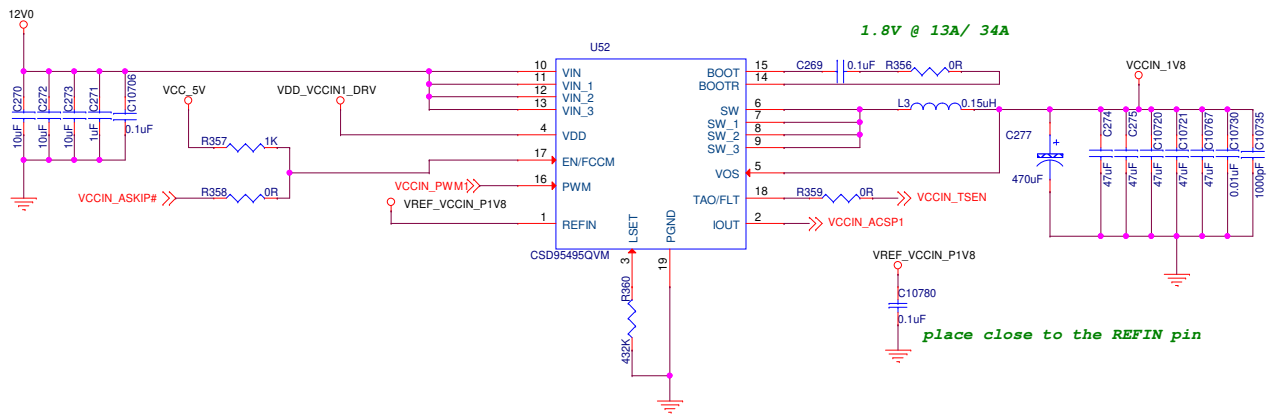
place on top side, near inductor

place close to the REFIN pin

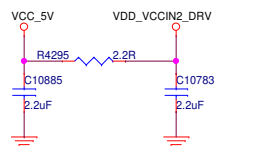
Title	<Title>	Rev	<Rev Code>
Size	A3	Document Number	<Doc>
Date:	Sunday, April 14, 2024	Sheet	1 of 1



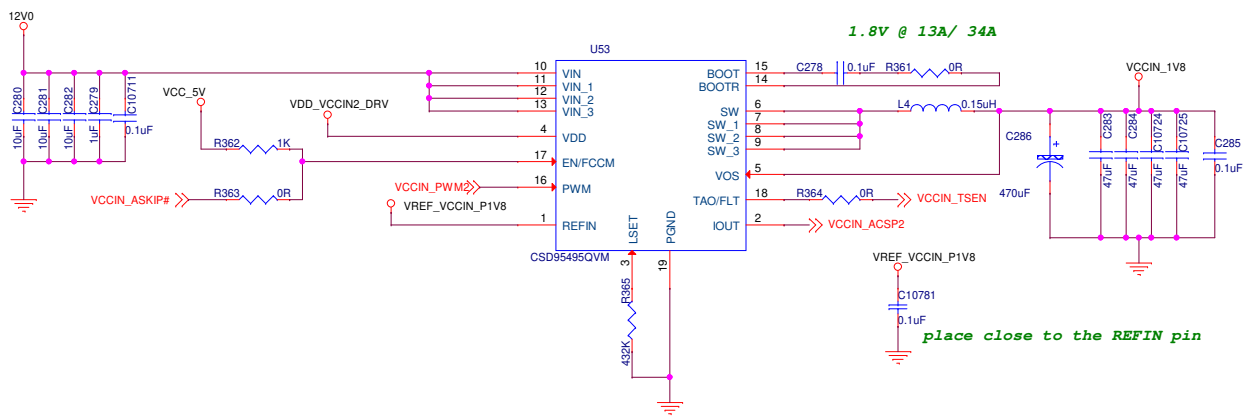
place close to the VDD pin



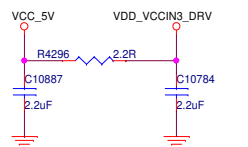
place close to the REFIN pin



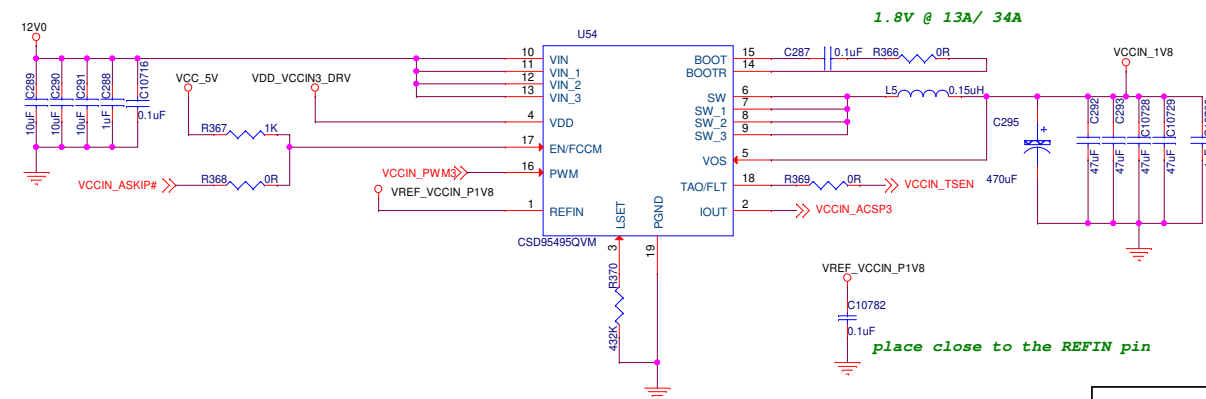
place close to the VDD pin



place close to the REFIN pin



place close to the VDD pin



place close to the REFIN pin

Title	<Title>	Rev	<Rev>
Size	A3	Document Number	<Doc>
Date:	Sunday, April 14, 2024	Sheet	1 of 1