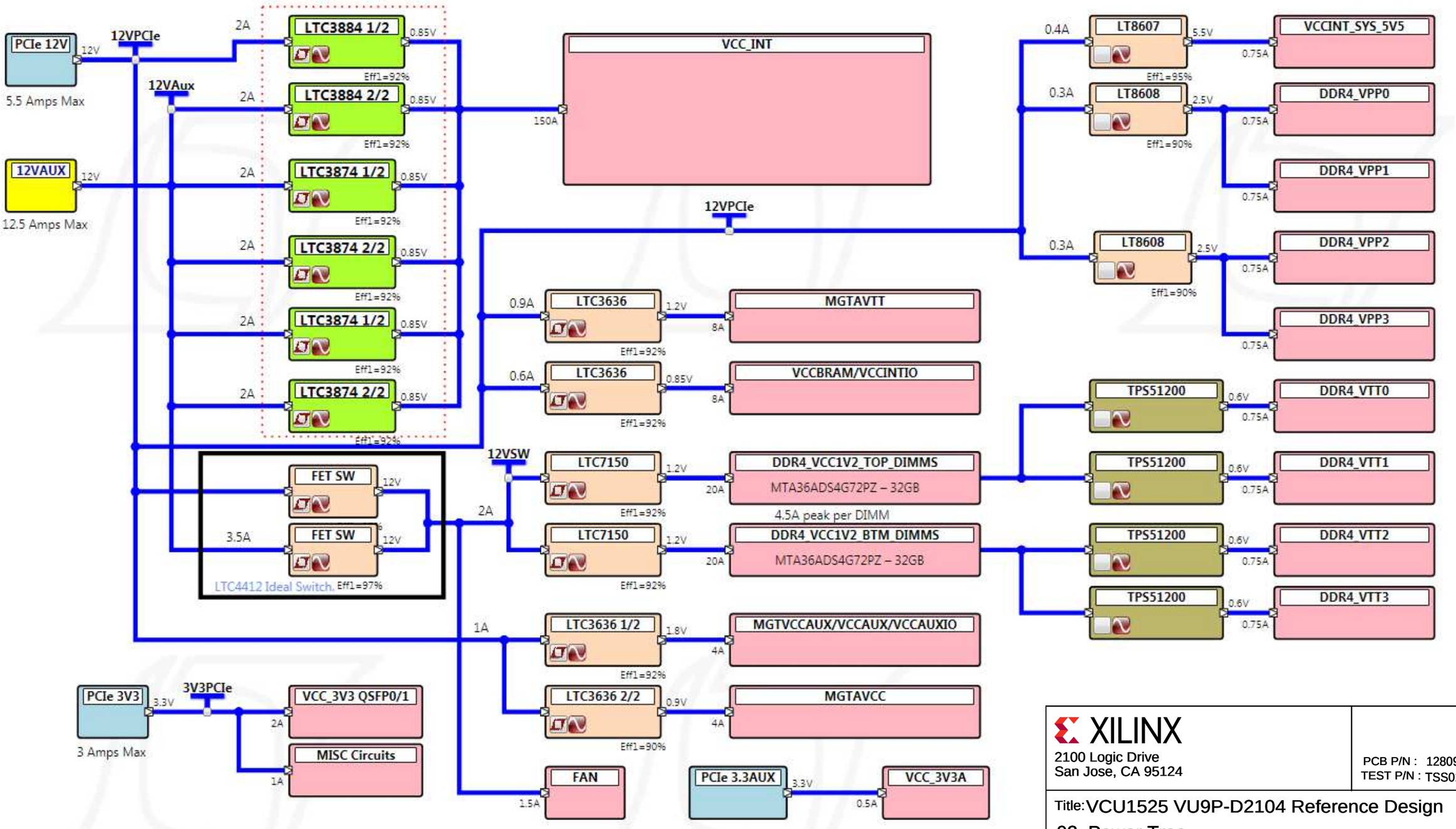
Power Tree

VCCINT is a 6-Phase PMBUS controllable Buck desing with one master controller and two slaves with 25Amps per phase.



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San Jose, CA 95124

PCB P/N : 1280962
TEST P/N : TSS0198

Title: VCU1525 VU9P-D2104 Reference Design

02. Power Tree

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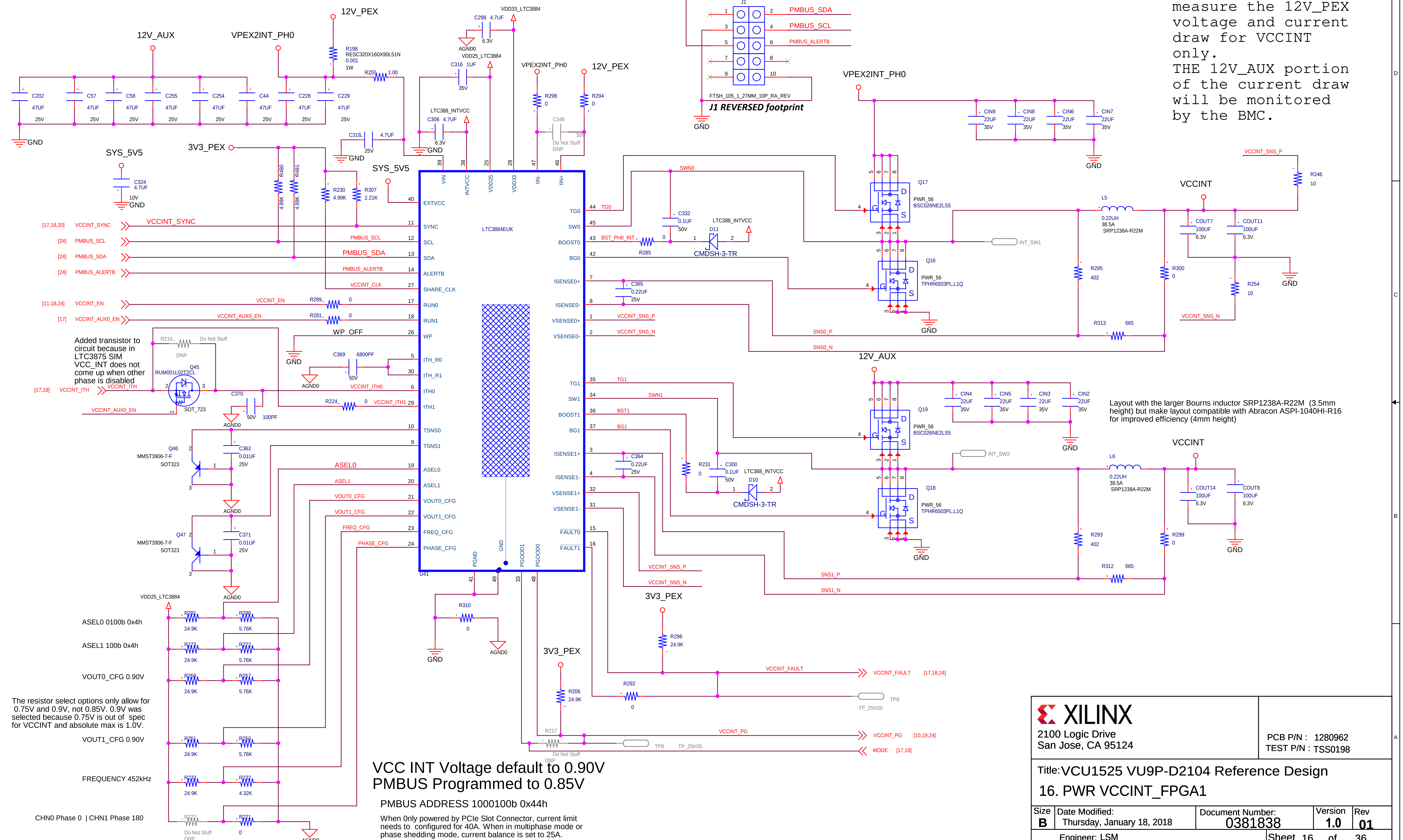
POWER SUPPLY VCCINT(1 of 3)



The LTC3884 is configured to measure the 12V_PEX voltage and current draw for VCCINT only.
THE 12V_AUX portion of the current draw will be monitored by the BMC.

Layout with the larger Bourns inductor SRP1238A-R22M (3.5mm height) but make layout compatible with Abracon ASPI-1040HI-R16 for improved efficiency (4mm height)

The resistor select options only allow for 0.75V and 0.9V, not 0.85V. 0.9V was selected because 0.75V is out of spec for VCCINT and absolute max is 1.0V.

VCC INT Voltage default to 0.90V
PMBUS Programmed to 0.85V

PMBUS ADDRESS 1000100b 0x44h

When 0nly powered by PCIe Slot Connector, current limit needs to configured for 40A. When in multiphase mode or phase shedding mode, current balance is set to 25A.

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Title: VCU1525 VU9P-D2104 Reference Design			
16. PWR VCCINT_FPGA1			
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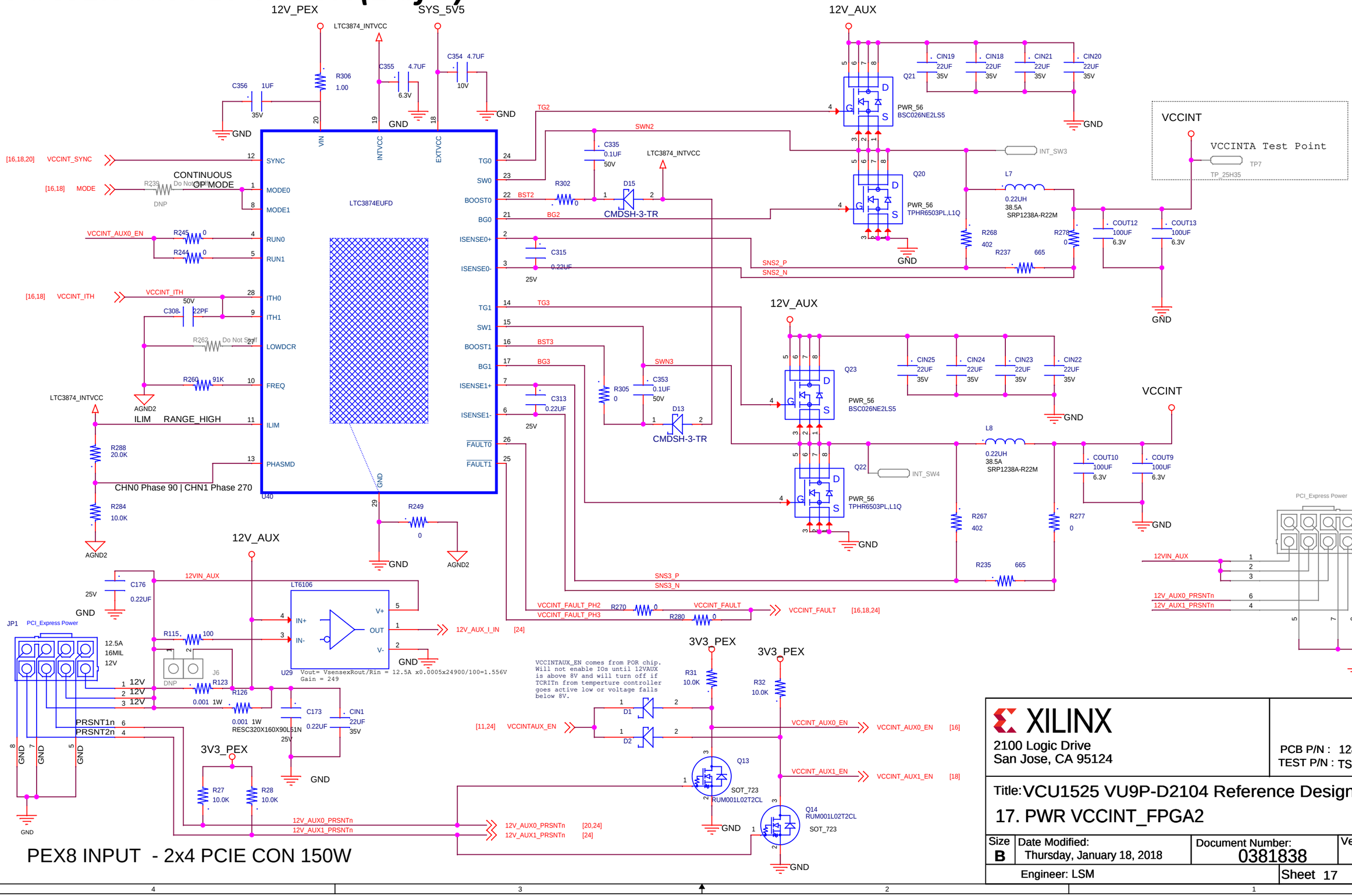
POWER SUPPLY VCCINT(2 of 3)



PEX8 INPUT - 2x4 PCIE CON 150W

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17. PWR VCCINT_FPGA2

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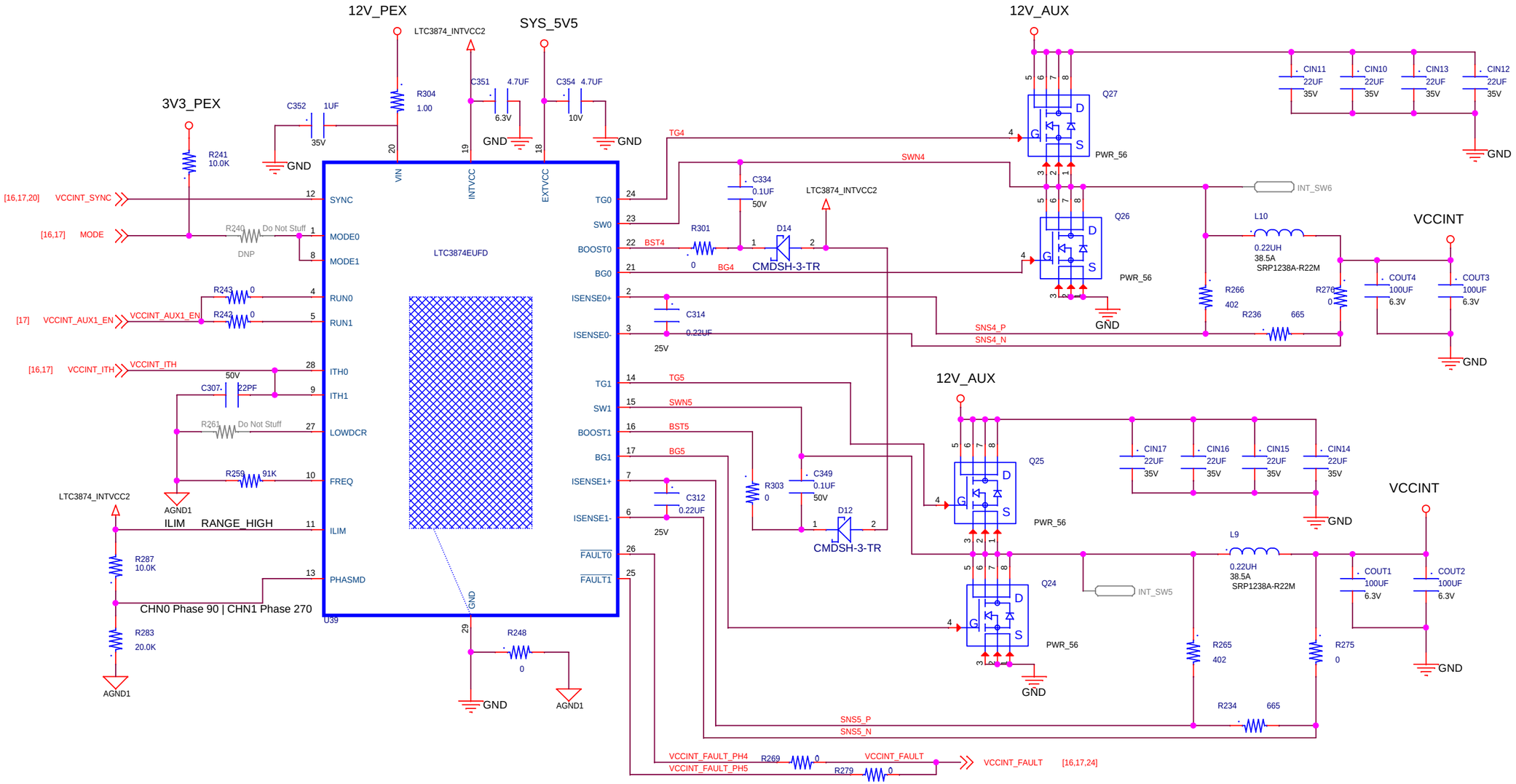
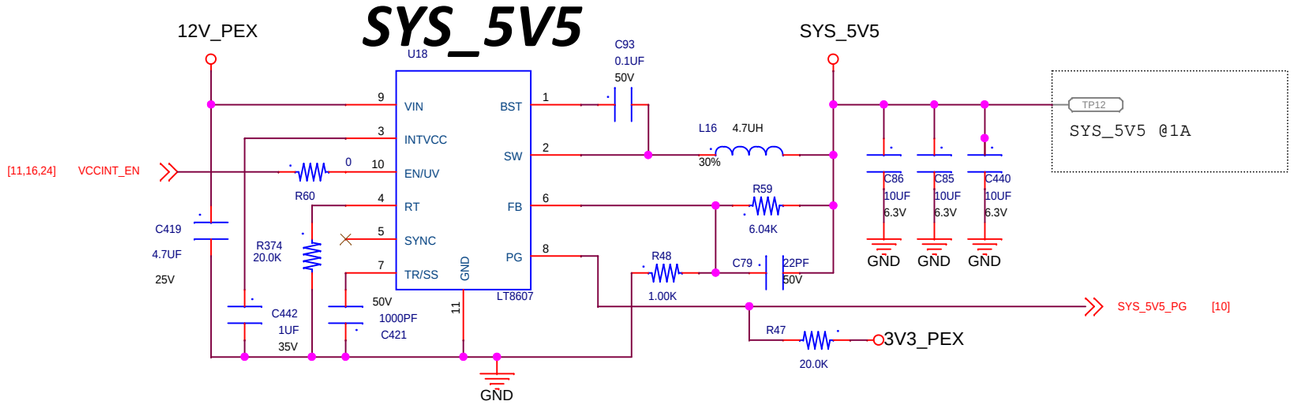
POWER SUPPLY VCCINT(3 of 3)





XILINX 2100 Logic Drive San Jose, CA 95124			PCB P/N : 1280962 TEST P/N : TSS0198
Title: VCU1525 VU9P-D2104 Reference Design 18. PWR VCCINT_FPGA3			
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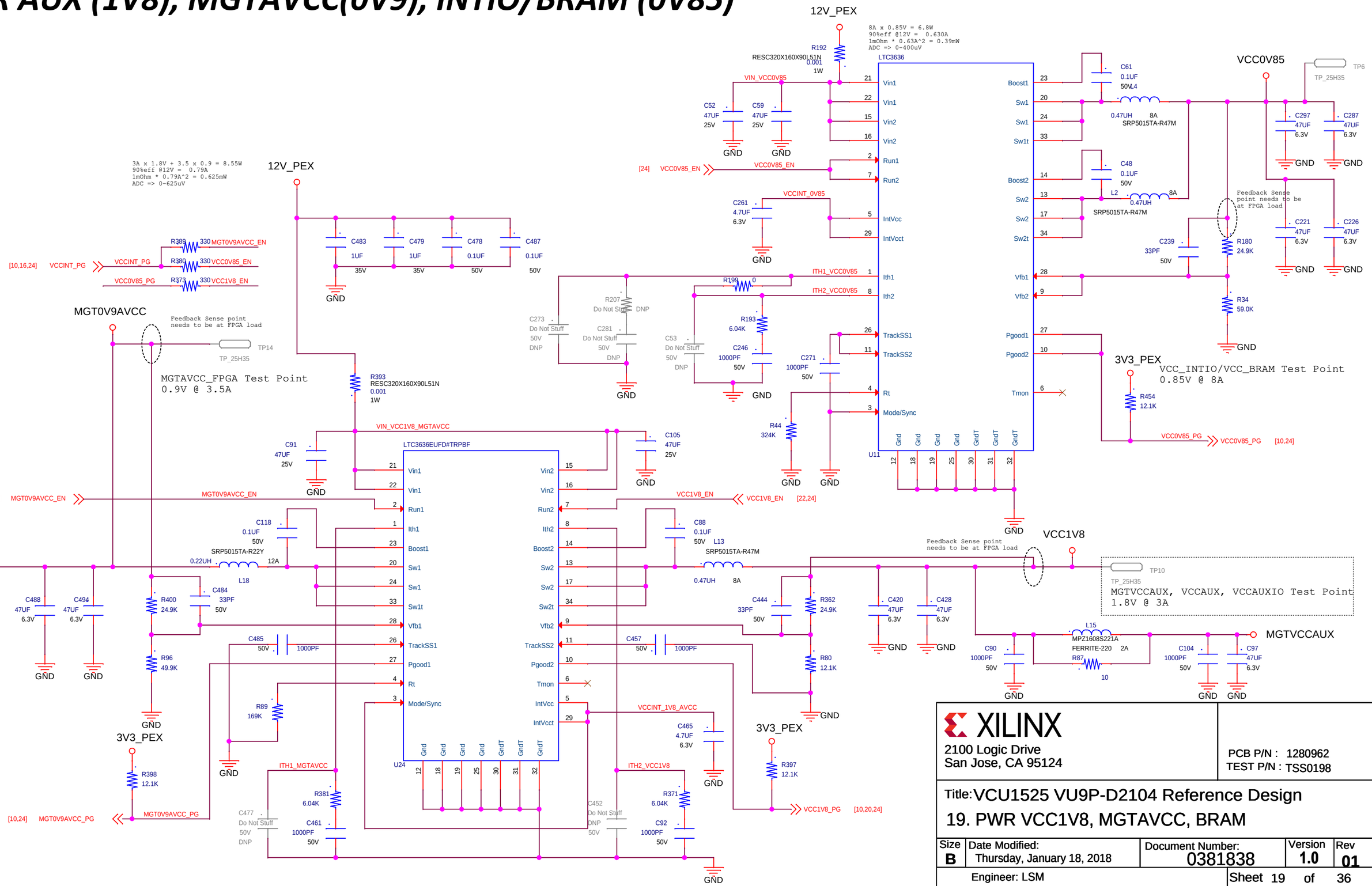
PWR AUX (1V8), MGTAVCC(0V9), INTIO/BRAM (0V85)



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Title: VCU1525 VU9P-D2104 Reference Design
19. PWR VCC1V8, MGTAVCC, BRAM

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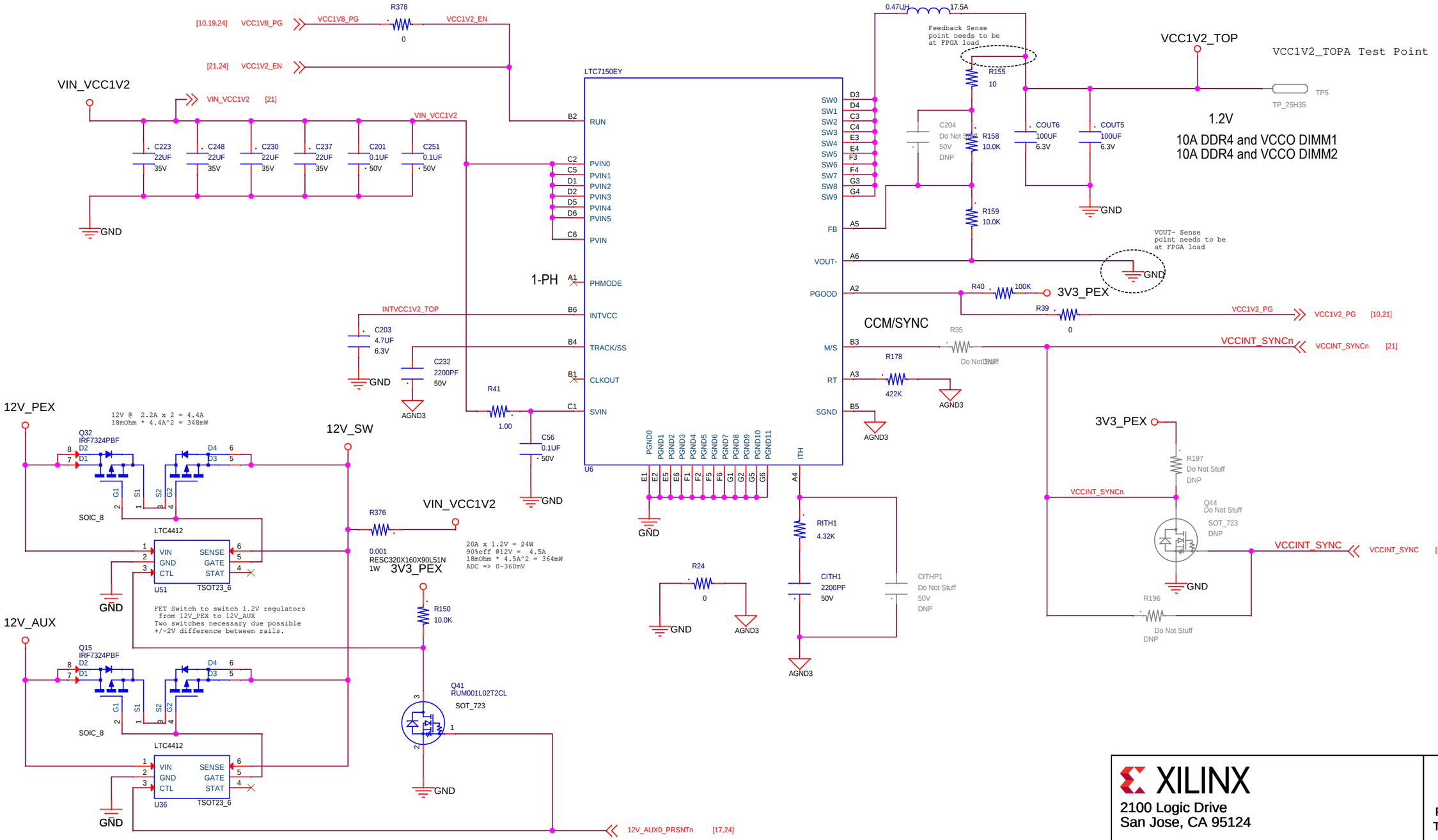
POWER SUPPLY VCC1V2_TOP



Switches 12V power from PEX connecter to AUX connector
when AUX connector present by grounding the CTRL pin (ON/OFF).

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Title: VCU1525 VU9P-D2104 Reference Design
20. PWR DDR VCC1V2_TOP

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POWER SUPPLY VCC1V2_BTM, MGTAVTT

20A x 1.2V = 24W
90%eff @12V = 2.22A
1mOhm * 2.22A^2 = 4.93mW
ADC => 0-5mV

[20,24] VCC1V2_EN → RUN (B2)

[20] VIN_VCC1V2 → PVIN0 (C2), PVIN1 (C5), PVIN2 (D1), PVIN3 (D2), PVIN4 (D5), PVIN5 (D6), PVIN (C6)

VIN_VCC1V2
C443 22UF 35V
C432 22UF 35V
C453 22UF 35V
C424 22UF 35V
C459 0.1UF 50V
C412 0.1UF 50V
GND

1-PH
PHMODE (A1)

INTVCC (B6)
C416 4.7UF 6.3V
C437 2200PF 50V
AGND4
GND

TRACK/SS (B4)

CLKOUT (B1)

SVIN (C1)
R91 1.00
C94 0.1UF 50V
GND

12V_PEX
20A x 1.2V = 24W
90%eff @12V = 2.22A
1mOhm * 2.22A^2 = 4.93mW
ADC => 0-5mV
R399 RESC320X160X90L51N 0.001 1W

LTC7150EY
U20
PGND0 PGND1 PGND2 PGND3 PGND4 PGND5 PGND6 PGND7 PGND8 PGND9 PGND10 PGND11
E1 E2 E5 E6 F1 F2 F5 F6 G1 G2 G5 G6
ITH (A4)

SW0 D3
SW1 D4
SW2 C3
SW3 C4
SW4 E3
SW5 E4
SW6 F3
SW7 F4
SW8 G3
SW9 G4

FB (A5)
VOUT- (A6)
PGOOD (A2)
M/S (B3)
RT (A3)
SGND (B5)

L14 0.47UH IHLP2525CZERR47M01 17.5A
R324 10
C417 Do Not Stuff 50V DNP
RFB1 10.0K
R335 10.0K
COUT16 100UF 6.3V
COUT15 100UF 6.3V
GND

VCC1V2_BTM
Feedback Sense point needs to be at FPGA load
TP11 TP_25H35
1.2V
10A DDR4 and VCCO DIMM1
10A DDR4 and VCCO DIMM2

VOUT- Sense point needs to be at FPGA load
GND

R86 0
VCC1V2_PG → VCC1V2_PG [10,20]

R81 DNP Do Not Stuff
R363 422K
VCCINT_SYNCn → VCCINT_SYNCn [20]

AGND4

CITHP2 Do Not Stuff 50V DNP
RITH2 4.32K
CITH2 2200PF 50V
AGND4

R49 0
GND
AGND4

LTC3636EUFD#TRPBF
U25
Vin1 (21)
Vin1 (22)
Vin2 (15)
Vin2 (16)
Run1 (2)
Run2 (7)
IntVcc (5)
IntVcct (29)
Ith1 (1)
Ith2 (8)
TrackSS1 (26)
TrackSS2 (11)
Rt (4)
Mode/Sync (3)
Gnd (12) Gnd (18) Gnd (19) Gnd (25) GndT (30) GndT (31) GndT (32)

Boost1 (23)
Sw1 (20)
Sw1 (24)
Sw1t (33)
Boost2 (14)
Sw2 (13)
Sw2 (17)
Sw2t (34)
Vfb1 (28)
Vfb2 (9)
Pgood1 (27)
Pgood2 (10)
Tmon (6)

VIN_MGTAVTT
C121 47UF 25V
C122 47UF 25V
GND

VCC1V2_EN

VCCINT_AVTT
C501 4.7UF 6.3V
GND

ITH1_MGTAVTT
R418 0
ITH2_MGTAVTT
R419 Do Not Stuff DNP
C502 Do Not Stuff DNP 50V
C510 Do Not Stuff 50V DNP
C141 Do Not Stuff DNP 50V
R417 6.04K
C512 1000PF 50V
C498 1000PF 50V
R100 324K

C129 0.1UF 50V
L20 0.47UH 8A SRP5015TA-R47M
C130 0.1UF 50V
SRP5015TA-R47M L19 0.47UH 8A

MGTAVTT
MGTAVTT => 1.2V at 8A
C147 47UF 6.3V
C142 47UF 6.3V
C144 47UF 6.3V
C143 47UF 6.3V
GND

Feedback Sense point needs to be at FPGA load
TP17 TP_25H35
MGTAVTT_FPGA Test Point

C503 33PF 50V
R415 24.9K
R405 24.9K
3V3_PEX
R97 100K
MGTAVTT_PG [10]

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TEST P/N : TSS0198

Title: VCU1525 VU9P-D2104 Reference Design
21. PWR DDR VCC1V2_BTM, MGTAVTT

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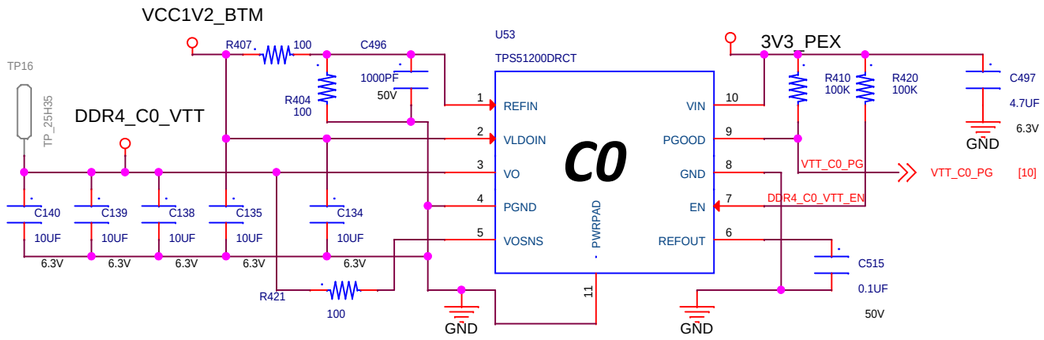
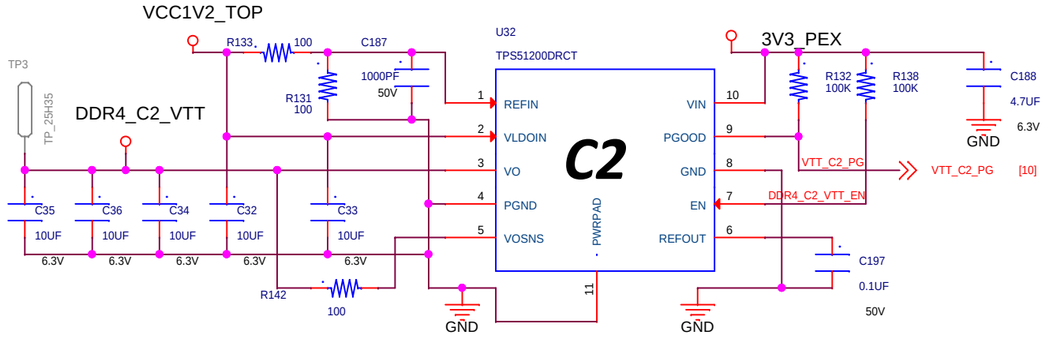
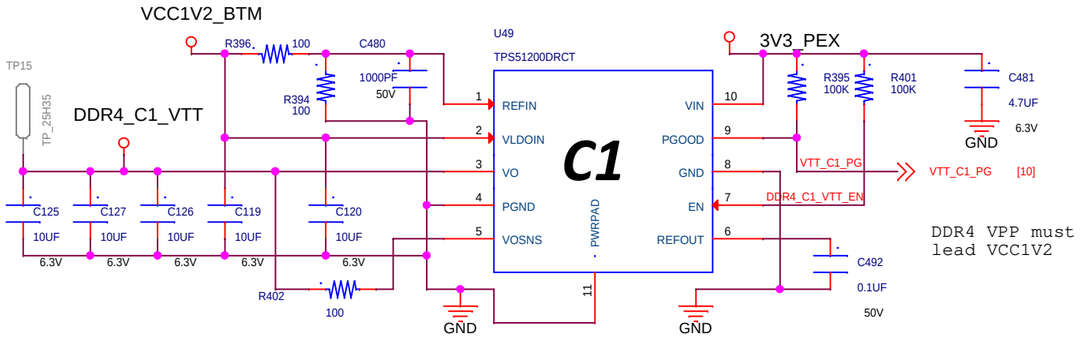
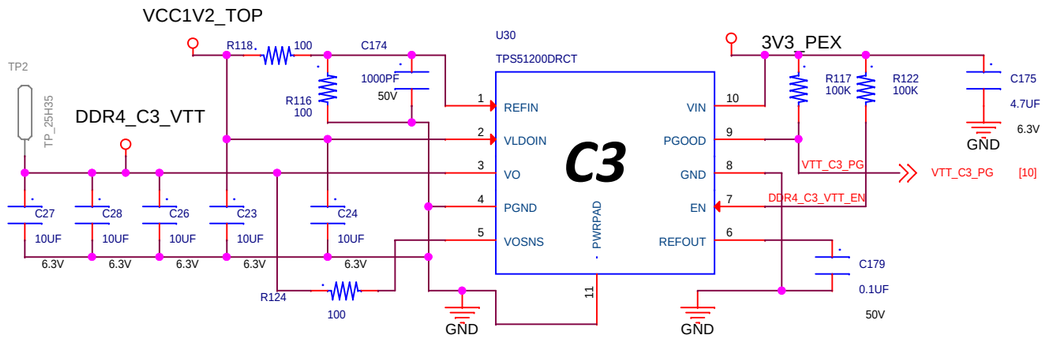
PWR DDR4_C0 - C3 VTT & VPP RAILS



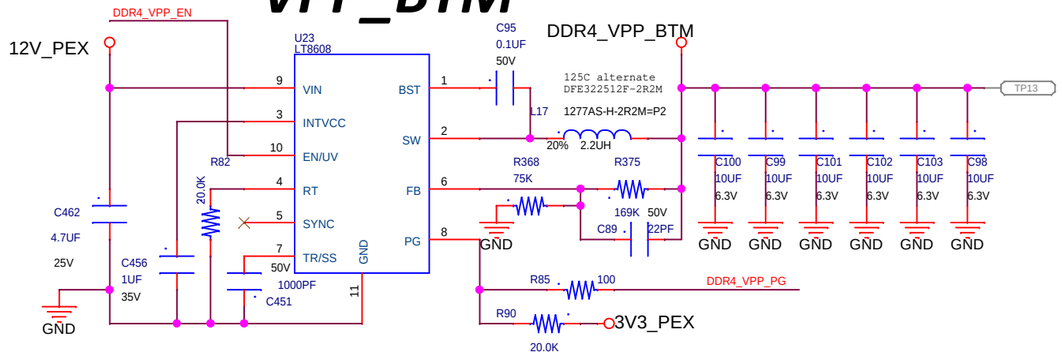




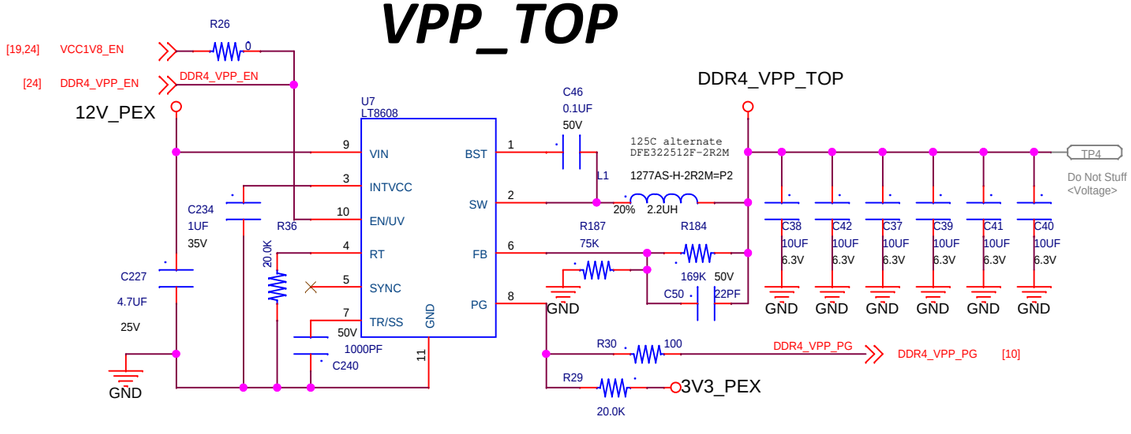
DDR4 VPP must lead VCC1V2



VPP_BTM



VPP_TOP



XILINX 2100 Logic Drive San Jose, CA 95124			PCB P/N : 1280962 TEST P/N : TSS0198
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