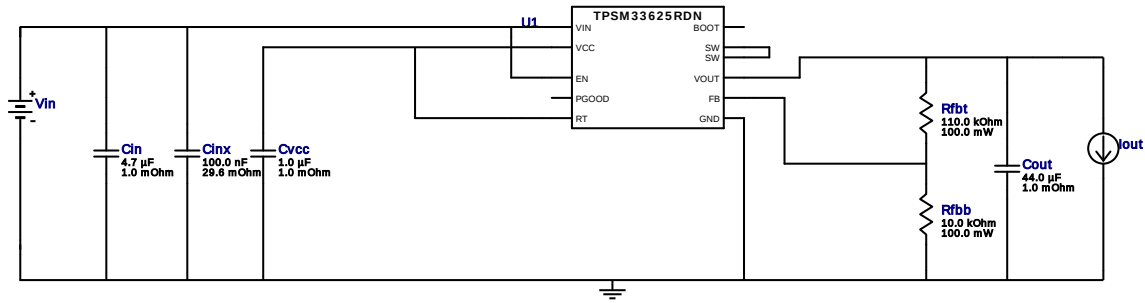


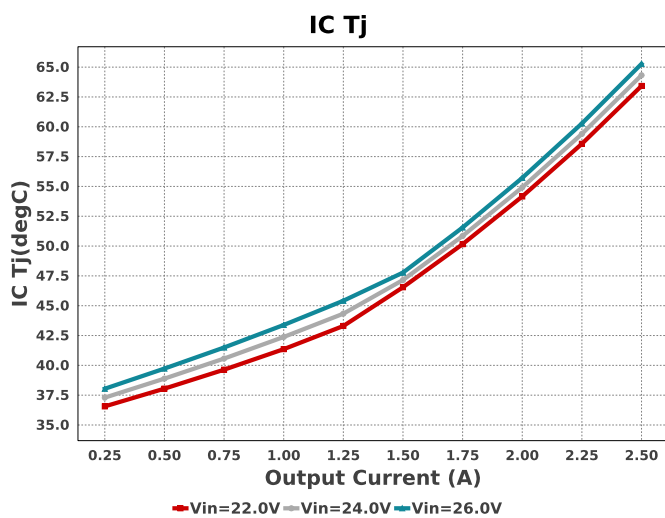
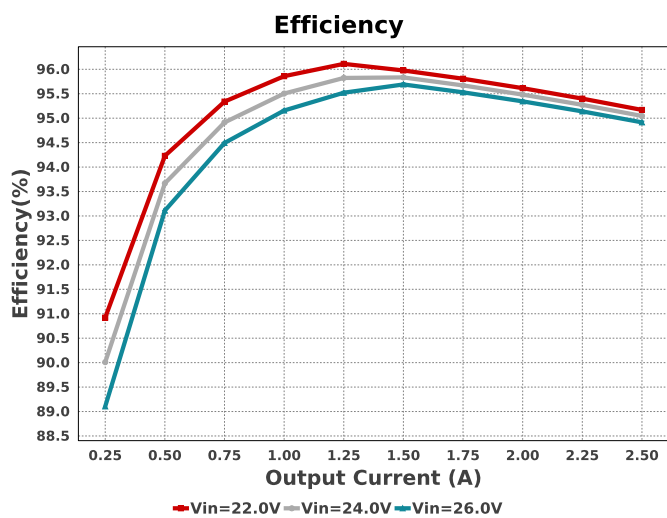
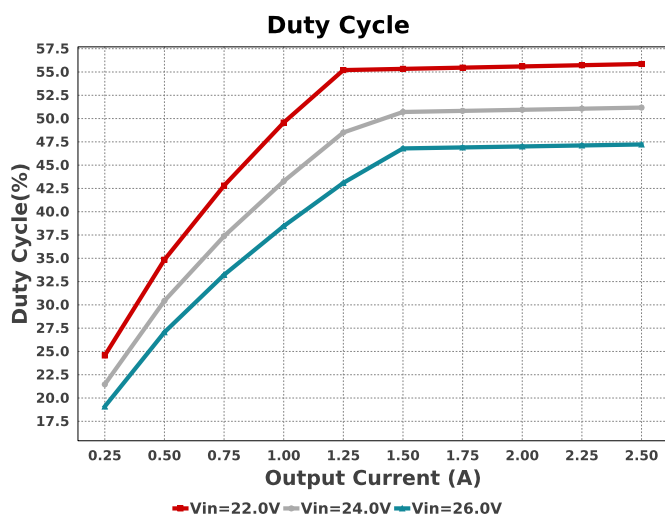
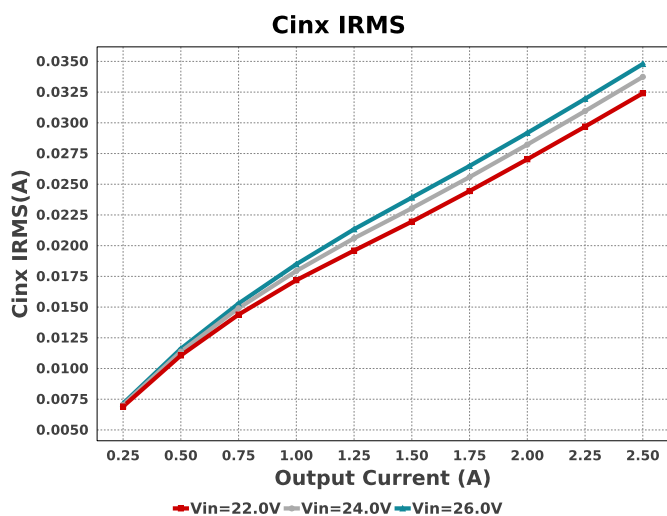
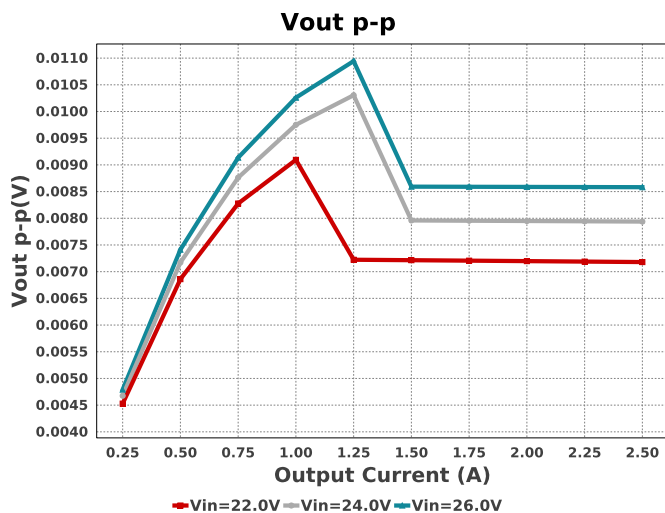
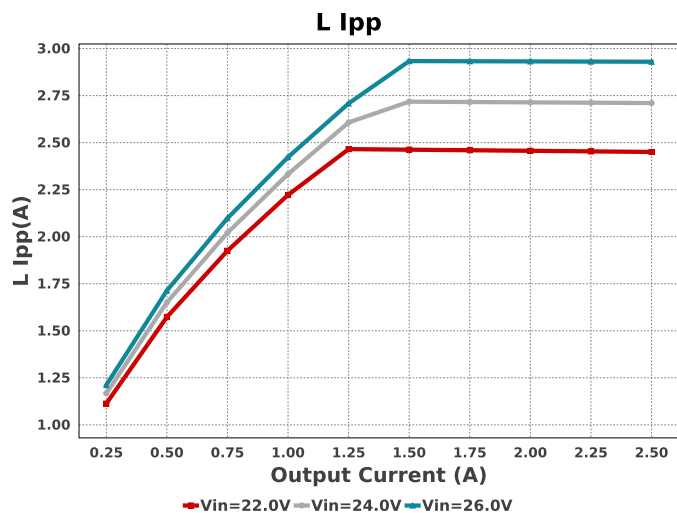
WEBENCH® Design Report

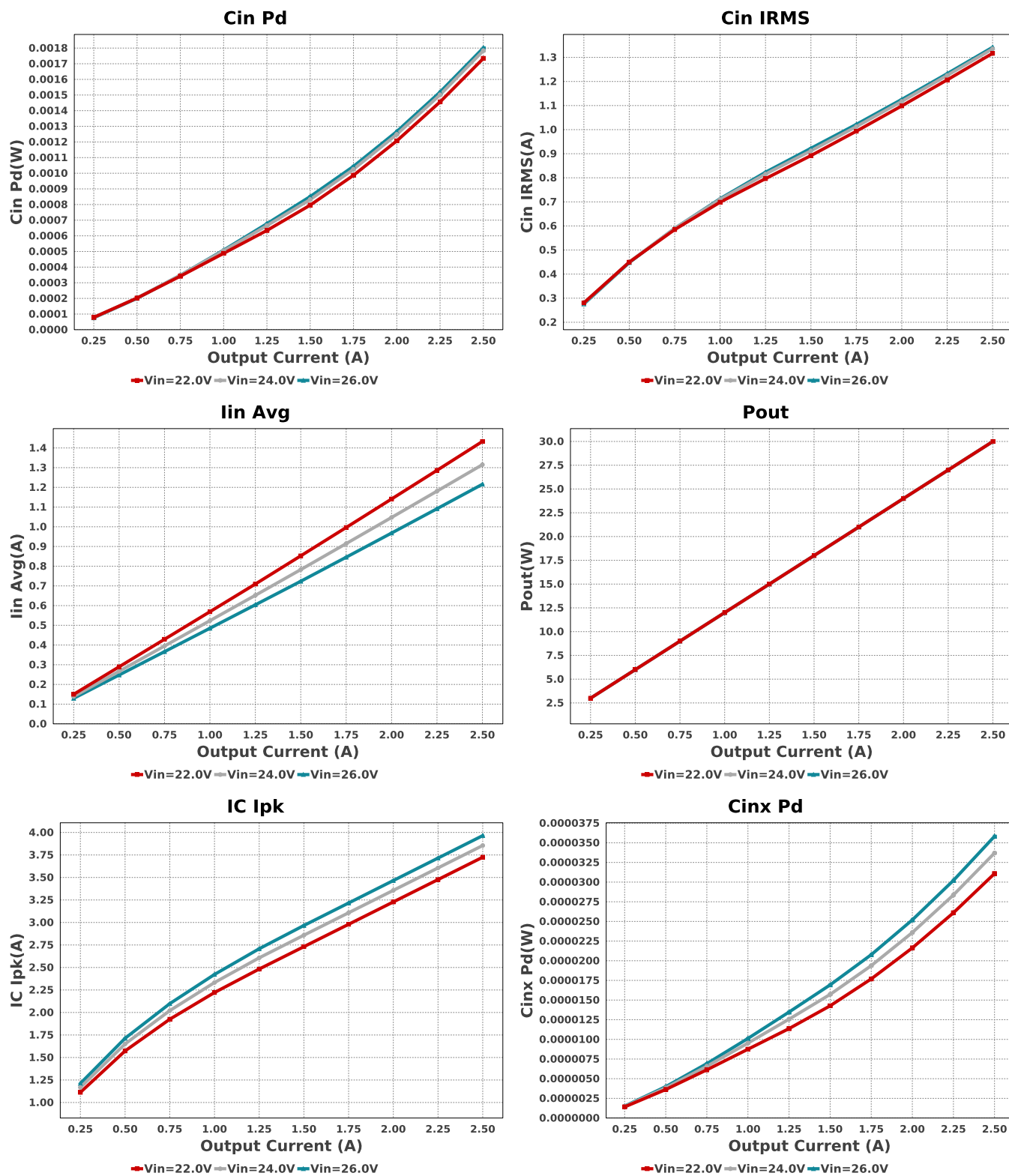
Design : 176 TPSM33625RDNR
TPSM33625RDNR 22V-26V to 12.00V @ 2.5A

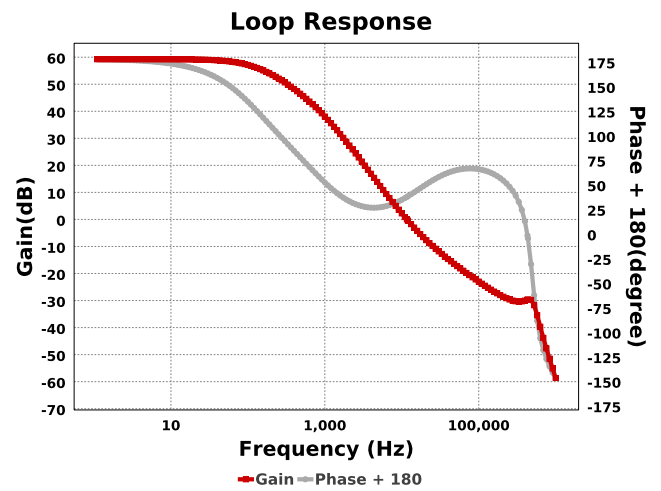
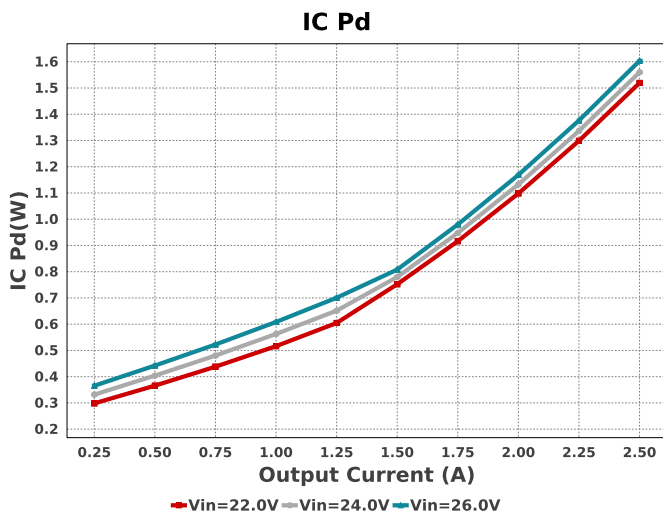
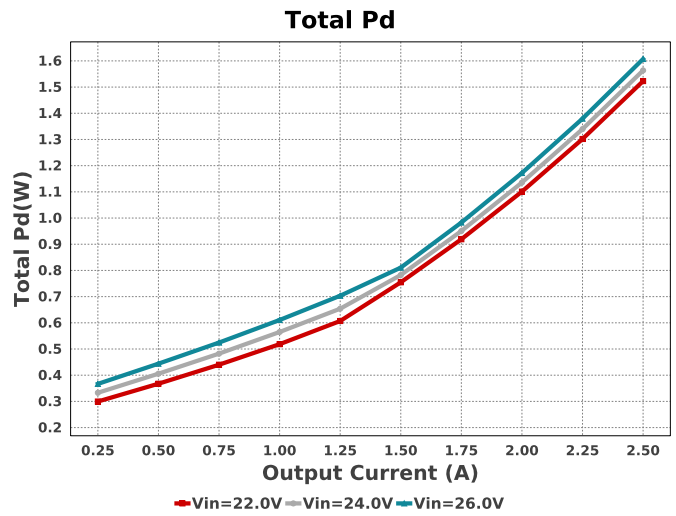
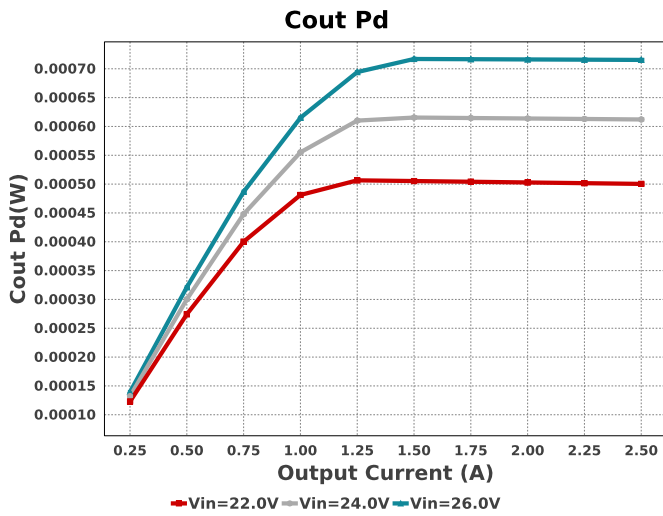
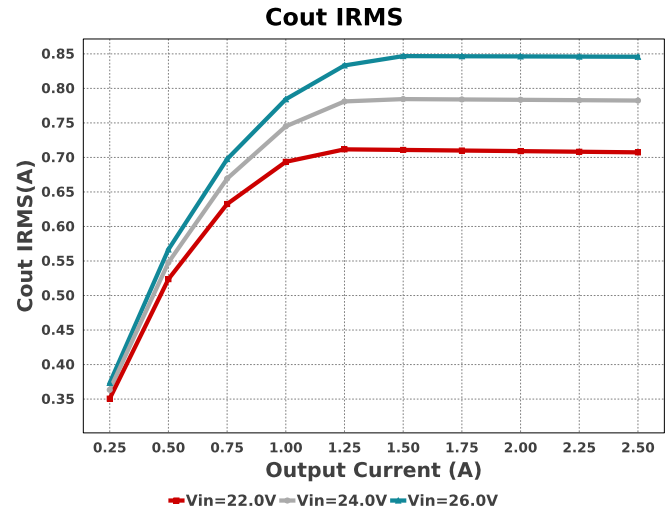
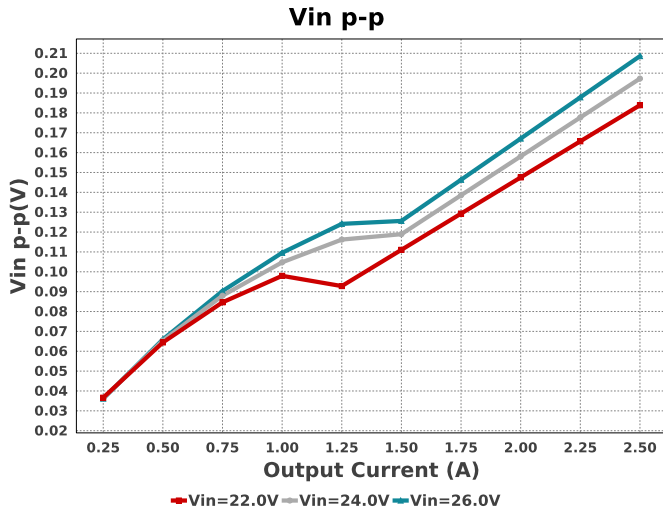


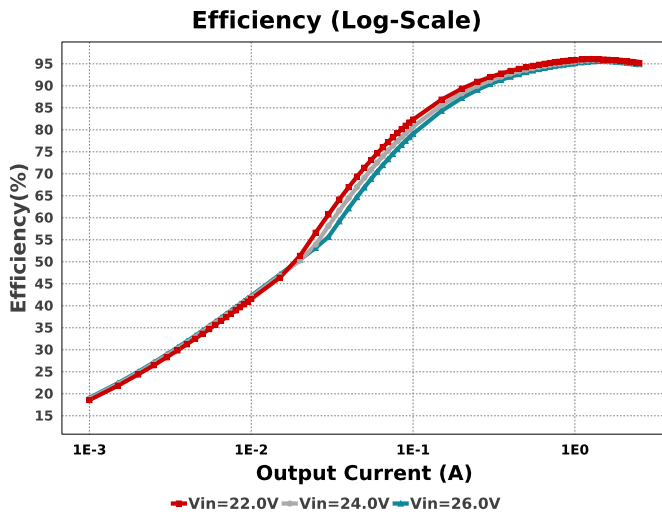
Electrical BOM

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cin	MuRata	GRM32ER71H475KA88L Series= X7R	Cap= 4.7 uF ESR= 1.0 mOhm VDC= 50.0 V IRMS= 6.0 A	1	\$0.16	1210 15 mm ²
Cinx	TDK	CGA3E2X7R1H104K080AA Series= X7R	Cap= 100.0 nF ESR= 29.6 mOhm VDC= 50.0 V IRMS= 971.99 mA	1	\$0.01	0603 5 mm ²
Cout	CUSTOM	CUSTOM Series= ?	Cap= 44.0 uF ESR= 1.0 mOhm VDC= 18.0 V IRMS= 1.57078 A	1	NA	CUSTOM 0 mm ²
Cvcc	Taiyo Yuden	EMK107B7105KA-T Series= X7R	Cap= 1.0 uF ESR= 1.0 mOhm VDC= 16.0 V IRMS= 0.0 A	1	\$0.01	0603 5 mm ²
Rfbb	Yageo	RC0603FR-0710KL Series= ?	Res= 10.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm ²
Rfbb	Yageo	RC0603FR-07110KL Series= ?	Res= 110.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm ²
U1	Texas Instruments	TPSM33625RDNR	Switcher	1	\$1.40	RPE0009A 9 mm ²









Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	1.342 A	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	1.801 mW	Capacitor	Input capacitor power dissipation
3.	Cinx IRMS	34.789 mA	Capacitor	Bulk capacitor RMS ripple current
4.	Cinx Pd	35.824 μ W	Capacitor	Bulk capacitor power dissipation
5.	Cout IRMS	845.804 mA	Capacitor	Output capacitor RMS ripple current
6.	Cout Pd	715.38 μ W	Capacitor	Output capacitor power dissipation
7.	IC Ipk	3.965 A	IC	Peak switch current in IC
8.	IC Pd	1.603 W	IC	IC power dissipation
9.	IC Tj	65.274 degC	IC	IC junction temperature
10.	IC Tolerance	12.5 mV	IC	IC Feedback Tolerance
11.	ICThetaJA Effective	22.0 degC/W	IC	Effective IC Junction-to-Ambient Thermal Resistance
12.	Iin Avg	1.216 A	IC	Average input current
13.	Cin Pd	1.801 mW	Power	Input capacitor power dissipation
14.	Cinx Pd	35.824 μ W	Power	Bulk capacitor power dissipation
15.	Cout Pd	715.38 μ W	Power	Output capacitor power dissipation
16.	IC Pd	1.603 W	Power	IC power dissipation
17.	Total Pd	1.607 W	Power	Total Power Dissipation
18.	BOM Count	7	System	Total Design BOM count
19.	Cross Freq	11.666 kHz	System	Bode plot crossover frequency
20.	Duty Cycle	47.221 %	System	Duty cycle
21.	Efficiency	94.915 %	System	Steady state efficiency
22.	FootPrint	82.0 mm ²	System	Total Foot Print Area of BOM components
23.	Frequency	1000.0 kHz	System	Switching frequency
24.	Gain Marg	-29.668 dB	System	Bode Plot Gain Margin
25.	Iout	2.5 A	System	Iout operating point
26.	L Ipp	2.93 A	System	Peak-to-peak inductor ripple current
27.	Low Freq Gain	59.259 dB	System	Gain at 1Hz
28.	Mode	CCM	System	Conduction Mode
29.	Phase Marg	39.339 deg	System	Bode Plot Phase Margin
30.	Pout	30.0 W	System	Total output power
31.	Total BOM	NA	System	Total BOM Cost
32.	Vin	26.0 V	System	Vin operating point
33.	Vin p-p	208.587 mV	System	Peak-to-peak input voltage
34.	Vout	12.0 V	System	Operational Output Voltage

#	Name	Value	Category	Description
35.	Vout Actual	12.0 V	System Information	Vout Actual calculated based on selected voltage divider resistors
36.	Vout Tolerance	3.125 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
37.	Vout p-p	8.582 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	2.5	Maximum Output Current
VinMax	26.0	Maximum input voltage
VinMin	22.0	Minimum input voltage
Vout	12.0	Output Voltage
base_pn	TPSM33625	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature
UserFsw	1000.0 k	Customer Selected Frequency

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of C_{in} and C_{out} , and the inductance and DC resistance of $L1$ before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

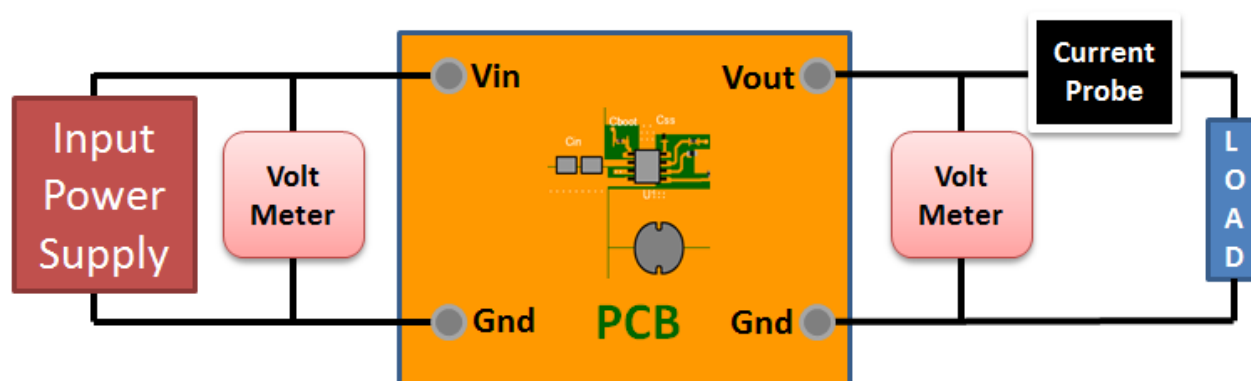
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab down to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 22.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to V_{in} and GND. Connect a digital volt meter and a load if needed to set the minimum load of the design from V_{out} and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between V_{in} and GND, a load is connected between V_{out} and GND and a current meter is connected in series between V_{out} and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

1. Master key : F20DB821062544F1[v1]
2. **TPSM33625** Product Folder : <http://www.ti.com/product/TPSM33625> : contains the data sheet and other resources.

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