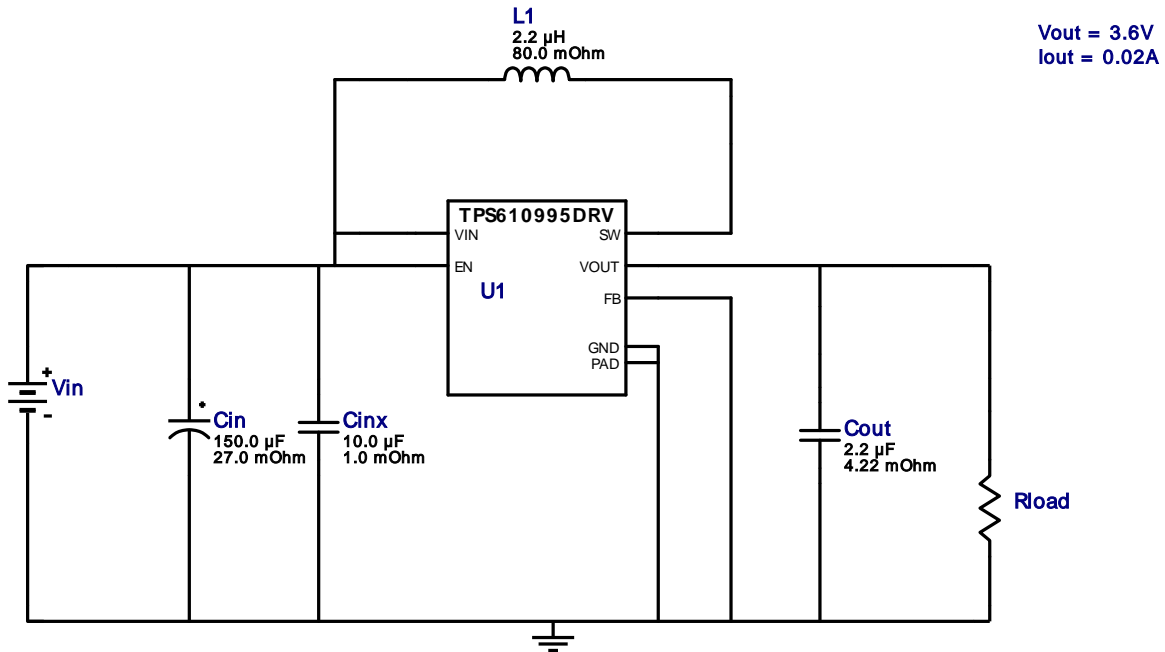
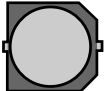






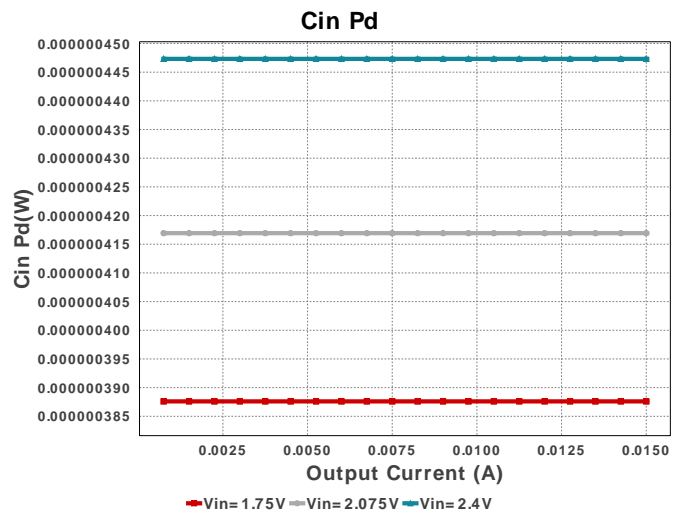
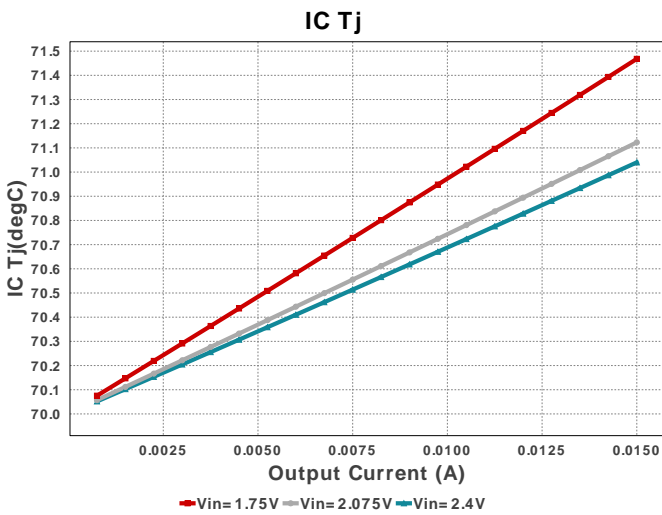
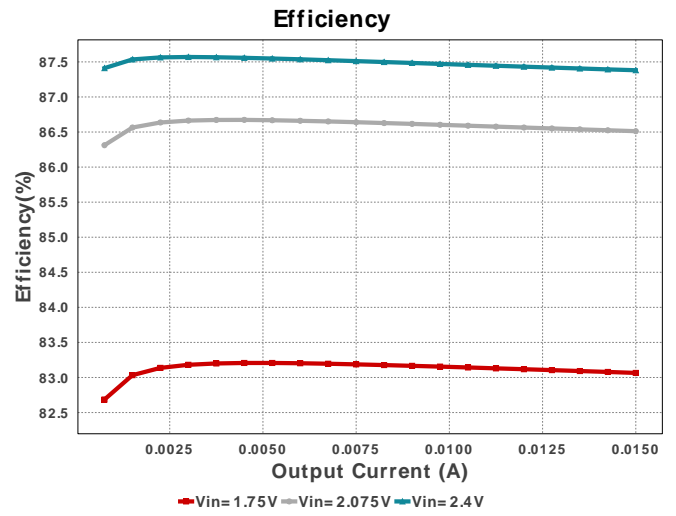
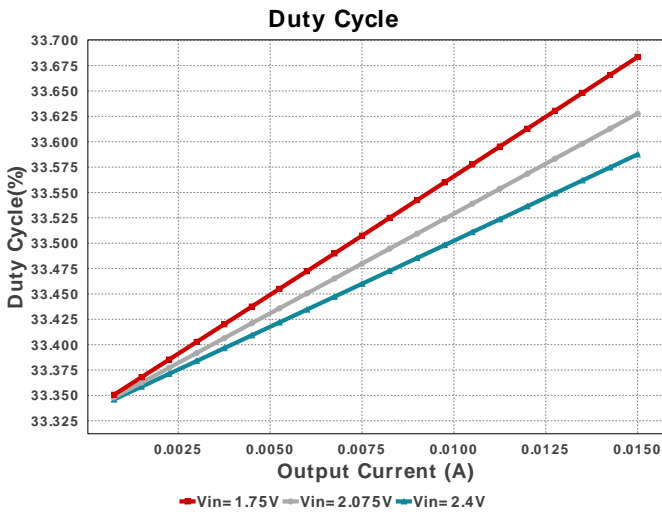
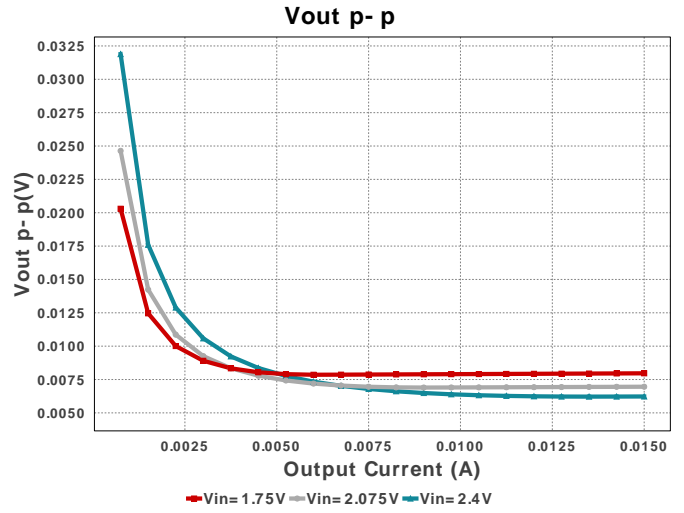
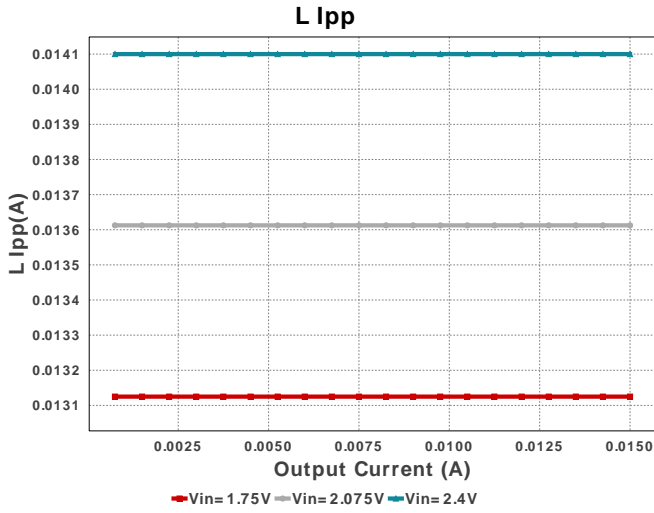
**WEBENCH® Design Report**

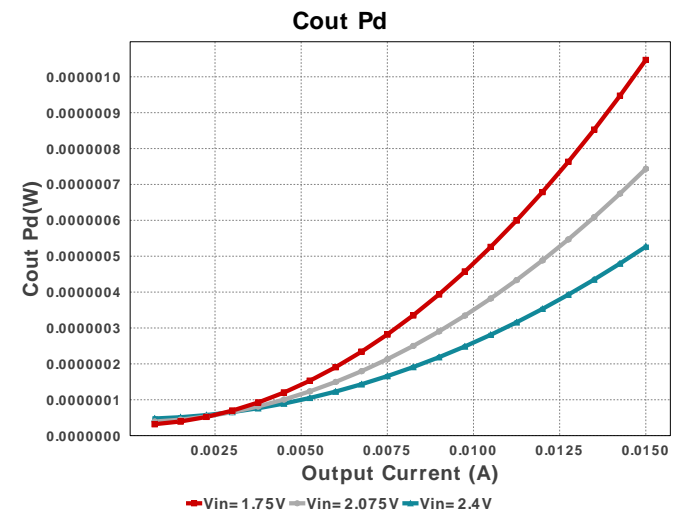
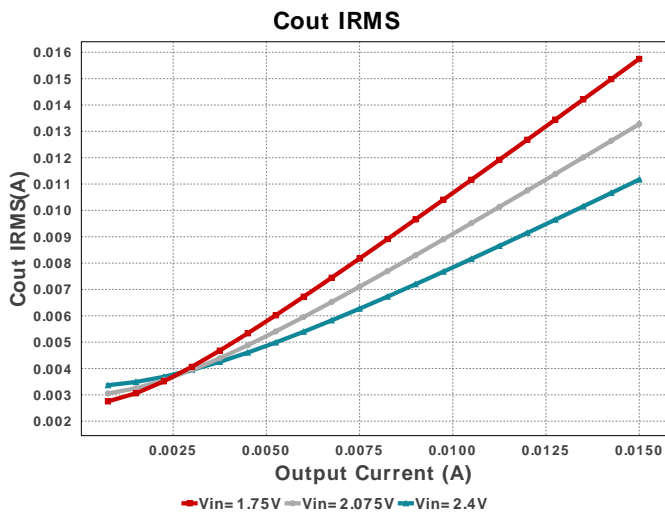
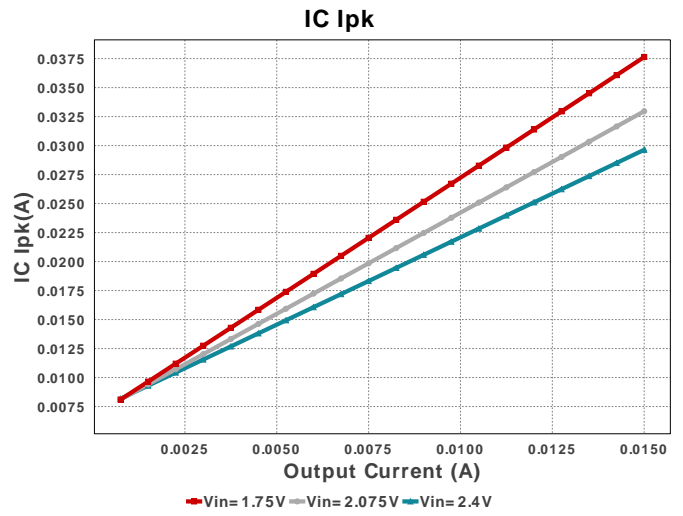
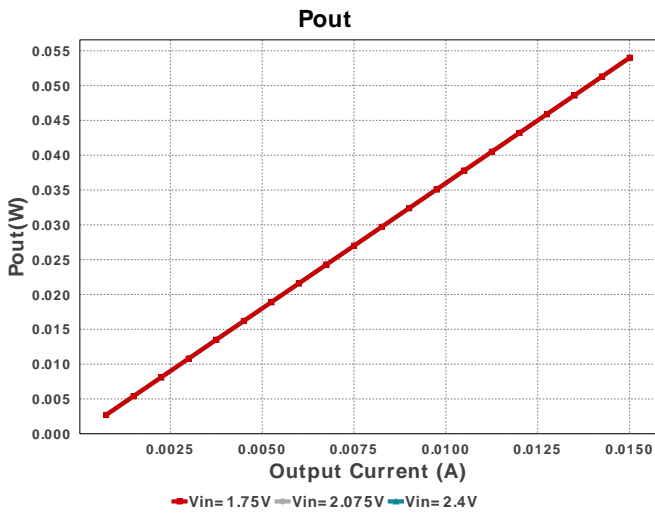
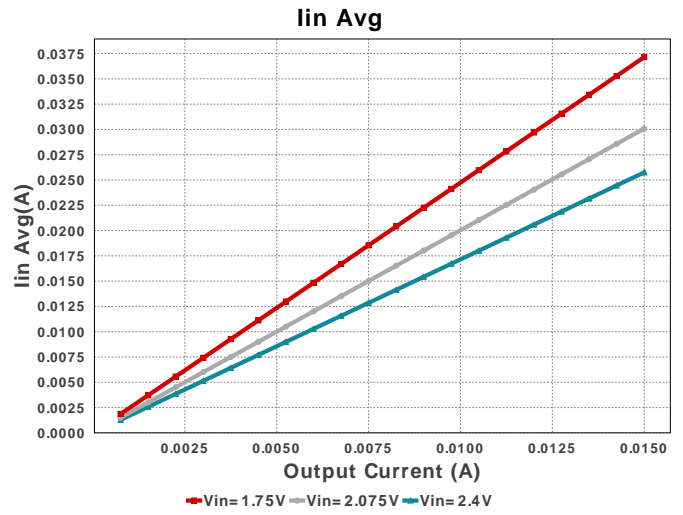
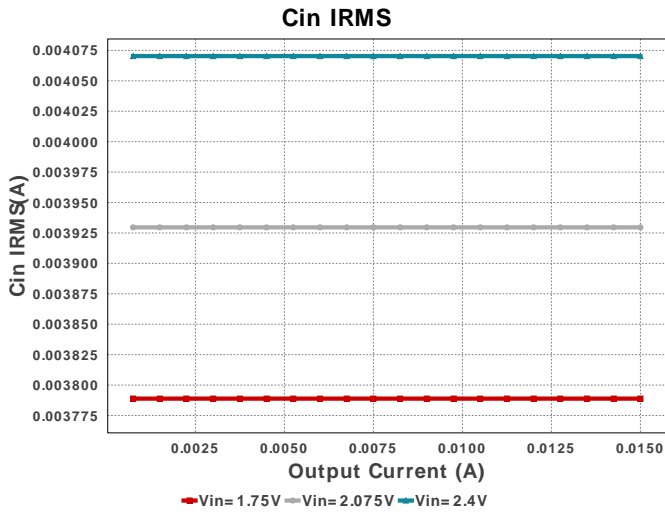
 Design : 296 TPS610995DRV  
 TPS610995DRV 1.8V-2.3V to 3.60V @ 0.05A

**Design Alerts**
**Component Selection Information**

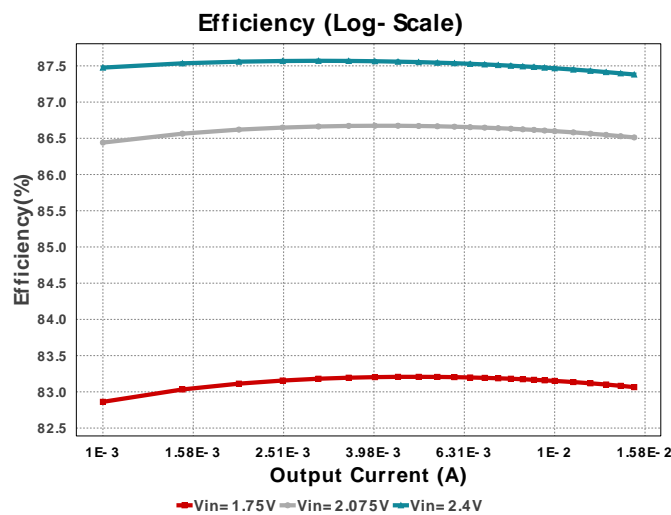
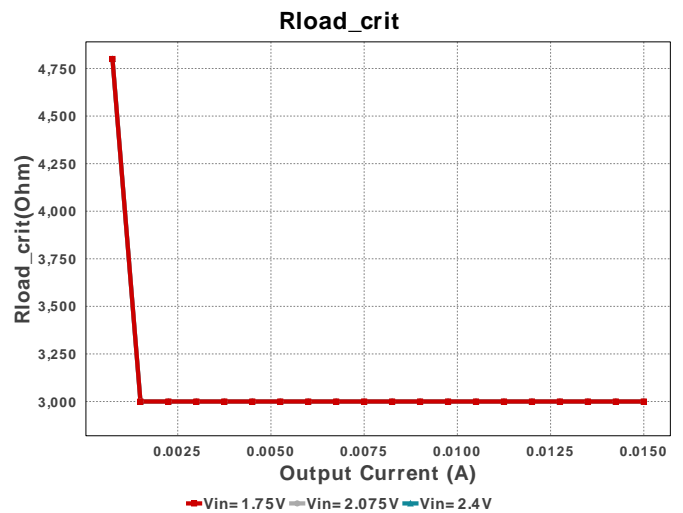
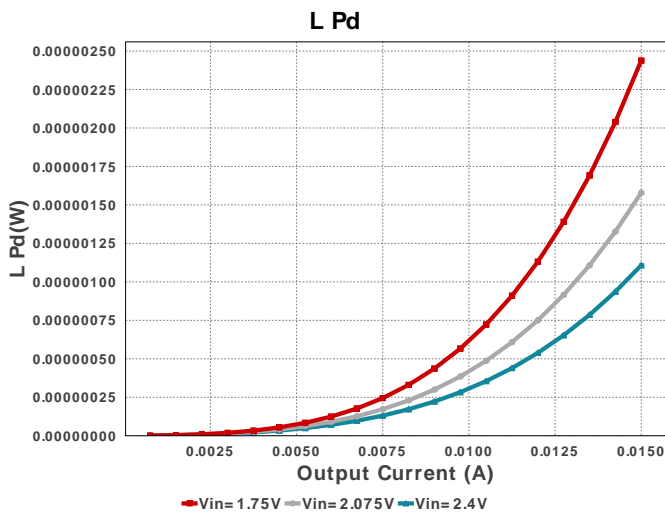
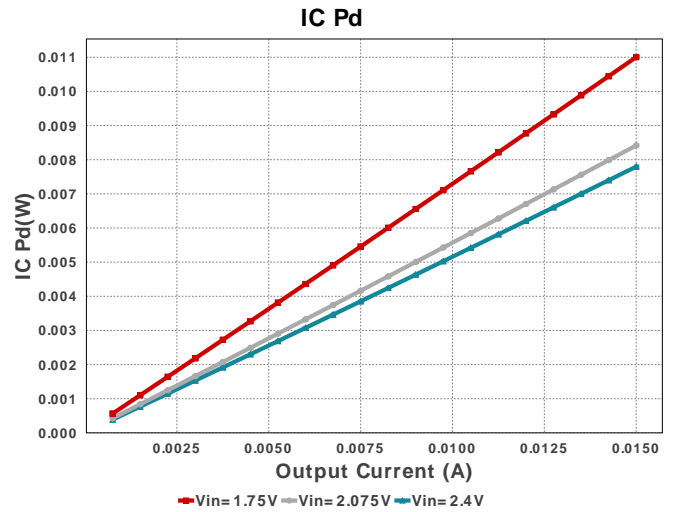
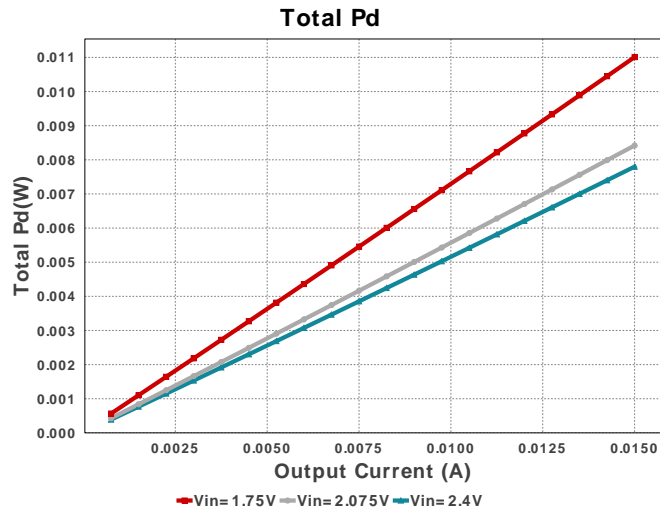
TPS610995-DRV can support VIN higher than VOUT but this behaviour is not modeled in WEBENCH.

**Electrical BOM**

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cin	Panasonic	EEHZC1V151P Series= ZC	Cap= 150.0 uF ESR= 27.0 mOhm VDC= 35.0 V IRMS= 1.6 A	1	\$2.59	 SM_RADIAL_8MM 113 mm <sup>2</sup>
Cinx	MuRata	GRM155R60G106ME44D Series= X5R	Cap= 10.0 uF ESR= 1.0 mOhm VDC= 4.0 V IRMS= 6.0 A	1	\$0.03	 0402_070 3 mm <sup>2</sup>
Cout	MuRata	GRM21BR71C225KA12L Series= X7R	Cap= 2.2 uF ESR= 4.22 mOhm VDC= 16.0 V IRMS= 1.94677 A	1	\$0.08	 0805 7 mm <sup>2</sup>
L1	MuRata	LQM2HPN2R2MG0L	L= 2.2 uH 80.0 mOhm	1	\$0.12	 1008 10 mm <sup>2</sup>
U1	Texas Instruments	TPS610995DRV	Switcher	1	\$0.58	 DRV0006A 9 mm <sup>2</sup>







### Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	3.789 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	387.6 nW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	15.751 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	1.047 μW	Capacitor	Output capacitor power dissipation
5.	IC Ipk	37.64 mA	IC	Peak switch current in IC
6.	IC Pd	11.005 mW	IC	IC power dissipation
7.	IC Tj	71.468 degC	IC	IC junction temperature
8.	IC Tolerance	40.0 mV	IC	IC Feedback Tolerance
9.	ICThetaJA	133.4 degC/W	IC	IC junction-to-ambient thermal resistance
10.	Iin Avg	37.148 mA	IC	Average input current
11.	L Ipp	13.125 mA	Inductor	Peak-to-peak inductor ripple current

#	Name	Value	Category	Description
12.	L Pd	2.438 $\mu$ W	Inductor	Inductor power dissipation
13.	Cin Pd	387.6 nW	Power	Input capacitor power dissipation
14.	Cout Pd	1.047 $\mu$ W	Power	Output capacitor power dissipation
15.	IC Pd	11.005 mW	Power	IC power dissipation
16.	L Pd	2.438 $\mu$ W	Power	Inductor power dissipation
17.	Total Pd	11.009 mW	Power	Total Power Dissipation
18.	BOM Count	5	System Information	Total Design BOM count
19.	Duty Cycle	33.684 %	System Information	Duty cycle
20.	Efficiency	83.065 %	System Information	Steady state efficiency
21.	FootPrint	143.0 mm <sup>2</sup>	System Information	Total Foot Print Area of BOM components
22.	Frequency	467.172 kHz	System Information	Switching frequency
23.	Iout	15.0 mA	System Information	Iout operating point
24.	Mode	DCM	System Information	Conduction Mode
25.	Pout	54.0 mW	System Information	Total output power
26.	Rload_crit	3.0 kOhm	System Information	Minimum Rload required during Start up
27.	Total BOM	\$3.4	System Information	Total BOM Cost
28.	Vin	1.75 V	System Information	Vin operating point
29.	Vout	3.6 V	System Information	Operational Output Voltage
30.	Vout Tolerance	1.111 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
31.	Vout p-p	7.965 mV	System Information	Peak-to-peak output ripple voltage

## Design Inputs

Name	Value	Description
Iout	15.0 m	Maximum Output Current
VinMax	2.4	Maximum input voltage
VinMin	1.75	Minimum input voltage
Vout	3.6	Output Voltage
base_pn	TPS610995-DRV	Base Product Number
source	DC	Input Source Type
Ta	70.0	Ambient temperature

## WEBENCH® Assembly

### Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of  $C_{in}$  and  $C_{out}$ , and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

### Soldering Component to Board

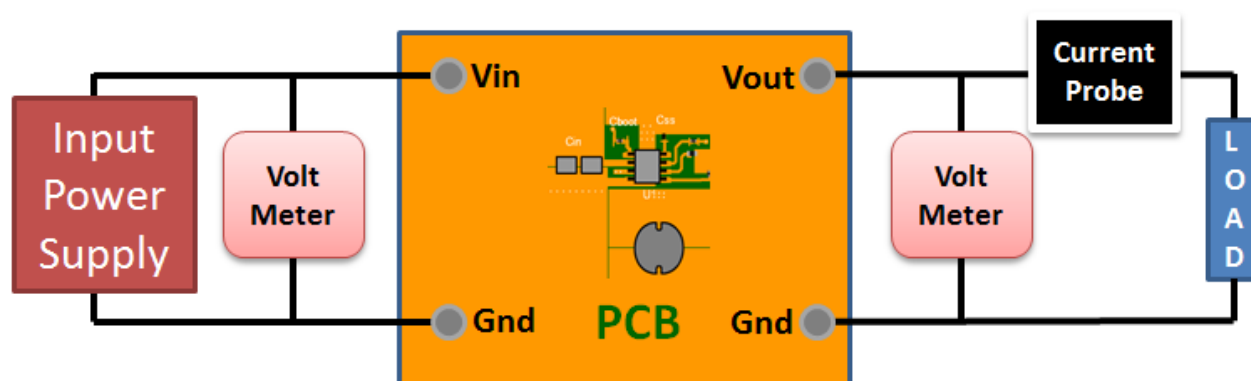
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab down to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

### Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 1.75V and set the input supply's current limit to zero. With the input supply off connect up the input supply to  $V_{in}$  and GND. Connect a digital volt meter and a load if needed to set the minimum load of the design from  $V_{out}$  and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

### Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between  $V_{in}$  and GND, a load is connected between  $V_{out}$  and GND and a current meter is connected in series between  $V_{out}$  and the load. The load must be able to handle at least rated output power + 50% ( 7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



### Design Assistance

1. Master key : B2CA6B61370DF259[v1]
2. **TPS61095-DRV** Product Folder : <http://www.ti.com/product/TPS61099> : contains the data sheet and other resources.

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