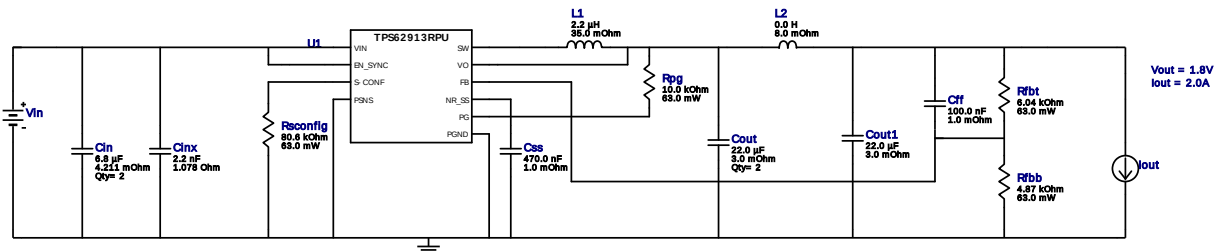


WEBENCH® Design Report

Design : 788 TPS62913RPUR
TPS62913RPUR 12V-12V to 1.80V @ 2A



Design Alerts

TPS62913 Design

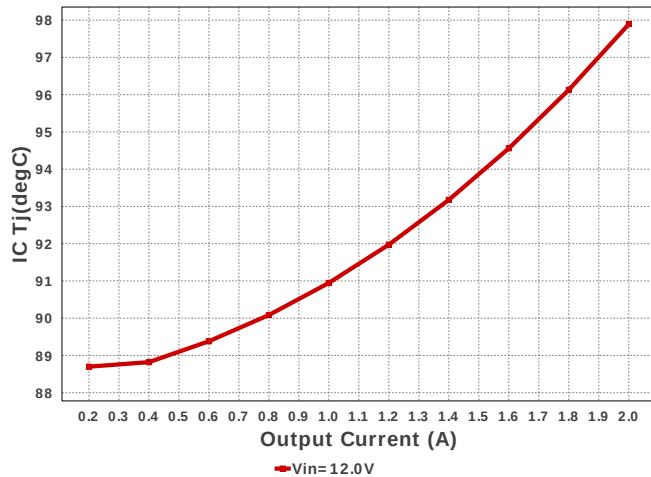
The TPS62913 supports a second LC ferrite bead output filter to achieve lowest output voltage ripple. To enable this filter in the design, use the Second Stage Output Filter dropdown option from Advanced options on the left side. Please refer to the TPS62913 datasheet for more information.

Electrical BOM

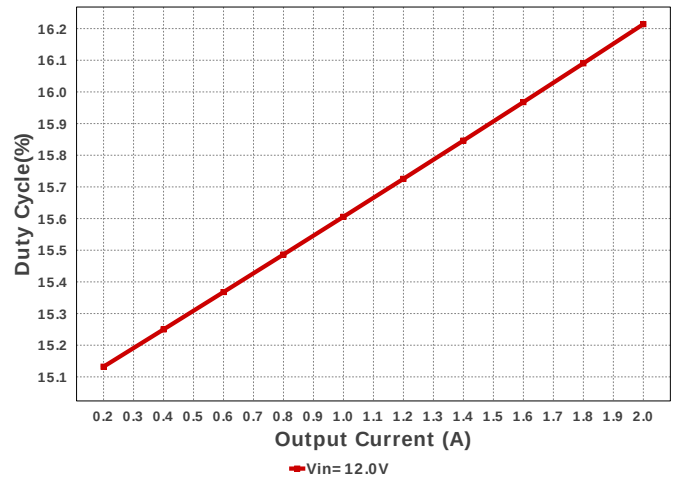
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cff	MuRata	GRM155R71C104KA88D Series= X7R	Cap= 100.0 nF ESR= 1.0 mOhm VDC= 16.0 V IRMS= 0.0 A	1	\$0.01	0402 3 mm ²
Cin	TDK	C1608X5R1E685K080AC Series= X5R	Cap= 6.8 uF ESR= 4.211 mOhm VDC= 25.0 V IRMS= 2.5341 A	2	\$0.17	0603 5 mm ²
Cinx	TDK	CGA2B2X7R1H222K050BA Series= X7R	Cap= 2.2 nF ESR= 1.0779 Ohm VDC= 50.0 V IRMS= 264.071 mA	1	\$0.01	0402 3 mm ²
Cout	MuRata	GRM21BR61A226ME44L Series= X5R	Cap= 22.0 uF ESR= 3.0 mOhm VDC= 10.0 V IRMS= 3.84 A	2	\$0.13	0805 7 mm ²
Cout1	MuRata	GRM21BR61A226ME44L Series= X5R	Cap= 22.0 uF ESR= 3.0 mOhm VDC= 10.0 V IRMS= 3.84 A	1	\$0.13	0805 7 mm ²
Css	MuRata	GRM188R60J474KA01D Series= X5R	Cap= 470.0 nF ESR= 1.0 mOhm VDC= 6.3 V IRMS= 0.0 A	1	\$0.02	0603 5 mm ²
L1	Abracon Corporation	ASPI-0530HI-2R2M-T2	L= 2.2 uH 35.0 mOhm	1	\$0.41	ASPI-0530HI 55 mm ²
L2	Würth Elektronik	782853200	L= 0.0 H 8.0 mOhm	1	\$0.09	0805 7 mm ²
Rfbb	Vishay-Dale	CRCW04024K87FKED Series= CRCW..e3	Res= 4.87 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Rfbt	Vishay-Dale	CRCW04026K04FKED Series= CRCW..e3	Res= 6.04 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rpg	Vishay-Dale	CRCW040210K0FKED Series= CRCW..e3	Res= 10.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rsconfig	Vishay-Dale	CRCW040280K6FKED Series= CRCW..e3	Res= 80.6 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
U1	Texas Instruments	TPS62913RPUR	Switcher	1	\$1.16	RPU0010A-MFG 9 mm ²

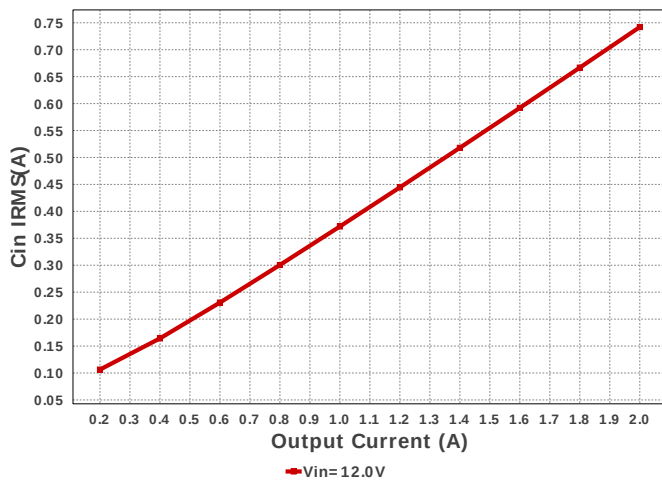
IC Tj



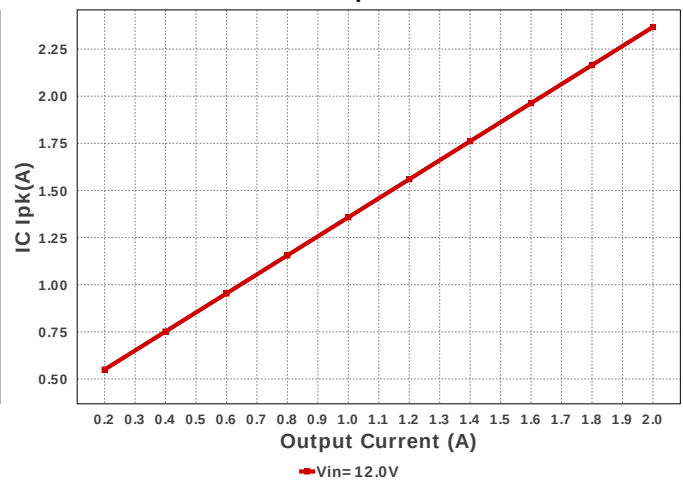
Duty Cycle

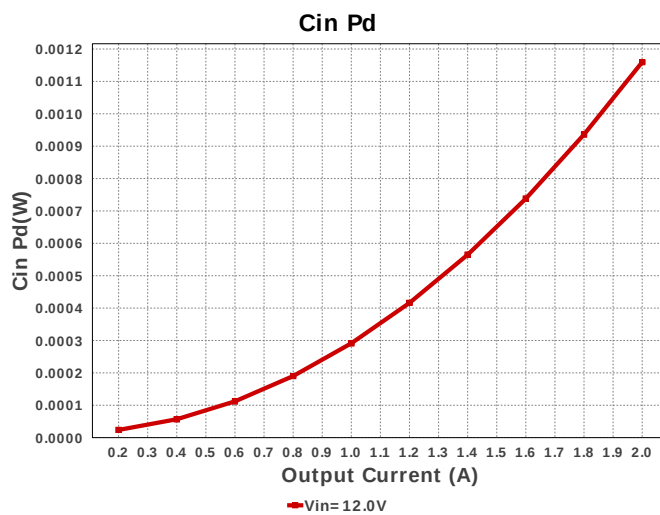
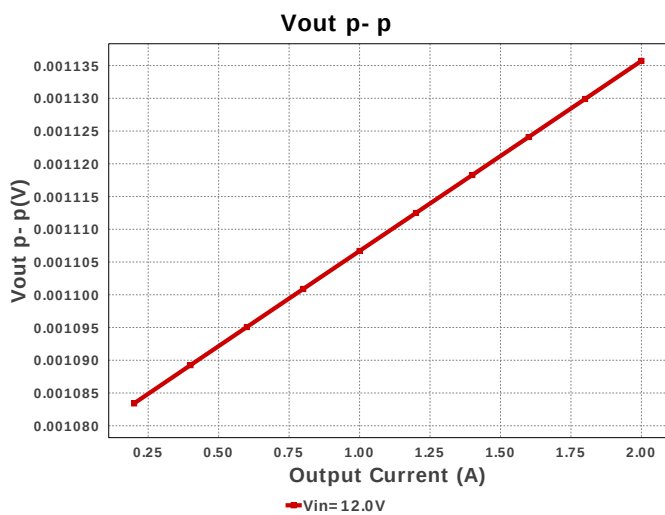
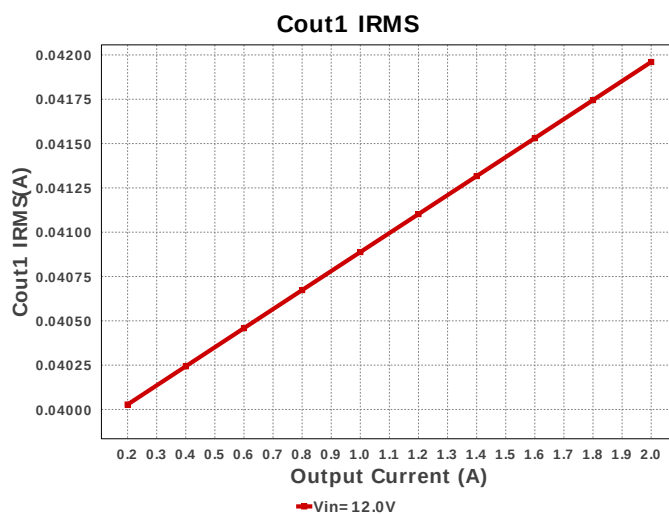
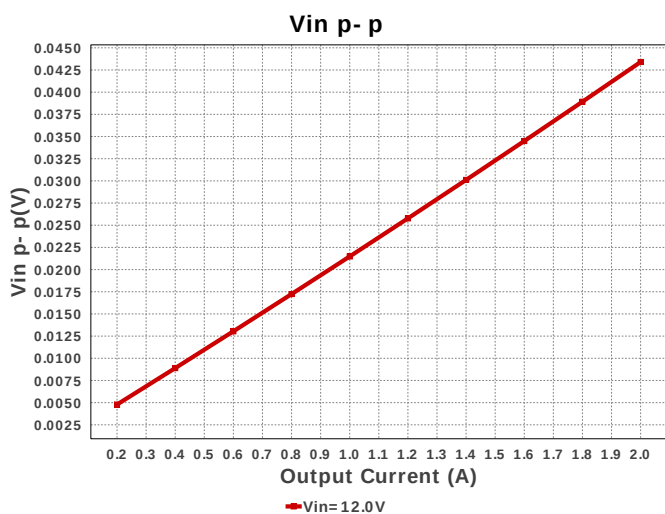
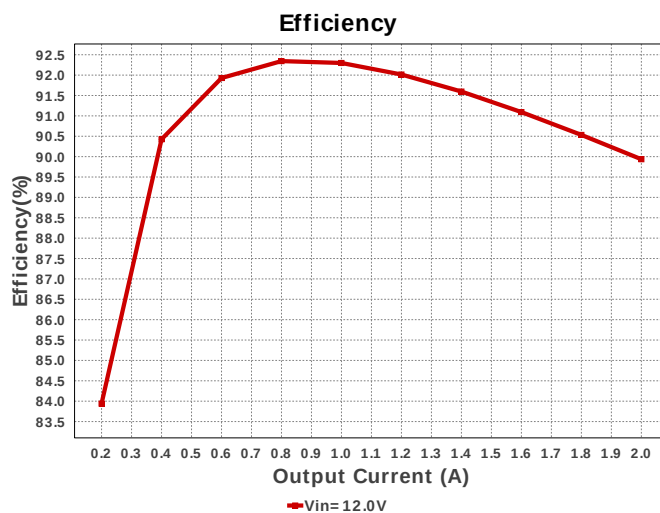
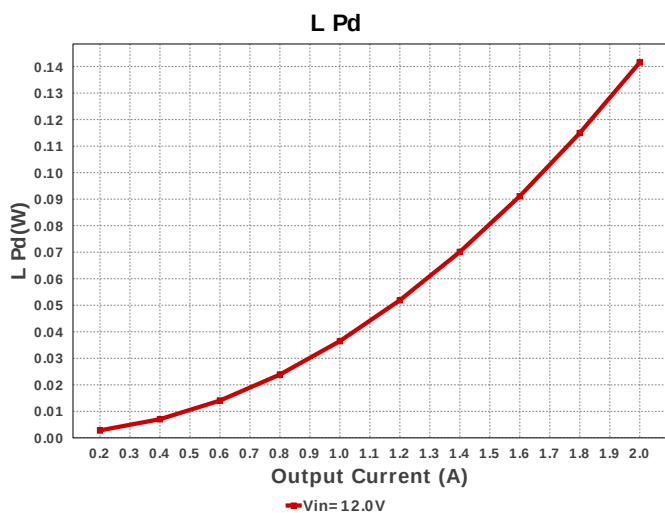


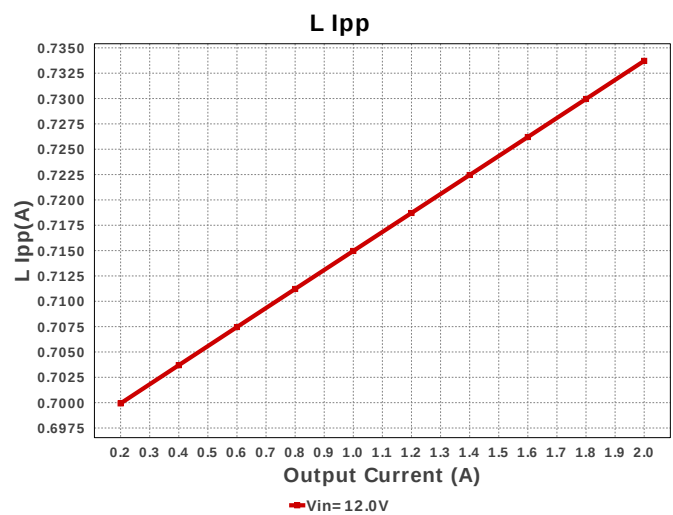
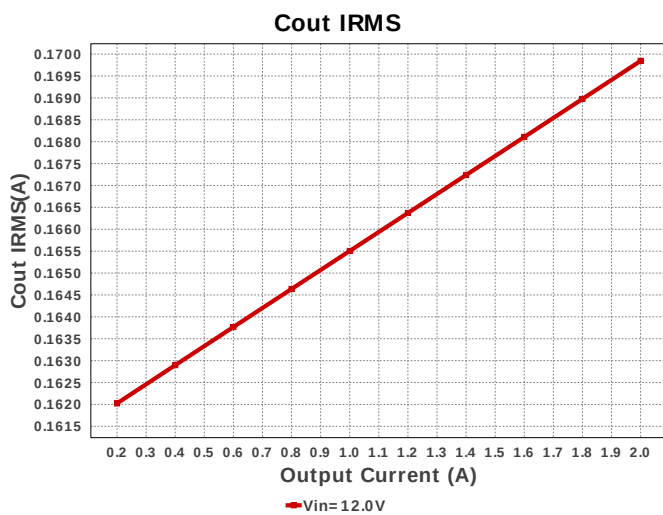
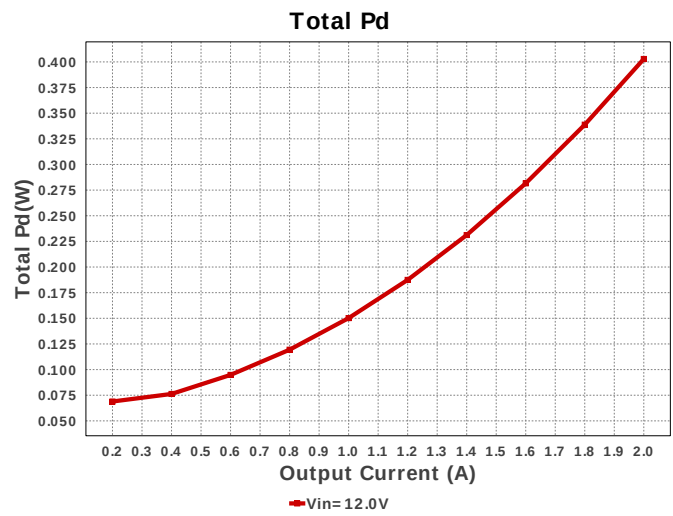
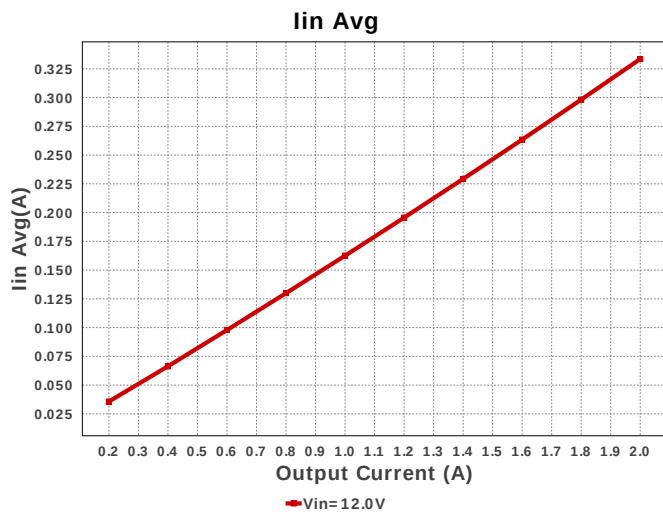
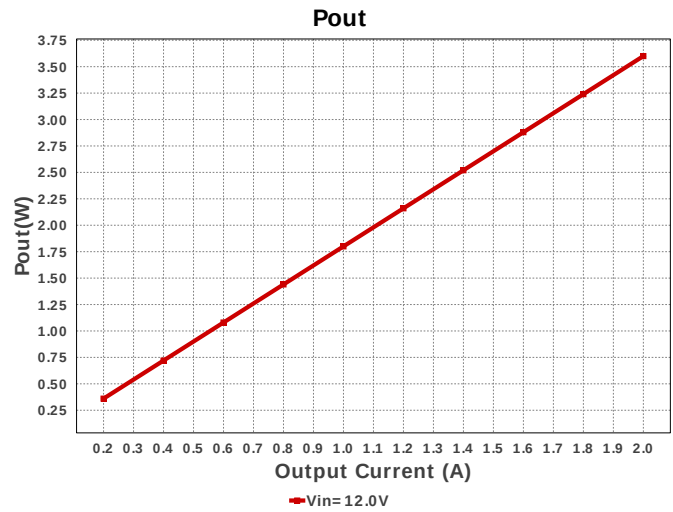
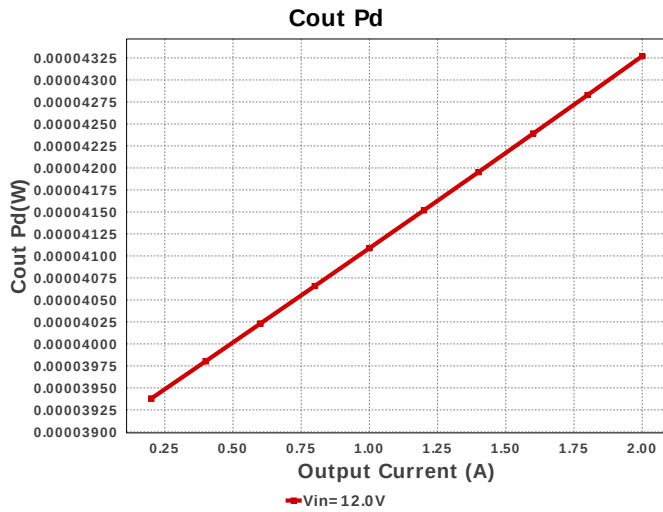
Cin IRMS

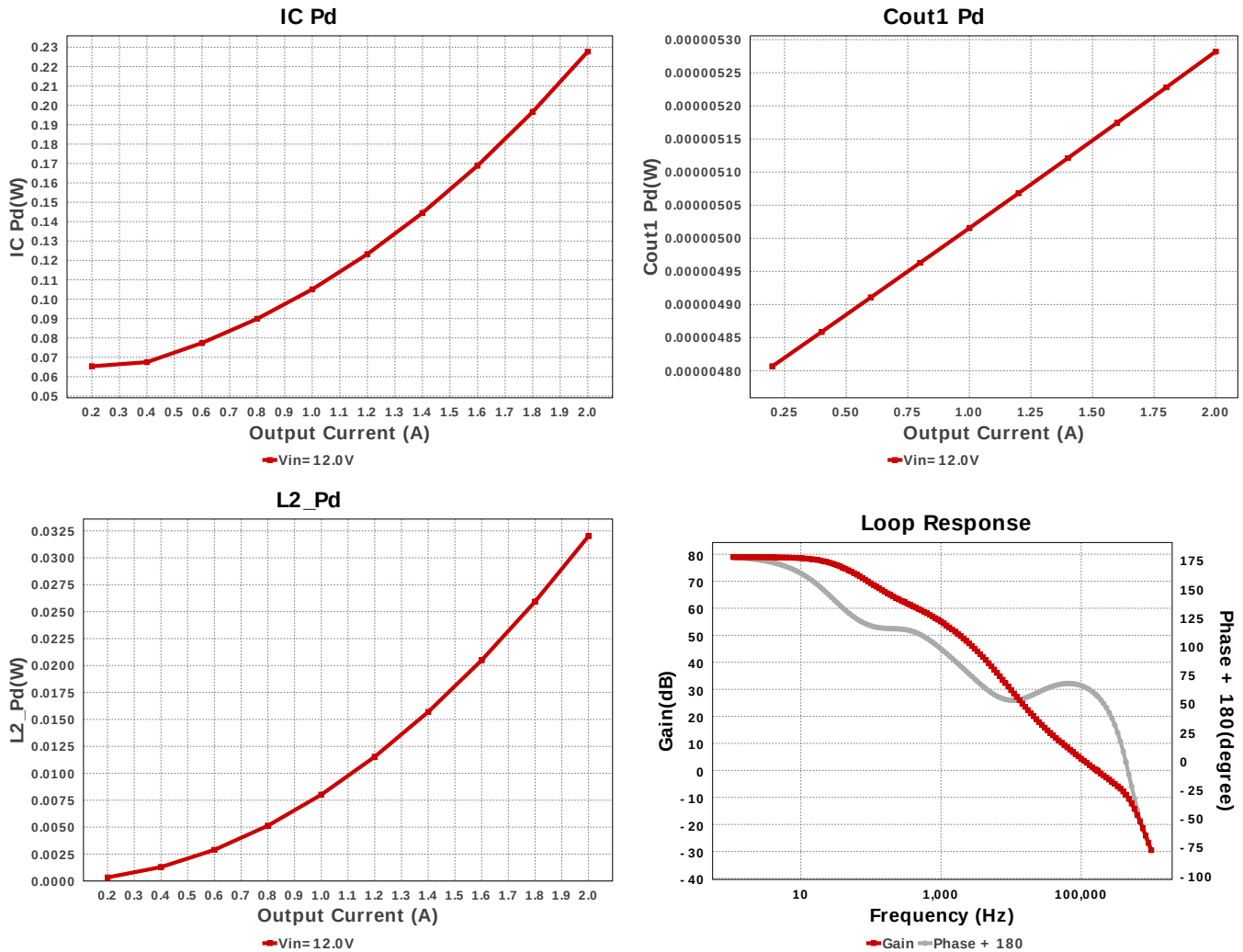


IC Ipk









Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	742.076 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	1.16 mW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	169.845 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	43.271 μ W	Capacitor	Output capacitor power dissipation
5.	Cout1 IRMS	41.96 mA	Capacitor	Output capacitor1 RMS ripple current
6.	Cout1 Pd	5.282 μ W	Capacitor	Output capacitor1 power dissipation
7.	IC IpK	2.367 A	IC	Peak switch current in IC
8.	IC Pd	227.77 mW	IC	IC power dissipation
9.	IC Tj	97.892 degC	IC	IC junction temperature
10.	ICThetaJA	56.6 degC/W	IC	IC junction-to-ambient thermal resistance
11.	Iin Avg	333.57 mA	IC	Average input current
12.	Ipp percentage	36.686 %	Inductor	Inductor ripple current percentage (with respect to average inductor current)
13.	L Ipp	733.72 mA	Inductor	Peak-to-peak inductor ripple current
14.	L Pd	141.57 mW	Inductor	Inductor power dissipation
15.	L2_Pd	32.014 mW	Inductor	Inductor2 power loss
16.	Cin Pd	1.16 mW	Power	Input capacitor power dissipation
17.	Cout Pd	43.271 μ W	Power	Output capacitor power dissipation
18.	Cout1 Pd	5.282 μ W	Power	Output capacitor1 power dissipation
19.	IC Pd	227.77 mW	Power	IC power dissipation
20.	L Pd	141.57 mW	Power	Inductor power dissipation
21.	L2_Pd	32.014 mW	Power	Inductor2 power loss
22.	Total Pd	402.846 mW	Power	Total Power Dissipation
23.	BOM Count	15	System	Total Design BOM count
24.	Cross Freq	166.833 kHz	System	Bode plot crossover frequency
25.	Duty Cycle	16.214 %	System	Duty cycle
26.	Efficiency	89.936 %	System	Steady state efficiency

#	Name	Value	Category	Description
27.	FootPrint	123.0 mm ²	System Information	Total Foot Print Area of BOM components
28.	Frequency	1000.0 kHz	System Information	Switching frequency
29.	Gain Marg	-8.982 dB	System Information	Bode Plot Gain Margin
30.	Iout	2.0 A	System Information	Iout operating point
31.	Low Freq Gain	78.919 dB	System Information	Gain at 1Hz
32.	Mode	FCCM	System Information	Conduction Mode
33.	Phase Marg	57.662 deg	System Information	Bode Plot Phase Margin
34.	Pout	3.6 W	System Information	Total output power
35.	Total BOM	\$2.47	System Information	Total BOM Cost
36.	Vin	12.0 V	System Information	Vin operating point
37.	Vin p-p	43.403 mV	System Information	Peak-to-peak input voltage
38.	Vout	1.8 V	System Information	Operational Output Voltage
39.	Vout Actual	1.792 V	System Information	Vout Actual calculated based on selected voltage divider resistors
40.	Vout Tolerance	1.624 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors at 25 degC
41.	Vout p-p	1.136 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	2.0	Maximum Output Current
SoftStart	5.0 ms	Soft Start Time (ms)
VinMax	12.0	Maximum input voltage
VinMin	12.0	Minimum input voltage
Vout	1.8	Output Voltage
base_pn	TPS62913	Base Product Number
source	DC	Input Source Type
Ta	85.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of C_{in} and C_{out} , and the inductance and DC resistance of $L1$ before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

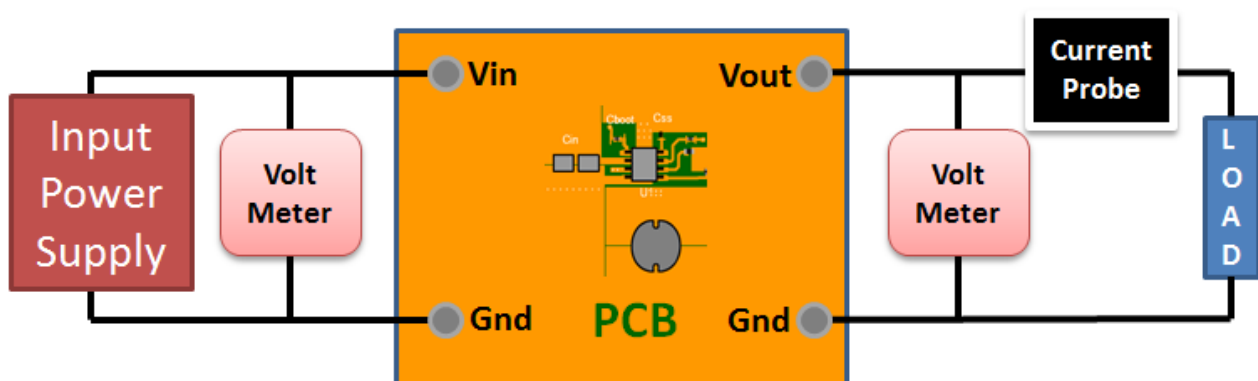
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab down to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 12.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to V_{in} and GND. Connect a digital volt meter and a load if needed to set the minimum load of the design from V_{out} and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between V_{in} and GND, a load is connected between V_{out} and GND and a current meter is connected in series between V_{out} and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.

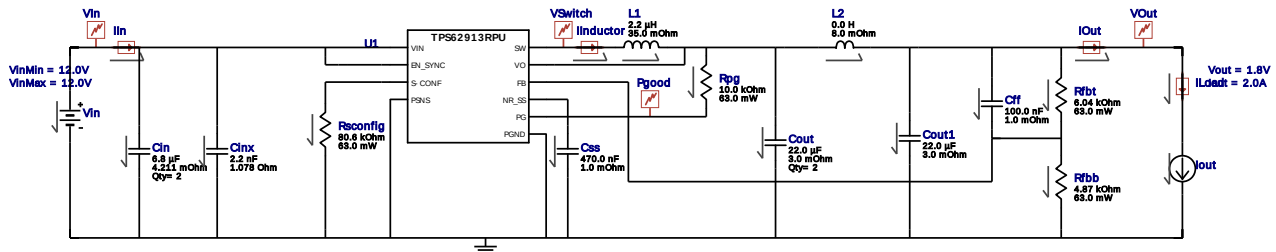


WEBENCH® Electrical Simulation Report

Design Id = 788

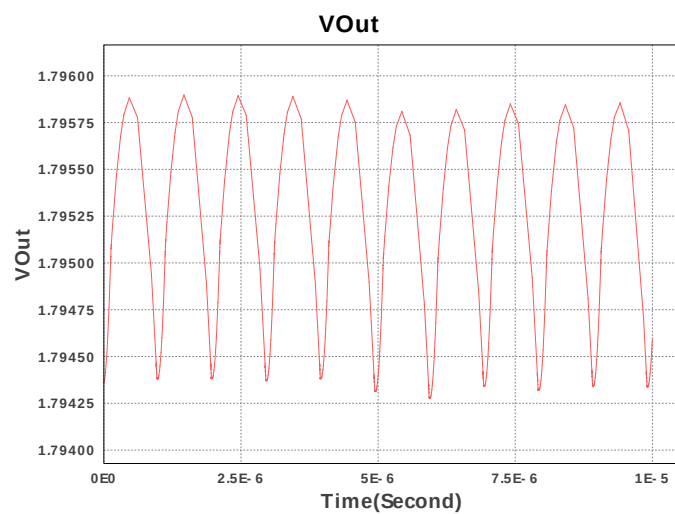
sim_id = 1

Simulation Type = Steady State



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	L1	IC	no description	2.0
2.	Css	IC	no description	0.8 V
3.	Cin	IC	Initial Condition	VinDefault V
4.	Cout	IC	Initial V	Vout V
5.	Iout	I	output current	2.0 A



Design Assistance

- Master key : 705BAF3F164BD058[v1]
- TPS62913** Product Folder : <http://www.ti.com/product/TPS62913> : contains the data sheet and other resources.

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