



About = Input Box

V 1.0.0 February 2024

Step 1: Operating Specifications

Input Voltage - Min, $V_{IN(min)}$	4.2 V
Input Voltage - Nom, $V_{IN(nom)}$	12 V
Input Voltage - Max, $V_{IN(max)}$	24 V
Output Voltage, V_{OUT}	5 V
Full Load Output Current, $I_{OUT(max)}$	6 A
Switching Frequency, f_{SW}	400 kHz
Frequency Set Resistor, R_T	20 k Ω

Step 2: Filter Inductor

Recommended Filter Inductance	1.4 μ H
Inductance, L_F	1.8 μ H
Inductor DCR	10 m Ω
PK-to-PK Ripple Current at $V_{IN(min)}$, ΔI_L	1.0 A _{pk-ck}
PK-to-PK Ripple Current at $V_{IN(nom)}$, ΔI_L	4.1 A _{pk-ck}
PK-to-PK Ripple Current at $V_{IN(max)}$, ΔI_L	5.6 A _{pk-ck}
ΔI_L as a % at $V_{IN(min)}$	13 %
ΔI_L as a % at $V_{IN(nom)}$	69 %
ΔI_L as a % at $V_{IN(max)}$	94 %

Step 3: OCP, Sense Resistors, Slope Comp

Required $I_{OCP(MIN)}$ Setpoint at $V_{IN(nom)}$	6 A
Recommended Sense Resistance	14.2 m Ω
Sense Resistance, R_S	10 m Ω
Peak Inductor Current, $I_{L(PK)}$	13.6 A
Power Loss in R_S at Full Load (Max VIN)	0.30 W
Recommended SLOPE Capacitance	68 pF
SLOPE Capacitance, C_{SLOPE}	68 pF
$V_{IN(min)}$	9.4 A
$I_{OUT(TYP)}$ at OCP Inception: $V_{IN(nom)}$	10.1 A
$V_{IN(max)}$	10.8 A
Set Const Current Loop Setpoint (?)	5 A
Output Leg Shunt Resistance, $R_{CS(OUT)}$	10 m Ω

Step 4: Output Capacitor

Output Voltage Ripple Spec	50 mV _{pk-pk}
Minimum Output Capacitance	53.6 μ F
Output Capacitance, C_{OUT}	100 μ F
Maximum Permitted ESR	3.9 m Ω
Output Capacitor ESR	2 m Ω
Resulting Output Voltage Ripple (max)	39 mV _{pk-pk}
Output Capacitor RMS Current (max)	2.6 A (rms)

Step 5: Input Capacitor

Input Voltage Ripple Spec	200 mV _{pk-pk}
Minimum Input Capacitance	18.8 μ F
Input Capacitance, C_{IN}	44 μ F
Maximum Permitted ESR	13.0 m Ω
Input Capacitor ESR	2 m Ω
Resulting Input Voltage Ripple (max)	103 mV _{pk-pk}
Input Capacitor RMS Current (max)	3.0 A (rms)

Step 6: Soft-start, Dither, UVLO

Soft-Start Time, t_{SS}	15 ms
Soft-Start Capacitance, C_{SS}	100 nF
Modulating Frequency	10 kHz
DITHER Enabled	<input checked="" type="checkbox"/>
DITHER Capacitance, C_d	3.9 nF
Required Input Voltage UVLO On	4 V
Input Voltage UVLO Off	3.25 V
Upper UVLO Resistor, R_{UV1}	249 k Ω
Lower UVLO Resistor, R_{UV2}	93.1 k Ω

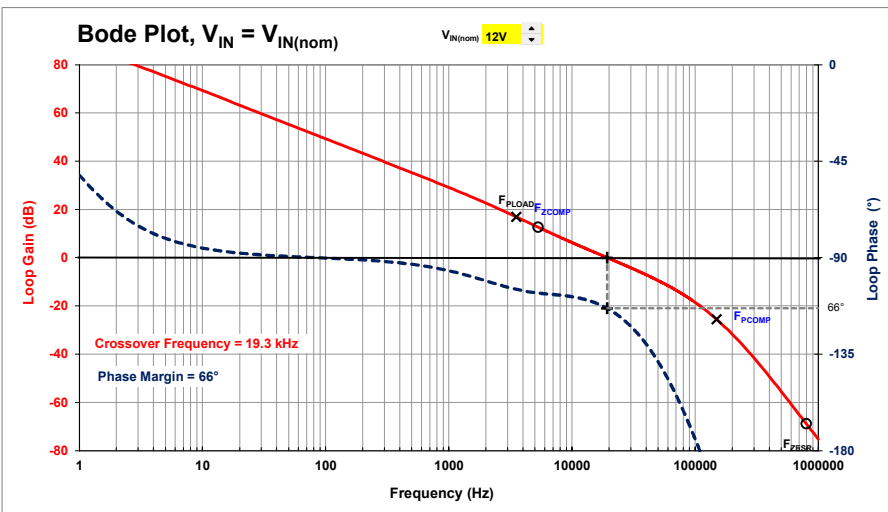
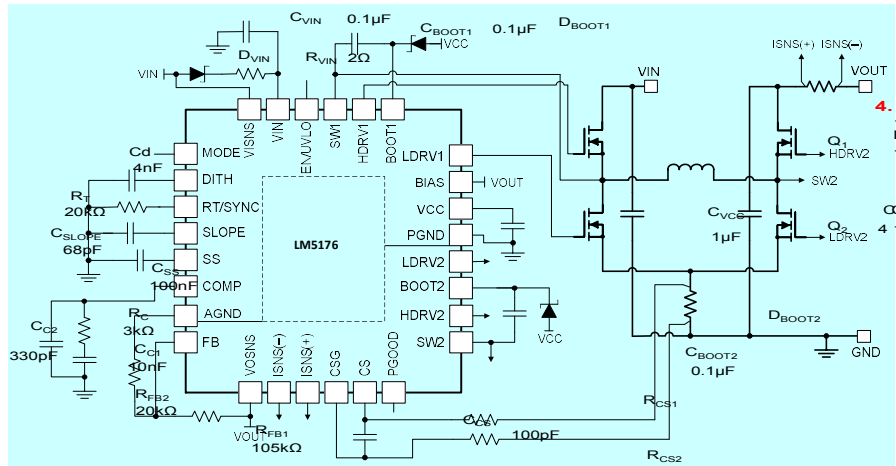
Step 7: Compensation Design

Load Pole Frequency	3532 Hz
C_{OUT} ESR Zero Frequency	796 kHz
Boost RHP Zero Frequency	24 kHz
Desired Crossover Frequency	20 kHz
Error Amp Pole Frequency	1 Hz
Upper Feedback Resistor, R_{FB1}	105 k Ω
Lower Feedback Resistor, R_{FB2}	20 k Ω

Compensation Components

Component	Calculated / Std Values	Selected	Actual PzZ Frequencies
R_C	3.1 / 3.09	3 k Ω	1 Hz (F_{PEA})
C_{C1}	9.7 / 10	10 nF	5.3 kHz (F_{ZCOMP})
C_{C2}	342 / 330	330 pF	149 kHz (F_{PCOMP})

Min COMP Voltage 0.24V
Max COMP Voltage 2.06V



Efficiency / Power Loss Analyzer

Step 8: Efficiency

Buck-Leg Power MOSFETs (Q1, Q2) CSD18563Q5A	
	Hi-side / Low-side
On-State Resistance, $R_{DS(on)}$	5.7 / 5.7 m Ω
Total Gate Charge, Q_G	11 / 11 nC
Gate-Drain Charge, Q_{GD}	2.9 / 2.9 nC
Gate-Source Charge, Q_{GS}	3.3 / 3.3 nC
Gate Resistance, R_G	1.5 / 1.5 Ω
Transconductance, g_{FS}	60 / 60 S
Gate-Source Threshold Voltage, V_{TH}	4 / 4 V
Body Diode Forward Voltage, V_{FD}	0.8 / 0.8 V
Body Diode Rev Recovery Charge, Q_{RR}	63 nC
Thermal Resistance, θ_{JA}	50 / 50 $^{\circ}$ C/W

Boost-Leg Power MOSFETs (Q3, Q4) CSD16321Q5	
	Hi-side / Low-side
On-State Resistance, $R_{DS(on)}$	1.9 / 1.9 m Ω
Total Gate Charge, Q_G	22 / 22 nC
Gate-Drain Charge, Q_{GD}	2.5 / 2.5 nC
Gate-Source Charge, Q_{GS}	4 / 4 nC
Gate Resistance, R_G	1.5 / 1.5 Ω
Transconductance, g_{FS}	150 / 150 S
Gate-Source Threshold Voltage, V_{TH}	2 / 2 V
Body Diode Forward Voltage, V_{FD}	0.8 / 0.8 V
Body Diode Rev Recovery Charge, Q_{RR}	33 nC
Thermal Resistance, θ_{JA}	50 / 50 $^{\circ}$ C/W

External Schottky Diode (if applicable)	Buck Leg	Boost Leg
Schottky Fwd Voltage, V_{FWDsch}	0 V	0 V
Schottky Rev Recovery Charge, Q_{RRsch}	0 nC	0 nC

Efficiency vs IOUT Plot

