Cross Conduction in Modern Power MOSFETs

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Introduction

The synchronous buck converter is the DC-DC converter of choice in PC and notebook computers and has been so for many years. This topology provides ease of control and high power conversion efficiencies at a relatively low cost and within a small footprint. One of the keys to success in designing a synchronous buck converter is limiting the shoot-through or cross-conduction current. This phenomenon can cause excessive losses which leads to poor performance and results in low power conversion efficiency. Mathematical formulae will be derived that allow MOSFET and power supply designers to test the suitability of a specific device for its use as a synchronous rectifier in this converter.

Choosing the Right MOSFET

Shoot-through may be explored by examining the factors that control the induced gate-source voltage when the drain voltage is switched between near ground and input voltage, V_{cc}, levels. This situation is encountered in the Synchronous Buck topology (Figure 1) during the time interval when the top or control MOSFET, $M_{HS,}$ is switched ON while the PWM controller holds OFF the lower MOSFET or synchronous rectifier M_{LS}.

If the induced voltage is larger than the Gate Threshold Voltage of the MOSFET, M_{LS} could be turned ON while the top MOSFET is ON. Since an ON MOSFET has a very low on-resistance in the order of few milliohms to a few tens of milliohms, this condition will result in fairly excessive currents flowing through both devices, leading to excessive power dissipation in both MOSFETs and ultimately to failure in either one or both devices. By examining the mechanism causing this phenomenon, proper MOSFET selection can be made and cross conduction can be eliminated or reduced to negligible levels.

Shoot-Through in the Synchronous Buck Converter

A common synchronous buck converter is shown in Figure 1:

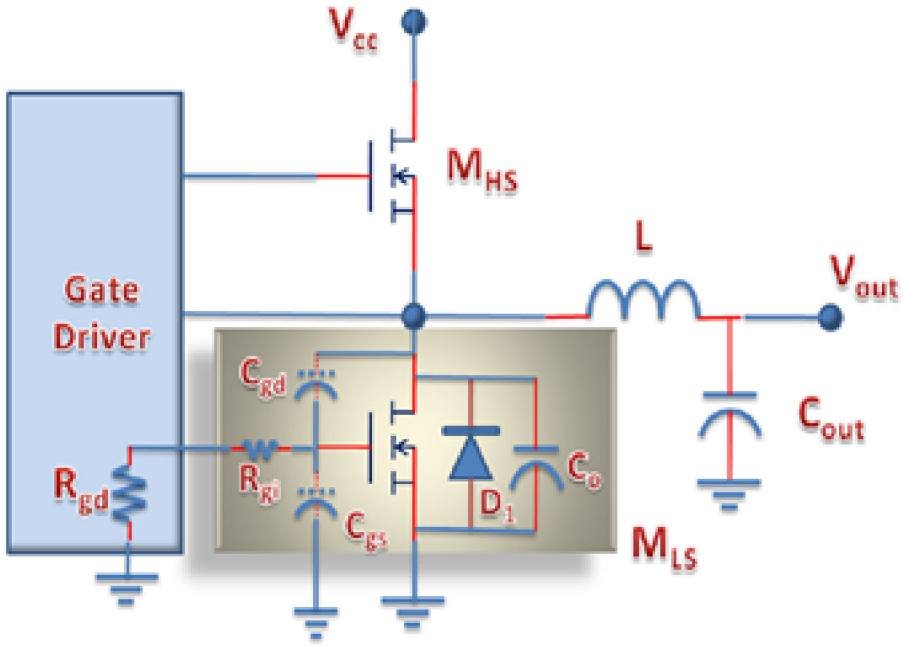


Figure 1. A common synchronous buck converter using two N-channel MOSFETs. The synchronous rectifier, M_{LS}, is shown with internal lumped parameters.

Assume the lower MOSFET, M_{LS}, is initially turned OFF and the top MOSFET, M_{HS}, turned ON. This applies the input voltage on one end of the inductor, causing the inductor current to ramp up. When M_{HS} is turned OFF, the current will continue flowing through the inductor but now it flows through the body diode D1 of M_{LS}. After a dead time on the order of a few tens of nanoseconds—dictated by the PWM controller—the MOSFET M_{LS} turns ON. This allows all the inductor current now to flow through M_{LS} rather than D1, since the voltage drop across its R_{DSON} is much lower than the diode voltage drop. Assuming that the current through the inductor does not reach zero (the Continuous Conduction Mode), the voltage across the lower MOSFET will simply be $= R_{DSON} \cdot I_{LOAD}$ during the full on period of the M_{LS} where R_{DSON} *i*s the on-resistance and I_{LOAD} is the inductor current ≈ the load current.

Assumptions

In the following analysis we will assume, for simplicity, that all the electrodes parasitic inductances are negligible. This will allow us to derive simple equations with reasonable accuracies.

Analysis

Figure 2 shows the lower MOSFET in the OFF state and its equivalent circuit for this analysis.

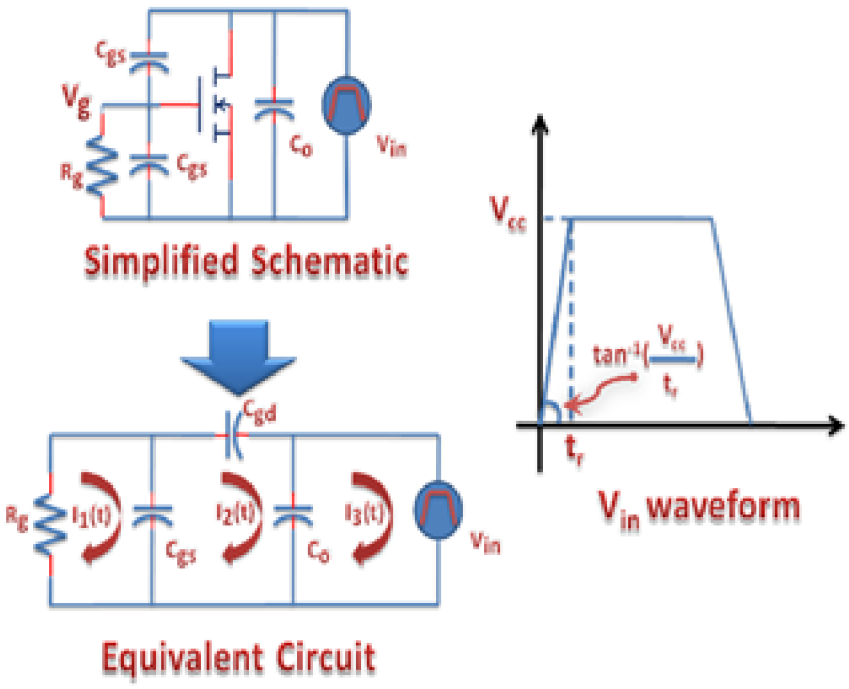


Figure 2. Resistances, capacitances and voltages associated with the lower MOSFET in the synchronous buck converter, equivalent circuit and V_{in} waveform.

The analysis begins by writing Kirchoff's equations for the equivalent circuit of M_{LS}. *Vin* is a voltage source representing the effect of the external circuit as the top MOSFET , M_{HS}, turns ON. The Drain Voltage $Vin = a \cdot t$, where *a* is the rate of change of the drain voltage and t is time. Kirchoff's loop equation for this circuit yields:

$$Vin := a \cdot t :$$

$$e1 := Vin = \int \frac{i3(t)}{Co}\, dt - \int \frac{i2(t)}{Co}\, dt :$$

$$e11 := \frac{d}{dt}\, e1 = a = \frac{i3(t)}{Co} - \frac{i2(t)}{Co}$$

$$e2 := i2(t) \cdot \left(\frac{1}{Co} + \frac{1}{Cgd} + \frac{1}{Cgs} \right) - \frac{i3(t)}{Co} - \frac{i1(t)}{Cgs} = 0 :$$

$$e3 := Rg \cdot i1(t) + \int \frac{i1(t)}{Cgs}\, dt - \int \frac{i2(t)}{Cgs}\, dt = 0 :$$

Where

$Rg = R_{gi} + R_{gd}$ and R_{gi} is the internal effective gate resistance and R_{gd} is the gate driver integrated circuit sink resistance.

$$e33 := \frac{d}{dt} e3 = Rg \left(\frac{d}{dt} i1(t) \right) + \frac{i1(t)}{Cgs} - \frac{i2(t)}{Cgs} = 0$$

Solving equations e11, e2 and e33 provides the value of current through the gate resistor:

$$sols := dsolve(\{e11, e2, e33, i1(0) = 0\}, [i1(t), i2(t), i3(t)]) :$$

$$i1t := simplify(eval(i1(t), sols)) = -\left(-1 + e^{-\frac{t}{Rg(Cgd + Cgs)}} \right) Cgd\, a$$

where $i1t$ is the current flowing in the gate resistor Rg.

Now we can calculate the gate voltage:

$$Vg := i1t \cdot Rg = -\left(-1 + e^{-\frac{t}{Rg(Cgd + Cgs)}} \right) Cgd\, a\, Rg$$

The condition for no shoot-through in a given MOSFET under a given rate of change of the Drain Voltage a can be calculated using the Vg equation. At the end of the rise time, $t=t_r$ and $Vin=V_{cc}$ (usually is 5V or 12V). At this instance, if $Vg>Vg_{th}$ (the MOSFET gate threshold voltage) cross conduction occurs. To find the value that will cause cross conduction, the equation of Vg can be derived by substituting $t = tr = \frac{Vcc}{a}$:

$$Vgl := subs\left(t = \frac{Vcc}{a}, Vg \right)$$

$$-\left(-1 + e^{-\frac{Vcc}{Rg(Cgd + Cgs)\, a}} \right) Cgd\, a\, Rg \qquad \textbf{(1)}$$

For a very fast rise time we can take the limit of equation (1) to get the gate voltage Vglimit at a point where the rise time=0 i.e. $a = \infty$.

$$Vglimit := \lim_{a \to \infty} Vgl$$

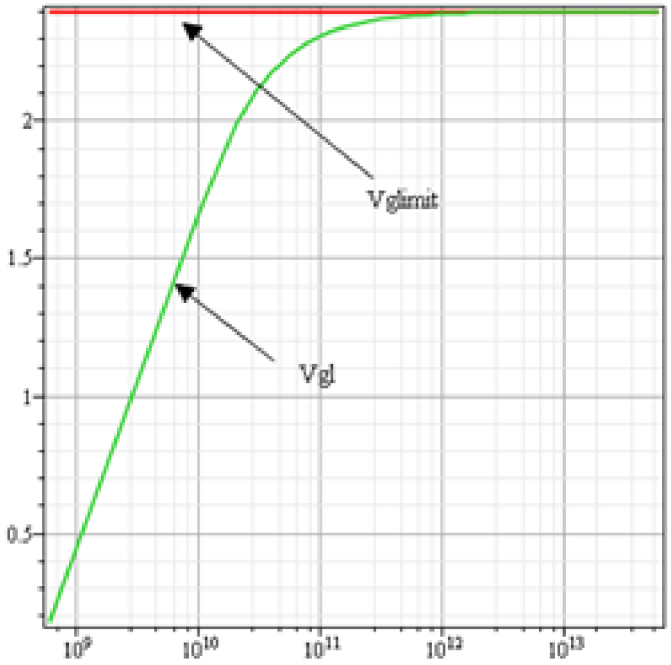
$$\frac{Vcc\, Cgd}{Cgd + Cgs} \qquad \textbf{(2)}$$

Equation (2) is a very important one since it indicates that if $\frac{Vcc\, Cgd}{Cgs + Cgd} \leq Vg_{th}$ there will be no shoot-through for any value of a. This can be achieved in so many ways like reducing the value of C_{gd} or increasing V_{gth} or C_{gs}. Increasing C_{gs} is not a good idea since it will adversely affect the dynamic losses. Also, notice that the equation is independent of Rg, which is to be expected. As a gets larger, the reactance of C_{gs} becomes much smaller than Rg and it becomes the only determining factor, since both

components are connected in parallel. Alternatively, if $Vg > V_{gth}$, then cross conduction can be expected at some level of a.

Even if a MOSFET meets the condition $Vg \geq V_{gth}$ in equation (2), it still may be suitable for the application as a synchronous rectifier as long as it satisfies equation (1) for an actual circuit rise time.

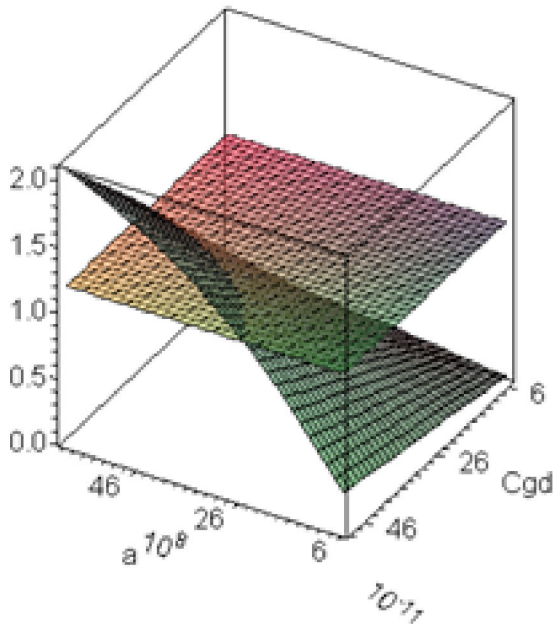
$$plot(\{subs(Cgs = 1.2\cdot 10^{-9},\ Cgd = 300\cdot 10^{-12},\ Vcc = 12,\ Rg = 1,\ Vgl), subs(Cgs = 1.2\cdot 10^{-9},\ Cgd = 300\cdot 10^{-12},\ Vcc = 12,\ Rg = 1,\ Vglimit)\}, a = 6 * 10^{8}..6\cdot 10^{13}, numpoints = 200, thickness = 2, resolution = 300, gridlines = true, axes = box, axis[1] = [mode = \log])$$



The above graph depicts both Vgl and the Vglimit. Clearly the gate voltage almost reaches the asymptotic value of Vglimit at $a \approx 10^{12}$.

In order to examine the range at which shoot-through occurs, we plot the gate voltage as a function of C_{gd} and a.

$$plot3d(\{subs(Cgs = 1.2\cdot 10^{-9},\ Rg = 1, Vcc = 12,\ Vgl), 1.2\},\ a = 6 * 10^{8}..6\cdot 10^{9}, Cgd = 50\cdot 10^{-12}..500\cdot 10^{-12}, axes = boxed, numpoints = 1000, transparency = 0.4, lightmodel = light2)$$



The above graph shows the V_{gth} plane at 1.2V and the induced gate voltage Vgl as a function of C_{gd} and *a*. All points above the V_{gth} plane should be expecting shoot-through at varying degrees proportional to the value of $\left(Vgl - V_{gth}\right)^2$.

Worst Case Analysis

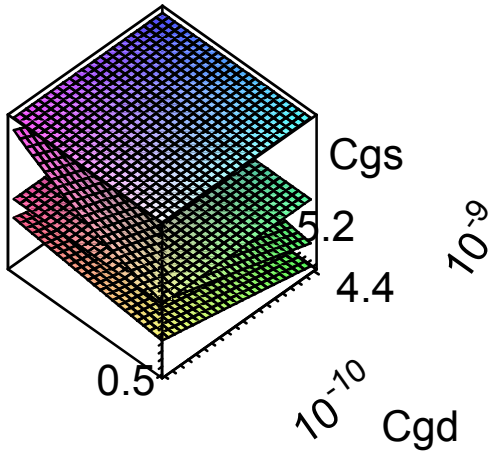
One last task we can do is to examine the suitability of a specific MOSFET for a 12 V application by evaluating the worst case MOSFET parameters conditions.

From the M_{LS} datasheet, the MOSFET parameters are:

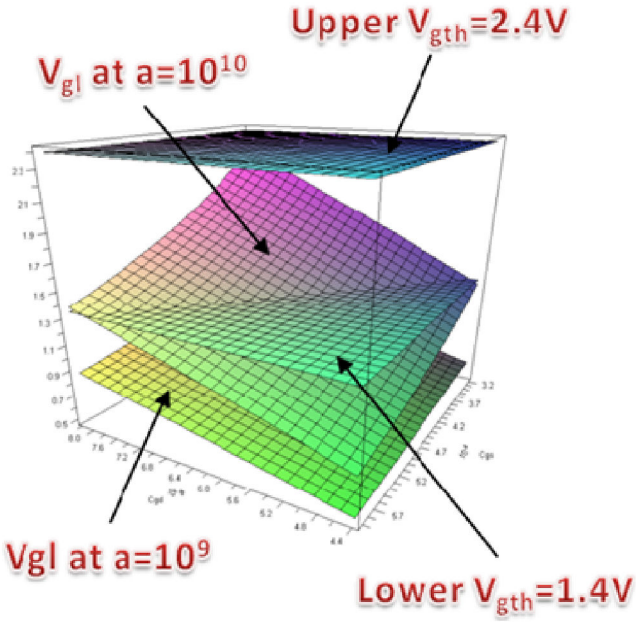
C_{gs}=3185pf..5915 pF C_{gd}=441pf..819 pF Rg=1..1.6 Ω V_{gth}=1.35..2.4 Ω

We can use equation (1) to do the evaluation using a 3D graph as seen below. The use of 3D graphing is particularly useful to get a more complete view of the gate voltage over the full tolerance of C_{gd}, C_{gs} and V_{gth} and effectively pinpointing the full range of the problem.

plot3d({*subs*(*a* = 10^{10}, *Rg* = 1.6, *Vcc* = 12, *Vgl*), *subs*(*a* = 10^{9}, *Rg* = 1.6, *Vcc* = 12, *Vgl*), 1.35, 2.4}, *Cgd* = 441·10^{-12} ..819 ·10^{-12}, *Cgs* = 3185·10^{-12} ..5915·10^{-12}, *axes* = *boxed*)



Vgl for $a = 10^9$ and $a = 10^{10}$ and gate threshold planes
at minimum and maximum gate thresholds of 1.4 and 2.4 V.



Identification of different curves.

As can be seen in the 3-D graph above, M_{LS} with V_{gth} at the upper limit of tolerance of 2.4V have no shoot-through problems over the entire tolerance range of both C_{gd} and C_{gs}. However for V_{gth} close to the lower limit of tolerance of 1.4V, designers should expect some significant shoot-through. The graph above right is there only to identify the different curves in relation to each other for reference.

Full Cycle Examination

Now that we have derived equations (1) and (2) that enable us to examine the propensity of a specific MOSFET for shoot-through,

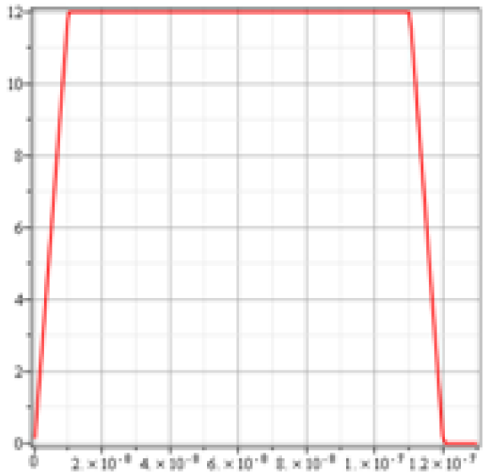
let us have a look at the MOSFET's response to one full wave.

$$tf := 10^{-8} : Vpk := 12 : ton := 10^{-7} : a := \frac{Vpk}{tr} : a := \frac{Vpk}{tr} : t1 := tr : t2 := tr + ton : t3 := t2 + tr : T := 2E\text{-}6 :$$

Using the Heaviside function, the input voltage for a full cycle may be represented as follows:

$$Vint := \text{Heaviside}(t) * a * t - \text{Heaviside}(t - tr) * a * t + \text{Heaviside}(t - tr) * Vpk - \text{Heaviside}(t - t2) * a * (t - t2) + \text{Heaviside}(t - t3) * a * (t - t3) :$$

$plot(subs(tr = 10^{-8},\ Vint), t = 0\ ..ton + 30E\text{-}9, gridlines = true, axes = box, thickness = 2)$



Now we can solve the same set of Kirchhoff equations using the s domain familiar to all electrical engineers. This is done to examine voltages and currents at the beginning and end of a single pulse.

$Vins := inttrans[laplace](Vint, t, s)$:

$$ea := Vins = \frac{i3}{s \cdot Co} - \frac{i2}{s \cdot Co} :$$

$$eb := i2 \cdot \left(\frac{1}{s \cdot Co} + \frac{1}{s \cdot Cgd} + \frac{1}{s \cdot Cgs} \right) - \frac{i3}{s \cdot Co} - \frac{i1}{s \cdot Cgs} = 0 :$$

$$ec := Rg \cdot i1 + \frac{i1}{s \cdot Cgs} - \frac{i2}{s \cdot Cgs} = 0 :$$

$solsa := solve(\{ea, eb, ec\}, \{i1,\ i2, i3\})$:

$i1s := eval(i1, solsa)$:

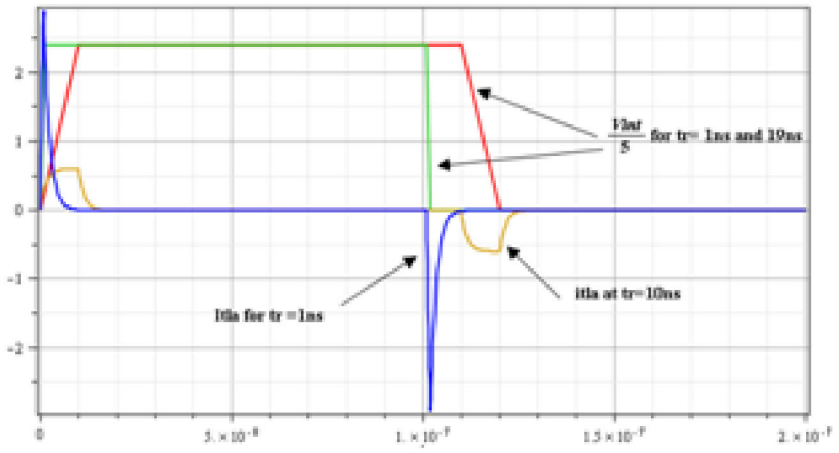
$i1ta := inttrans[invlaplace](i1s, s, t)$:

$Vga := Rg \cdot i1ta$:

Of particular importance is the *ilta* because this current must flow in the gate driver of M_{LS} without forcing it out of saturation and further aggravating the situation.

$plot(\{subs(Rg = 1, Cgd = 5 \cdot 10^{-10}, Cgs = 1 \cdot 10^{-9}, tr = 10^{-9},\ i1ta), subs(Rg = 1, Cgd = 5 \cdot 10^{-10}, Cgs = 1$

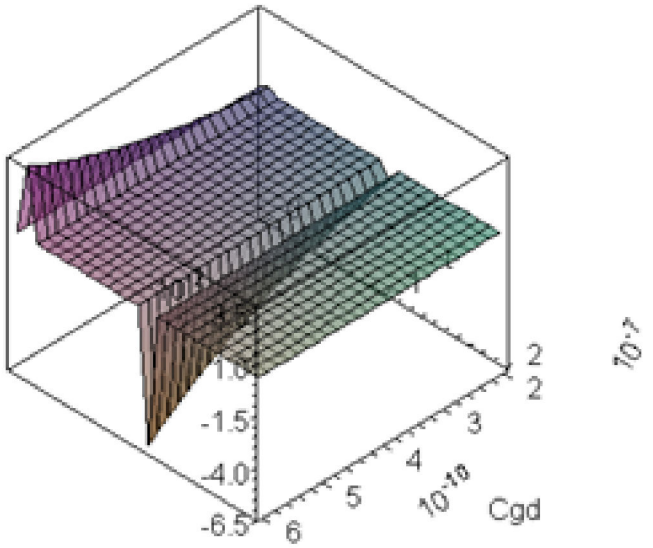
$$\cdot 10^{-9},\ tr = 10^{-8},\ i1ta\big),\ subs\left(tr = 10^{-9},\ \frac{Vint}{5}\right),\ subs\left(tr = 10^{-8},\ \frac{Vint}{5}\right)\Big\},\ t = 0\ ..ton + 10^{-7},$$
$$numpoints = 500,\ thickness = 2,\ gridlines = true,\ axes = box\Big)$$



By plotting the current at two different risetimes, *tr*, we can clearly observe that the current *ilta* is significantly higher in the case of $tr = 10^{-9}$ as compared to that at $tr = 10^{-8}$. For the time being we need not concern ourselves with rise times faster than 1 ns since almost all converters operate at a lower value.

Now we can examine the effect of gate-drain capacitance, $C_{gd,}$ on the value of the gate voltage Vga by plotting Vga as a function of both time and C_{gd} and keeping the remaining variables at a constant value.

$$plot3d\big(\{subs\big(Rg = 1,\ Cgs = 1\cdot 10^{-9},\ tr = 10^{-9},\ Vga\big)\},\ Cgd = 2\cdot 10^{-10}\ ..6\cdot 10^{-10},\ t = 0\ ..ton + 10^{-7},$$
$$transparency = 0.4,\ lightmodel = light2,\ axes = boxed\big)$$

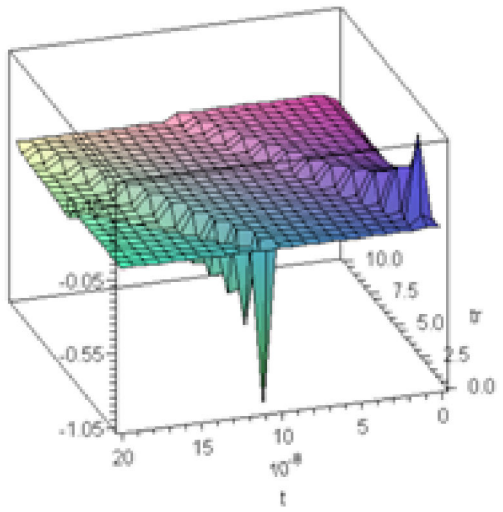


One can observe that an M_{LS} MOSFET with a higher Cgd value is more prone to shoot-through when compared to a lower value one.

Looking at one last plot of *i1ta* as a function of *tr* and time with the rest of the variables held constant, we can see the full range of currents that may be observed for different risetimes. This graph is very useful when designing synchronous buck converters because the current *i1ta* is also sinked by the output stage of the gate driver of M_{LS}.

Most commercially available gate drivers can sink and source a maximum of about 2 A. This means that if *i1ta* is larger than the maximum gate driver current, the output stage will get out of saturation resulting in the gate voltage climbing even higher, resulting in a more serious shoot-through condition.

$$plot3d(\{subs(Rg=1, Cgs=1\cdot 10^{-9}, Cgd=4\cdot 10^{-10}, i1ta)\}, tr=10^{-7}..10^{-10}, t=0..ton+10^{-7}, axes=boxed)$$



Conclusion:

1. Equation (1) should be used to evaluate a given MOSFET's susceptibility to shoot-through for almost all applications today.
2. Equation (2) should be used for the projected applications of the next few years where the rise and fall times are in the sub-nanosecond range.
3. We ignored the effect of MOSFET electrode inductances to derive simple and reasonably accurate equations. The use of parasitic inductances makes the problem so complicated that a simple equation is not attainable.
4. Shoot-through rarely results in a catastrophic failure of the MOSFETs. In general, it results in modest to serious degradation of the converter efficiency, resulting in higher operation temperatures.