XBL6021-SM Series

One Cell Lithium-ion/Polymer Battery Protection IC

GENERAL DESCRIPTION

The XBL6021-SM Series product is a high integration solution for lithium-ion/polymer battery protection. XBL6021-SM Series contains advanced power MOSFET, high-accuracy voltage detection circuits and delay circuits. XBL6021-SM Series is put into an DFN1X1x0.37-4 package and external MCU, GPIO signal to high level to enable the chip to enter shipping mode makes it an ideal solution in limited space of battery pack.

XBL6021-SM Series has all the protection functions required in the battery application including overcharging, over discharging, overcurrent and load short circuiting protection etc. The accurate overcharging detection voltage ensures safe and full utilization charging. The low standby current drains little current from the cell while in storage.

The device is not only targeted for digital cellular phones, but also for any other Li-Ion and Li-Poly battery-powered information appliances requiring long-term battery life.

FEATURES

- Protection of Battery Cell Reverse Connection with external load
- Control MOS of integrated shipping mode
- Support all pin rosin joint
- Integrate Advanced Power MOSFET with Equivalent of 55mΩ $R_{SS(ON)}$
- DFN 1x1x0.37-4Package
- Reverse connection of charger is supported
- Overdischarge Current 1 Protection
- Charger Detection Function
- 0V Battery Charging Function
- Delay Times are generated inside
- High-accuracy Voltage Detection
- Over-Discharge Self-locking
- Low Current Consumption
  -Operation Mode:0.5μA typ.
  -Power-down Mode: 10nA max.
- RoHS Compliant and Lead (Pb) Free
- Be suitable for 100% shipping mode

APPLICATIONS

One-Cell Lithium-ion Battery Pack
Lithium-Polymer Battery Pack
Wearable Device
Bluetooth Earphone

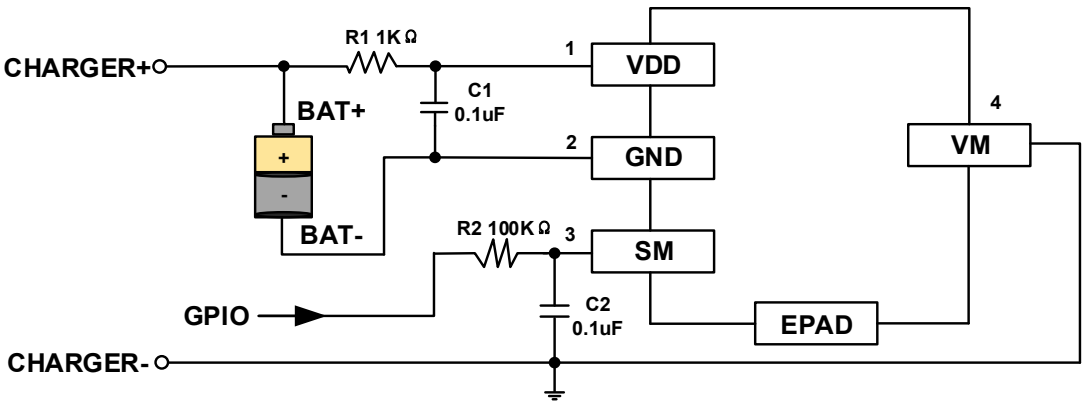


Figure 1. Typical Application Circuit

(Suggestion: Connect EPAD pin with GND)

ORDERING INFORMATION

Conventional basic voltage temperature parameters: Ta=25℃

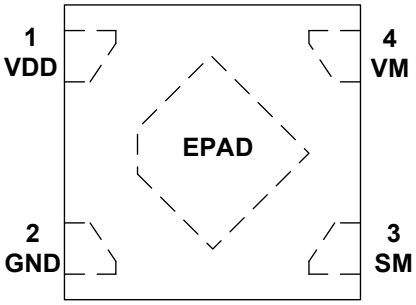
PART NUMBER	OCV [VCU] (V) （Ta=25℃）	OCV* [VCU] (V) （Ta=-5℃ ~55℃）	OCRV [VCL] (V)	ODV [VDL] (V)	ODRV [VDR] (V)	TOP MARK
XBL6021Q2S-SM	4.275±25mV	4.275±30mV	4.075±50mV	2.8±50mV	3.0±80mV	YWxx(note)
XBL6021J2S-SM	4.425±25mV	4.425±30mV	4.25±50mV	2.8±50mV	3.0±80mV	
XBL6021M2S-SM	4.475±25mV	4.475±30mV	4.30±50mV	2.8±50mV	3.0±80mV	

Conventional basic voltage temperature parameters: Ta=-40℃~85℃*

PART NUMBER	OCV [VCU] (V)	OCRV [VCL] (V)	ODV [VDL] (V)	ODRV [VDR] (V)	TOP MARK
XBL6021Q2S-SM	4.275-50mV ~4.275+35mV	4.075-75mV ~4.075+60mV	2.800-80mV ~2.800+80mV	3.000-100mV ~3.000+100mV	YWxx(note)
XBL6021J2S-SM	4.425-50mV ~4.425+35mV	4.250-75mV ~4.250+60mV	2.800-80mV ~2.800+80mV	3.000-100mV ~3.000+100mV	
XBL6021M2S-SM	4.475-50mV ~4.475+35mV	4.300-75mV ~4.300+60mV	2.800-80mV ~2.800+80mV	3.000-100mV ~3.000+100mV	

Note:1).“YW” is manufacture date code, “Y” means the year, “W” means the week.
2).“xx” is internal product code of XySemi.
*： Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

PIN CONFIGURATION



TOP VIEW

Figure 2. PIN Configuration

PIN DESCRIPTION

XBL6021-SM SERIES PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDD	Power Supply.
2	GND	Ground, connect the negative terminal of the battery to these pins.
3	SM	This Pin relative to VM is connected to high pulse signal, so that the chip enters SM mode.
4	VM	The negative terminal of the battery pack. The internal FET switch connects this terminal to GND.
EPAD	NC	Not Use. Suggest to connect with GND.

ABSOLUTE MAXIMUM RATINGS

(NOTE: DO NOT EXCEED THESE LIMITS TO PREVENT DAMAGE TO THE DEVICE. EXPOSURE TO ABSOLUTE MAXIMUM RATING CONDITIONS FOR LONG PERIODS MAY AFFECT DEVICE RELIABILITY.)

PARAMETER	VALUE	UNIT
VDD input pin voltage	-0.3 to 9	V
VM input pin voltage	-8 to 10	V
SM input pin voltage	-0.3 to 9	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C
Power Dissipation at T=25°C	0.3	W
Package Thermal Resistance (Junction to Ambient) θJA	250	°C/W
Package Thermal Resistance (Junction to Case) θJC	130	°C/W
ESD HBM	8000	V

ELECTRICAL CHARACTERISTICS

Typical and limits appearing in normal type apply for TA = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Detection voltage						
Discharge over-current release Voltage	V_{RIOV1}		VDD-1.0	VDD-0.7	VDD-0.4	V
Detection Current						
Overdischarge Current Detection	I_{IOV1}	V_{DD}=3.6V	0.10	0.15	0.20	A
Overcharge Current Detection	I_{CHOC}	V_{DD}=3.6V	0.20	0.30	0.40	A
Load Short-Circuiting Detection	*I_{SHORT}	V_{DD}=3.6V	0.30	0.45	0.60	A
Current Consumption						
Current Consumption in Normal Operation	I_{OPE}	VDD=3.6V VM =0V		0.5	0.8	μA
Current Consumption in Power Down	I_{PD}	VDD=2.0V VM pin floating			10	nA
VM Internal Resistance						
Internal Resistance between VM and V_{DD}	*R_{VMD}	VDD =2.0V VM pin floating	100	150	200	kΩ
Internal Resistance between VM and GND	*R_{VMS}	VDD=3.6V VM=3.6V	15	25	35	kΩ
Logic Levels on SM						
Logic Low input voltage to VM	V_{SML}				0.5	V
Logic High input voltage to VM	V_{SMH}		1.3			V
FET on Resistance						
Equivalent FET on Resistance	*$R_{SS(ON)}$	V_{DD}=3.6V I_{VM} =0.1A		55		mΩ
Detection Delay Time						
Overcharge Voltage Detection De-layTime	t_{CU}		58	185	255	mS
Overdischarge Voltage Detection Delay Time	t_{DL}		16	40	48	mS
Overdischarge Current1 Detection Delay Time	t_{IOV1}	V_{DD}=3.6V	4	10	15	mS
Overcharge Current Detection Delay Time	t_{CHOC}	V_{DD}=3.6V	4	10	15	mS
Load Short-Circuiting Detection Delay Time	*t_{SHORT}	V_{DD}=3.6V	144	350	500	μS
SM Detection Delay Time	t_{SM}		16	40	56	mS

Note1:

*：Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS

Typical and limits appearing in normal type apply for TA = -40˚C~85˚C, unless otherwise specified.*

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Detection voltage						
Discharge over-current release Voltage	V_{RIOV1}		VDD-1.1	VDD-0.7	VDD-0.3	V
Detection Current						
Overdischarge Current Detection	I_{IOV1}	V_{DD}=3.6V	0.07	0.15	0.26	A
Overcharge Current Detection	I_{CHOC}	V_{DD}=3.6V	0.14	0.30	0.52	A
Load Short-Circuiting Detection	*I_{SHORT}	V_{DD}=3.6V	0.21	0.45	0.78	A
Current Consumption						
Current Consumption in Normal Operation	I_{OPE}	VDD=3.6V VM =0V		0.5	1.0	μA
Current Consumption in Power Down	I_{PD}	VDD=2.0V VM pin floating			0.2	μA
VM Internal Resistance						
Internal Resistance between VM and V_{DD}	*R_{VMD}	VDD =2.0V VM pin floating	80	150	240	kΩ
Internal Resistance between VM and GND	*R_{VMS}	VDD=3.6V VM=3.6V	12	25	42	kΩ
Logic Levels on SM						
Logic Low input voltage to VM	V_{SML}				0. 4	V
Logic High input voltage to VM	V_{SMH}		1.6			V
FET on Resistance						
Equivalent FET on Resistance	*$R_{SS(ON)}$	V_{DD}=3.6V I_{VM}=0.1A		55		mΩ
Detection Delay Time						
Overcharge Voltage Detection De-layTime	t_{CU}		46.5	185.0	357.0	mS
Overdischarge Voltage Detection Delay Time	t_{DL}		12.8	40.0	67.2	mS
Overdischarge Current1 Detection Delay Time	t_{IOV1}	V_{DD}=3.6V	3.2	10.0	21.0	mS
Overcharge Current Detection Delay Time	t_{CHOC}	V_{DD}=3.6V	3.2	10.0	21.0	mS
Load Short-Circuiting Detection Delay Time	*t_{SHORT}	V_{DD}=3.6V	115.0	350.0	700.0	μS
SM Detection Delay Time	t_{SM}		12.8	40.0	78.5	mS

Note1:

*：Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

FUNCTIONAL BLOCK DIAGRAM

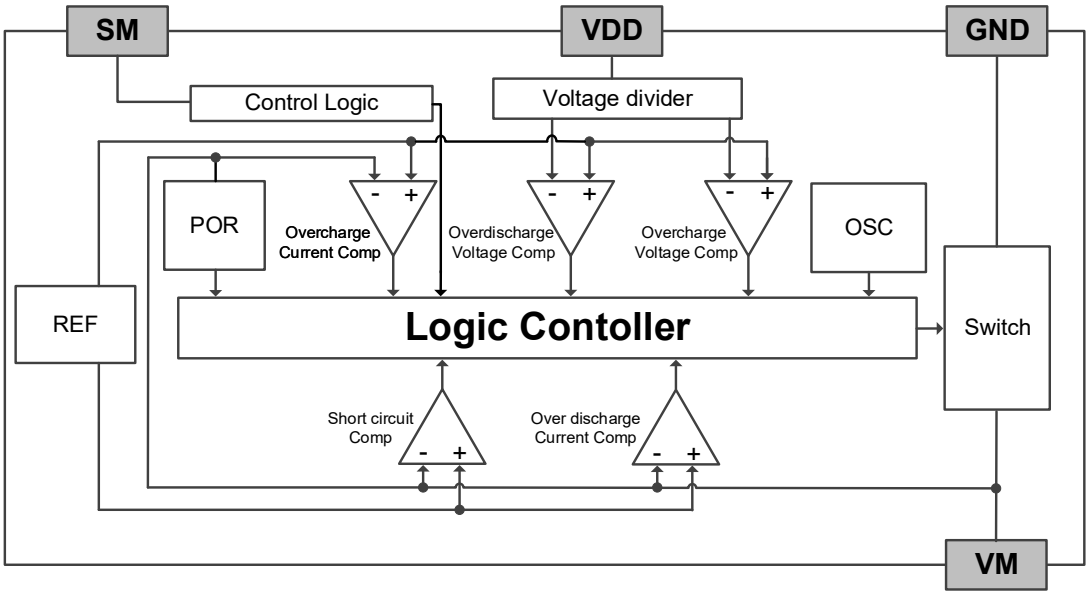


Figure 3. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The XBL6021-SM Series monitors the voltage and current of a battery and protects it from being damaged due to overcharge voltage, overdischarge voltage, overdischarge current, and short circuit conditions by disconnecting the battery from the load or charger. These functions are required in order to operate the battery cell within specified limits.

The device has built in R1 and C1 circuitry to ensure the proper operation of the chip,and built-in R2 and C2 to enhance the anti-interference circuitry. The MOSFET is integrated and its $R_{SS(ON)}$ is as low as 55mΩ typical.

Normal operating mode

If no exception condition is detected, charging and discharging can be carried out freely. This condition is called the normal operating mode.

Overcharge Condition

When the battery voltage becomes higher than the overcharge detection voltage (V_{CU}) during charging under normal condition and the state continues for the overcharge detection delay time (t_{CU}) or longer, the XBL6021-SM Series turns the charging control FET off to stop charging. This condition is called the overcharge condition. The overcharge condition is released in the following two cases:

1. When the connected charger battery voltage drops below the overcharge release voltage (V_{CL}), the XBL6021-SM Series turns the charging control FET on and returns to the normal condition.

2. When a load is connected and discharging starts, the XBL6021-SM Series turns the charging control FET on and returns to the normal condition. The release mechanism is as follows: the discharging current flows through an internal parasitic diode of the charging FET immediately after a load is connected and discharging starts, and the VM pin voltage increases about 0.7V (forward voltage of the diode) from the GND pin voltage momentarily. The XBL6021-SM Series detects this voltage and releases the overcharge condition. Consequently, in the case that the battery voltage is e

qual to or lower than the overcharge detection voltage (V_{CU}), the XBL6021-SM Series returns to the normal condition immediately, but in the case the battery voltage is higher than the overcharge detection voltage (V_{CU}),the chip does not return to the normal condition until the battery voltage drops below the overcharge detection voltage (V_{CU}) even if the load is connected. In addition, if the VM pin voltage is equal to or lower than the overcurrent detection voltage when a load is connected and discharging starts, the chip does not return to the normal condition.

Remark :

If the battery is charged to a voltage higher than the overcharge detection voltage (V_{CU}) and the battery voltage does not drops below the overcharge detection voltage (V_{CU}) even when a heavy load, which causes an overcurrent, is connected, the overcurrent do not work until the battery voltage drops below the overcharge detection voltage (V_{CU}). Since an actual battery has, however, an internal impedance of several dozens of mΩ, and the battery voltage drops immediately after a heavy load which causes an overcurrent is connected, the overcurrent work. Detection of load short-circuiting works regardless of the battery voltage.

Overdischarge Condition

When the battery voltage drops below the overdischarge detection voltage (V_{DL}) during discharging under normal condition and it continues for the overdischarge detection delay time (t_{DL}) or longer, the XBL6021-SM Series turns the discharging control FET off and stops discharging. This condition is called overdischarge condition. After the discharging control FET is turned off, the VM pin is pulled up by the R_{VMD} resistor between VM and VDD in XBL6021-SM Series. The current of the chip is reduced to the power-down current (I_{PDN}). This condition is called power-down condition. The VM and VDD pins are shorted by the R_{VMD} resistor in the IC under the overdischarge and power-down conditions.

The power-down condition is released when a charger is connected and the potential difference between VM and VDD becomes 2.0V (typ.) or higher (0V charger voltage when charging). At this time, the FET is still off. When the battery voltage becomes 1.6V or higher (see note), the XBL6021-SM Series turns the FET on and changes to the normal condition from the overdischarge condition.

Remark:

If the VM pin voltage is no less than the GND voltage ,when the battery under overdischarge condition is connected to a charger, the over discharge condition is released (the discharging control FET is turned on) as usu-al, provided that the battery voltage reaches the overdischarge voltage (V_{DL}) or higher.

Overcurrent Condition

When the discharging current becomes equal to or higher than a specified value (the VM pin voltage is equal to or higher than the overcurrent detection voltage) during discharging under normal condition and the state continues for the overcurrent detection delay time or longer, the XBL6021-SM Series turns off the discharging control FET to stop discharging. This condition is called overcurrent condition. (The overcurrent includes overcurrent, or load short-circuiting.)

The VM and GND pins are shorted internally by the R_{VMS} resistor under the overcurrent condition. When a load is connected, the VM pin voltage equals the VDD voltage due to the load.

The overcurrent condition returns to the normal condition when the load is released and the impedance between the B+ and B- pins becomes higher than the automatic recoverable impedance. When the load is removed, the VM pin goes back to the GND potential since the VM pin is shorted the GND pin with the R_{VMS} resistor. Detecting that the VM pin potential is lower than the overcurrent detection voltage ,the IC returns to the normal condition.

Abnormal Charge Current Detection

If the VM pin voltage drops below the charger detection voltage during charging under the normal condition and it continues for the overcharge detection delay time (t_{choc}) or longer, the XBL6021-SM Series turns the charging control FET off and stops charging. This action is called abnormal charge current detection.

Abnormal charge current detection works when the charging control FET is on and the VM pin voltage drops below the charger detection voltage .When an abnormal charge current flows into a battery in the overcharge condition, the XBL6021-SM Series consequently turns the charging control FET off and stops charging after the battery voltage becomes the overcharge detection voltage and the overcharge detection delay time (t_{choc}) elapses.

Abnormal charge current detection is released when the voltage difference between VM pin and GND pin becomes lower than the charger detection voltage by separating the charger. Since the 0 V battery charging function has higher priority than the abnormal charge current detection function, abnormal charge current may not be detected by the product with the 0 V battery charging function while the battery voltage is low.

Load Short-circuiting condition

If voltage of VM pin is equal or above short circuiting protection voltage , the XBL6021-SM Series will stop discharging and battery is disconnected from load.The maximum delay time to switch current off is t_{SHORT}. This status is released when voltage of VM pin is lower than short protection voltage ,such as when disconnecting the load.

Delay Circuits

The detection delay time for load short-circuiting starts when overdischarge current 1 is detected. As soon as load short-circuiting is detected over detection delay time for load short- circuiting, the XBL6021-SM Series stops discharging. When battery voltage falls below overdischarge detection voltage due to overdischarge current, the XBL6021-SM Series stop discharging by overdischarge current detection. In this case the recovery of battery voltage is so slow that if battery voltage after overdischarge voltage detection delay time is still lower than over discharge detection voltage, the XBL6021-SM Series shifts to power-down.

0V Battery Charging Function (1) (2) (3)

This function enables the charging of a connected battery whose voltage is 0 V by self-discharge.

Note:

(1) Some battery providers do not recommend charging of completely discharged batteries. Please refer to battery providers before the selection of 0 V battery charging function.

(2) The 0V battery charging function has higher priority than the abnormal charge current detection function. Consequently, a product with the 0 V battery charging function charges a battery and abnormal charge current cannot be detected during the battery voltage is low (at most 1.8 V or lower).

(3) When a battery is connected to the IC for the first time, the IC may not enter the normal condition in which discharging is possible. In this case, set the VM pin voltage equal to the GND voltage (short the VM and GND pins or connect a charger) to enter the normal condition.

Discharge Over-current /Short Self-recovery

The recovery condition of short circuit/ discharge overcurrent is that the VM voltage is less than V_{RIOV1}.

TIMING CHART

1. Overcharge and Overdischarge voltage detection

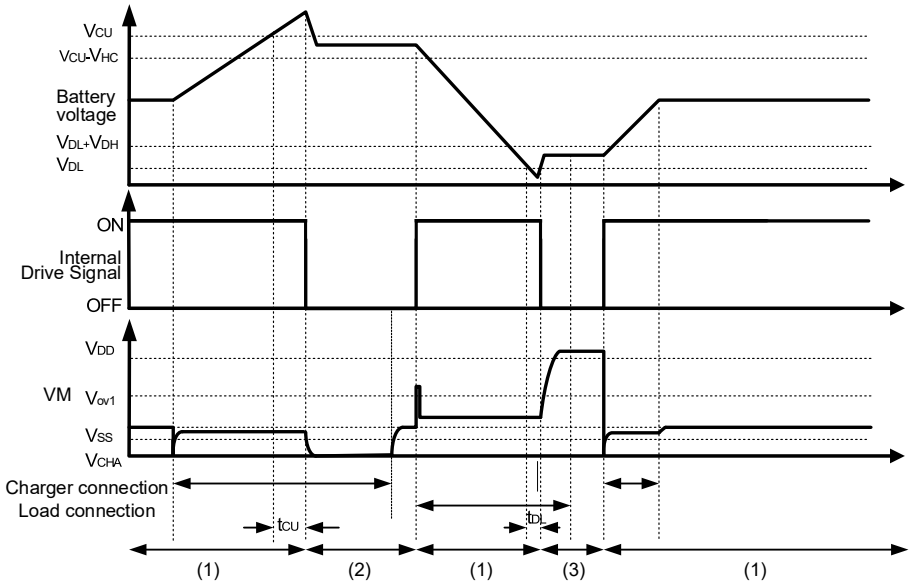


Figure4-1 Overcharge and Overdischarge Voltage Detection

Remark: (1) Normal condition (2) Overcharge voltage condition (3) Overdischarge voltage condition

2. Overdischarge Current and Load Short detection

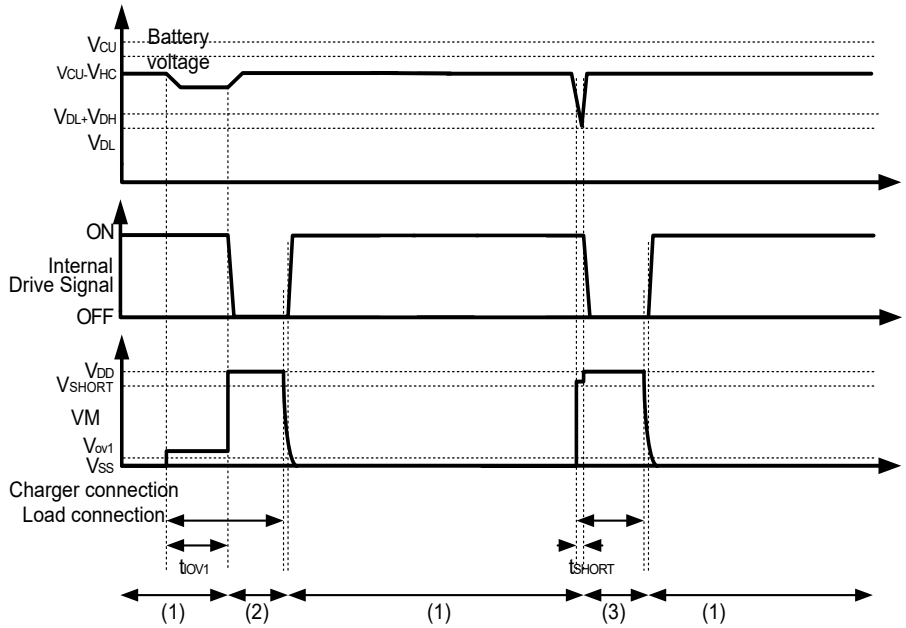


Figure4-2 Overdischarge Current and Short Detection

Remark: (1) Normal condition (2) Overcharge voltage condition (3) Overdischarge voltage condition

3. Abnormal Charger Detection

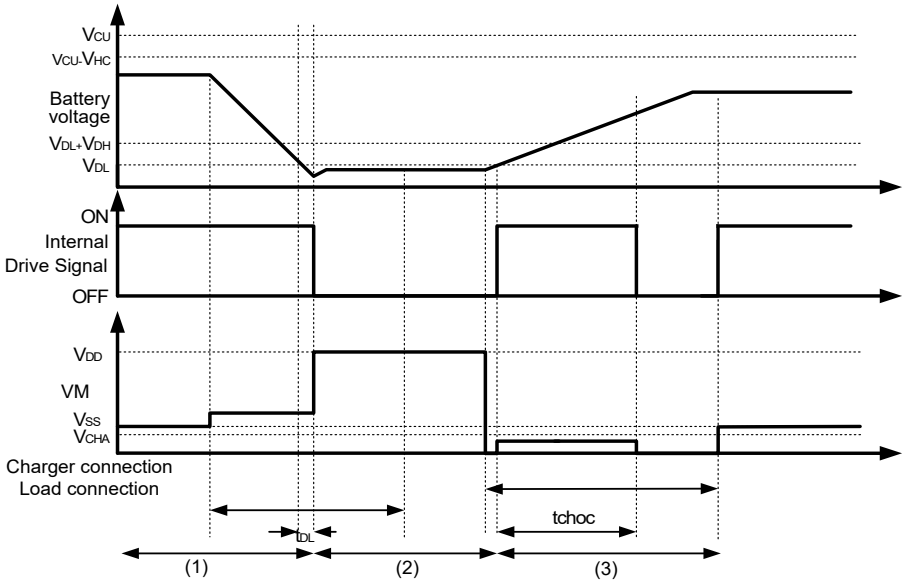


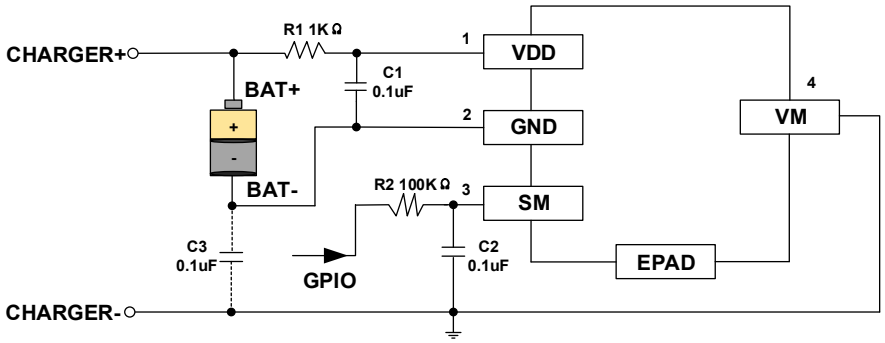
Figure4-3 Abnormal Charger Detection

Remark: (1) Normal condition (2) Overdischarge voltage condition (3) Overcharge voltage condition

TYPICAL APPLICATION

As shown in Figure 5, the current path which must be kept as short as possible. For thermal management, ensure that these trace widths are adequate. C is a decoupling ca pacitor which should be placed as close as possible to XBL6021-SM SERIES.

If add one 0.1uF capacitor between VM pin and GND pin closely, the system ESD level and anti-interference capability of circuit will improve greatly.



(Suggestion: Connect EPAD pin with GND)

Figure 5 XBL6021-SM SERIES in a Typical Battery Protection Circuit

Symbol	Typ	Value range	Unit
R1	1	0.47~2	KΩ
R2	100	50~150	KΩ
C1	0.1	0.1~1	μF
C2	0.1	0.047~0.1	μF
C3	0.1	-	μF

Remark:
1.The above parameters may be changed without notice;
2.The schematic diagram and parameters of the IC are not used as the basis to ensure the operation of the circuit. Please conduct full measurement on the actual application circuit before setting the parameters.
3.R2 and C2 affect the time to enter SM mode.

Precautions

• Pay attention to the operating conditions for input/output voltage and load current so that the power loss in XBL6021-SM SERIES does not exceed the power dissipation of the package.
• Do not apply an electrostatic discharge to this XBL6021-SM SERIES that exceeds the performance ratings of the built-in electrostatic protection circuit.

Description of shipping patterns

Entering shipping mode:
1.If V_{SM} is greater than VsmH, and Tsm is guaranteed to be the maximum time;
2.After the main switch is disconnected, the VM voltage is increased for 3 seconds and the voltage continues to be greater than 2V;
There are two ways to exit SM mode:
1. Short circuit the two pins of VM and GND;
2. Plug in the charger again.

APPLIED MEASUREMENT METHOD

(1).Overcharge characteristic test method:

a. According to the figure6-1, connect the power supply DC1 to the B + and GND pins of the system board and set the voltage to about 3.6V. Connect the power supply from GND to VM to DC2 power supply and set 100mV current limiting 10mA. Observe the waveform.

b. Adjust the power supply voltage V1 and increase it by 0.001V until the output level of VM pin changes from 0 to negative (-100mV). Record the overcharge protection voltage and measure the protection delay.

c. Adjust the power supply voltage V1 to decrease by 0.001V until the output voltage of VM pin is recovered from negative (-100mV) to 0 level, and record the overcharge recovery voltage.

(2).Over discharge characteristic test method:

a. According to the figure6-2, connect the power supply DC1 to the B + and GND pins of the system board and set the voltage to about 3.6V. Connect the DC2 power supply from VM to GND, set the 100mV current limiting 10mA, and observe the waveform.

b. Adjust the power supply voltage V1 and decrease it by 0.001V until the output level of VM pin changes from 0 to positive (100mV). Record the overdischarge protection voltage and measure the protection delay.

c. Adjust the power supply voltage V1 to increase by 0.001 V until the output voltage of VM pin is restored from positive (100 mV) to 0 level, and record the overdischarge recovery voltage.

(3).Discharge over current test method:

a. According to the figure6-3, connect the DC1 power supply to the B + and GND pins of the system board and set the voltage to about 3.0V/3.6V/4.2V. Connect the electronic load from B + to VM and observe the waveform.

b. Adjust the electronic load increase it by 1mA step, detect that the current from B + to VM is turned off and meet the delay standard (about 10ms), and record the discharge delay time.

(4).Charging over current test method:

a. According to the figure6-4, connect the DC1 power supply to the B + and GND pins of the system board and set the voltage to about 3.0V/3.6V/4.2V, and load DC2 power supply from GND to VM.

b. Adjust the current limiting value of DC2 power supply to increase by 1mA step, detect that the current from GND to VM is turned off and meet the delay standard(about 10ms), and record the charging over-current delay time.

(5).Iq test method:

a. As shown in the figure6-5, connect the positive pole of DC1 to B +, and the negative pole to GND, and set the voltage to 3.6V;

b. VM grounding, record the current passing through DC1 (Iq).

(6).Isd test method:

a. As shown in the figure6-6, connect the positive pole of DC1 to B + and the negative pole to GND, and set the voltage to 2V;

b. VM is suspended and the current passing through DC1 is recorded as Isd.

SCHEMATIC DIAGRAM OF TEST METHOD

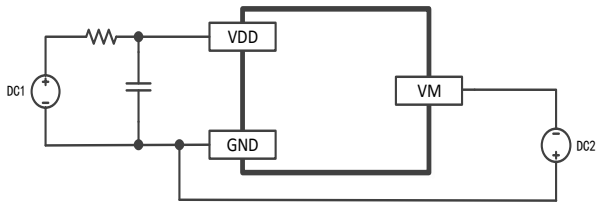


Figure6-1

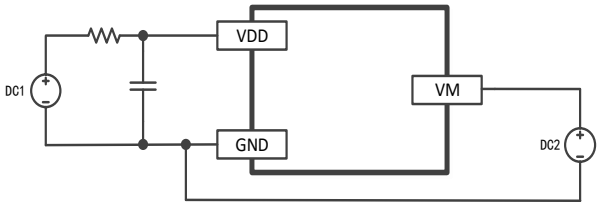


Figure6-2

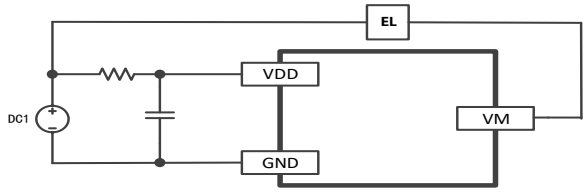


Figure6-3

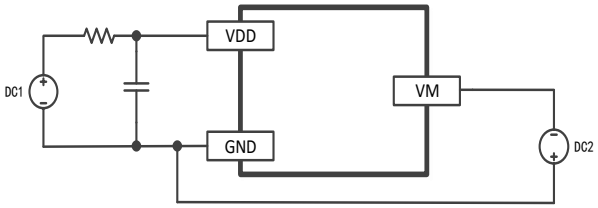


Figure6-4

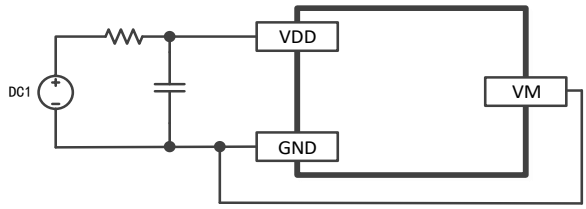


Figure6-5

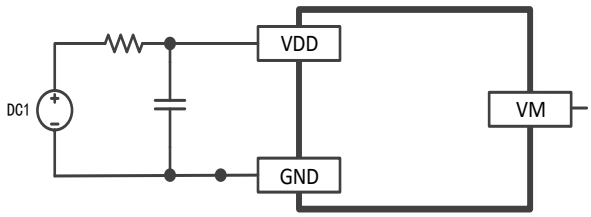
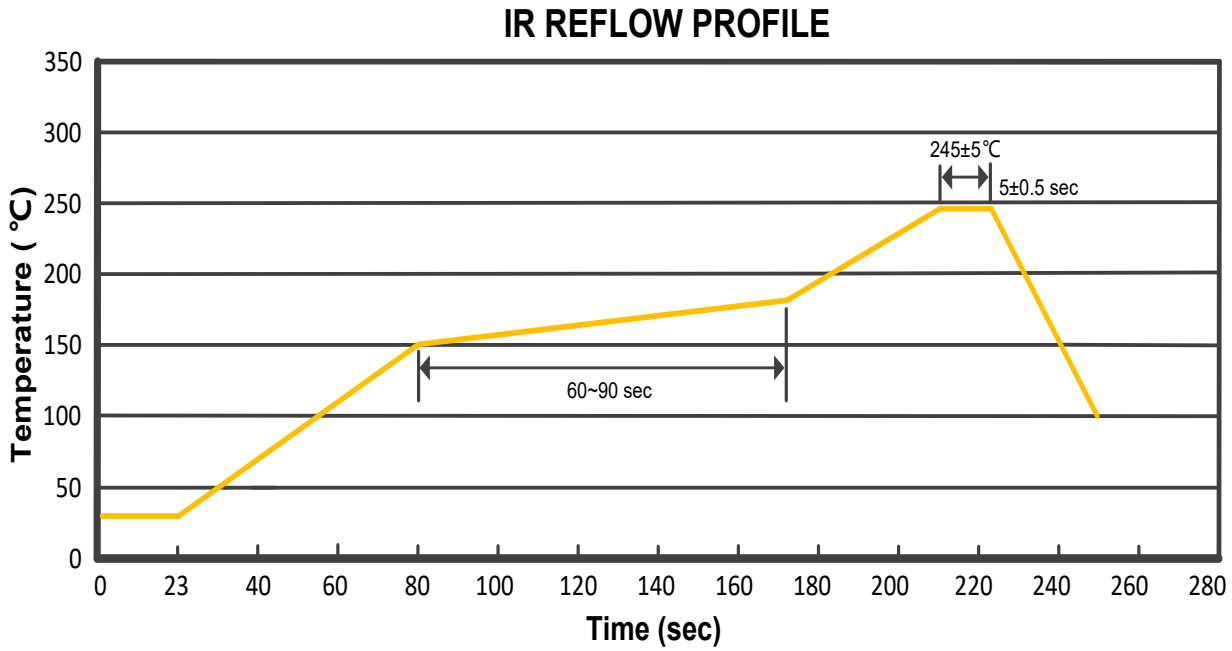


Figure6-6

Solderability Curve of Lead-Free Reflow Soldering (applicable to SMT tube)

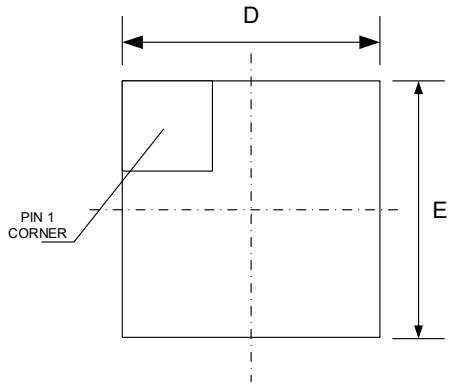


Explain:
1.Preheating temperature 25~150℃, duration 60~90sec;
2.Peak temperature 245 ± 5 ℃, duration 5 ± 0.5sec;
3.Cooling rate of welding process is 2~10℃/sec.

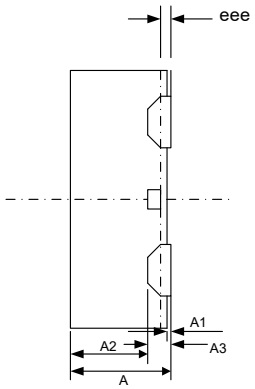
Resistance to welding heat conditions

Temperature: 270±5℃; Time:10±1sec

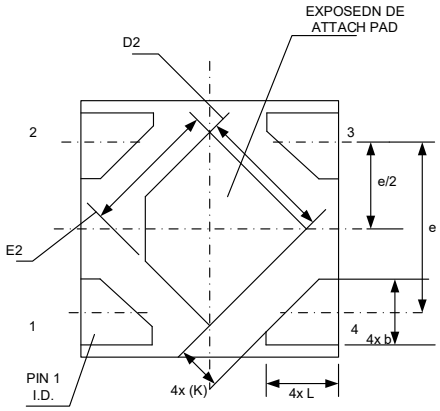
PACKAGE OUTLINE(DFN1x1-4)



TOP VIEW

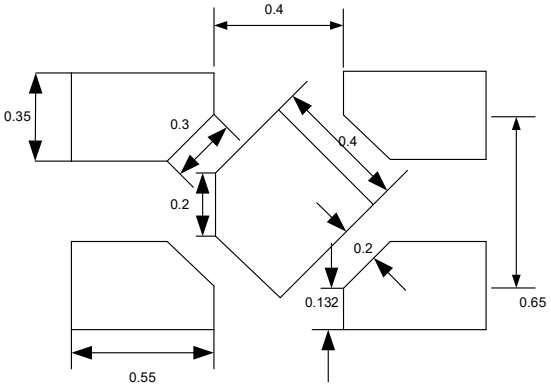


SIDE VIEW



BOTTOM VIEW

RECOMMENDED LAND PATTERN uint (mm)



	SYMBOL	NOM
TOTAL THICKNESS	A	0.37
STAND OFF	A1	0.02
MOLD THICKNESS	A2	0.27
L/F THICKNESS	A3	0.102REF
LEAD WIDTH	b	0.23
BODY SIZE	D	1BSC
	E	1BSC
LEAD PITCH	e	0.65BSC
EP SIZE	D2	0.48
	E2	0.48
LEAD LENGTH	L	0.25
Lead TIP TO EXPOSED PAD EDGE	K	0.21REF
COPLANARITY	eee	0.05

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