**[Xilinx® Zynq® 7000 series (XC7Z015) Power Solution, 8W - Reference Design](http://www.ti.com/tool/PMP10601?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 22 MAR 2017

**Description**

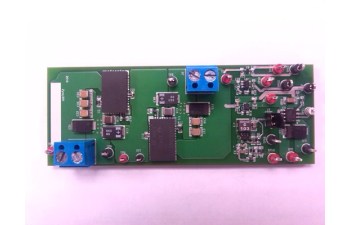
The PMP10601 reference design provides all the power supply rails necessary to power Xilinx® Zynq® 7000 series (XC7Z015)  FPGA.   This design uses several LMZ3 series modules, LDOs, and a DDR termination regulator to provide all the necessary rails to power the FPGA.  It also (...)

**Key Features**

* Provides all the power supply rails needed for a Xilinx® Zynq® 7000 series (XC7Z015)
* Design optimized to support a 12V input
* On board power up and power down sequencing
* Supports DDR3 memory device
* Module design for ease of use

**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidrcm6)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidrcm7)
* [Technical Reference](http://www.ti.com/lit/pdf/tidu745)
* [Gerber Files](http://www.ti.com/lit/zip/tidc883)
* **TI Devices**
* [LM3880](http://www.ti.com/tool/PMP10601?keyMatch=zynq&tisearch=tidesigns#tiDevice)
* [LMZ31503](http://www.ti.com/tool/PMP10601?keyMatch=zynq&tisearch=tidesigns#tiDevice)
* [LMZ31506](http://www.ti.com/tool/PMP10601?keyMatch=zynq&tisearch=tidesigns#tiDevice)
* [LP2998](http://www.ti.com/tool/PMP10601?keyMatch=zynq&tisearch=tidesigns#tiDevice)
* [LP3991](http://www.ti.com/tool/PMP10601?keyMatch=zynq&tisearch=tidesigns#tiDevice)
* [More](http://www.ti.com/tool/PMP10601?keyMatch=zynq&tisearch=tidesigns#tiDevice)



**Design Parameters**

|  | **Vin (V) (Min)**  **Vin (V) (Min)** | **Vin (V) (Max)**  **Vin (V) (Max)** | **Vout (V) (Nom)**  **Vout (V) (Nom)** | **Iout (A) (Max)**  **Iout (A) (Max)** | **Output Power (W)**  **Output Power (W)** | **Isolated/Non-Isolated**  **Isolated/Non-Isolated** | **Input Type**  **Input Type** | **Topology**  **Topology** | **Designed for**  **Designed for** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PMP10601.1 (Output Voltage 1) | 10.8 | 13.2 | 1 | 6 | 6 | Non-Isolated | DC | Buck- Integrated Switch | FPGA |
| PMP10601.2 (Output Voltage 2) | 10.8 | 13.2 | 1.8 | 2 | 3.6 | Non-Isolated | DC | Buck- Integrated Switch | FPGA |

**[Xilinx Zynq 7000 Series (XC7Z045) 20W Reference Design](http://www.ti.com/tool/PMP10613?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 03 MAR 2016

**Description**

The PMP10613 reference design provides all the power supply rails necessary to power Xilinx® Zynq® 7000 series (XC7Z045)  FPGA.   This design uses several LMZ3 series modules, LDOs, and a DDR termination regulator to provide all the necessary rails to power the FPGA.  It (...)

**Key Features**

* Provides all the power supply rails needed for a Xilinx® Zynq® 7000 series (XC7Z045)
* Design optimized to support 12V input
* On board power up and power down sequencing
* Supports DDR3 memory device
* Module design for ease of use

**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidreq4)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidreq5)
* [Technical Reference](javascript:refDesignKeyword('technicalReferencesimulation_2','downloadMultipletechnicalReference_2','technicalReferencesimulationdiv_2'))
* [CAD Files](http://www.ti.com/lit/zip/tidreq6)
* [Gerber Files](http://www.ti.com/lit/zip/tidca96)
* **TI Devices**
* [LM3880](http://www.ti.com/tool/PMP10613?keyMatch=zynq&tisearch=tidesigns#tiDevice)
* [LMZ31503](http://www.ti.com/tool/PMP10613?keyMatch=zynq&tisearch=tidesigns#tiDevice)

* [LMZ31520](http://www.ti.com/tool/PMP10613?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [LP2998](http://www.ti.com/tool/PMP10613?keyMatch=zynq&tisearch=tidesigns#tiDevice)

* [LP3892](http://www.ti.com/tool/PMP10613?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [More](http://www.ti.com/tool/PMP10613?keyMatch=zynq&tisearch=tidesigns#tiDevice)



**Design Parameters**

|  | **Vin (V) (Min)**  **Vin (V) (Min)** | **Vin (V) (Max)**  **Vin (V) (Max)** | **Vout (V) (Nom)**  **Vout (V) (Nom)** | **Iout (A) (Max)**  **Iout (A) (Max)** | **Output Power (W)**  **Output Power (W)** | **Isolated/Non-Isolated**  **Isolated/Non-Isolated** | **Input Type**  **Input Type** | **Topology**  **Topology** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PMP10613.1 (Output Voltage 1) | 10.8 | 13.2 | 1 | 17 | 17 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP10613.2 (Output Voltage 2) | 10.8 | 13.2 | 1.8 | 3 | 5.4 | Non-Isolated | DC | Buck- Integrated Switch |

**[Power Solution for Xilinx FPGA Zynq 7 (1.8V@0.15A)](http://www.ti.com/tool/PMP8251?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

Updated: 03 MAR 2016

**Description**

This reference design featuring multiple of the TPS54325 and other TI power devices, is a complete power solution for Xilinx Zynq FPGA. From 12V input, this reference solution provides all the power rails required by Zynq FPGA including DDR3 memory.

**Key Features**

* Provides all the power rails needed for Zynq FPGA
* Operates with wide input voltage range 5V to 12V
* Very high density PCB design saving board area
* Supports DDR3 memory device
* Optimum combination of switching regulators and LDO provides the best power distribution tree
* This design is tested and ready to (...)

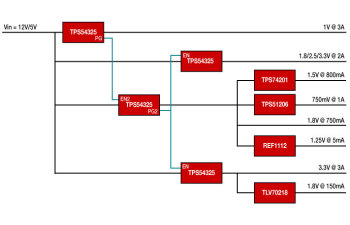
**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/slvraz6)
* [Bill of Materials](http://www.ti.com/lit/pdf/slvraz5)
* [Technical Reference](javascript:refDesignKeyword('technicalReferencesimulation_3','downloadMultipletechnicalReference_3','technicalReferencesimulationdiv_3'))
* [Layer plots (or PCB layout)](http://www.ti.com/lit/pdf/slvu764)
* [Gerber Files](http://www.ti.com/lit/zip/slvc440)
* **TI Devices**

* [REF1112](http://www.ti.com/tool/PMP8251?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [TLV702](http://www.ti.com/tool/PMP8251?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [TPS51206](http://www.ti.com/tool/PMP8251?keyMatch=zynq&tisearch=tidesigns#tiDevice)

* [TPS54325](http://www.ti.com/tool/PMP8251?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)



**Design Parameters**

|  | **Vin (V) (Min)**  **Vin (V) (Min)** | **Vin (V) (Max)**  **Vin (V) (Max)** | **Vout (V) (Nom)**  **Vout (V) (Nom)** | **Iout (A) (Max)**  **Iout (A) (Max)** | **Output Power (W)**  **Output Power (W)** | **Isolated/Non-Isolated**  **Isolated/Non-Isolated** | **Input Type**  **Input Type** | **Topology**  **Topology** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PMP8251.1 (Output Voltage 1) | 12 | 12 | 1 | 3 | 3 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP8251.2 (Output Voltage 2) | 12 | 12 | 1.8 | 2 | 3.6 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP8251.3 (Output Voltage 3) | 12 | 12 | 2.5 | 2 | 5 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP8251.4 (Output Voltage 4) | 12 | 12 | 3.3 | 2 | 6.6 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP8251.5 (Output Voltage 5) | 12 | 12 | 1.5 | .8 | 1.2 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP8251.6 (Output Voltage 6) | 12 | 12 | .75 | 1 | .75 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP8251.7 (Output Voltage 7) | 12 | 12 | 1.8 | .75 | 1.35 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP8251.8 (Output Voltage 8) | 12 | 12 | 3.3 | 3 | 9.9 | Non-Isolated | DC | Buck- Integrated Switch |
| PMP8251.9 (Output Voltage 9) | 12 | 12 | 1.8 | .15 | .27 | Non-Isolated | DC | Buck- Integrated Switch |

**[Multi-output Multi-buck 20W Power Supply for Xilinx Zynq FPGA Applications Reference Design](http://www.ti.com/tool/PMP9335?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 03 MAR 2016

**Description**

PMP9335 is designed for Xilinx Zynq FPGA applications utilizing the TPS84A20 and TPS84320. This design uses an external timer to synchronize the switching frequency to 300 kHz. It also employs a controlled power up and power down sequence.

**Key Features**

* Designed for Xilinx Zynq FPGA applications
* Compact solution and easy-to-use design with TPS84A20 and  TPS84320 buck regulator modules
* Controlled power up and power down sequence
* To be used as a “plug in” module, the use of extra bulk capacitance on external pcb is assumed

**Available resources**

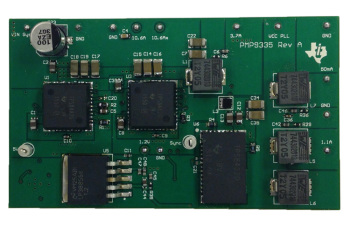
* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidrhk6)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidrhk7)
* [Technical Reference](http://www.ti.com/lit/pdf/tiduas5)
* [Layer plots (or PCB layout)](http://www.ti.com/lit/pdf/tidrhk9)
* [Assembly Drawings](http://www.ti.com/lit/pdf/tidrhk8)
* [CAD Files](http://www.ti.com/lit/zip/tidrhl0)
* [Gerber Files](http://www.ti.com/lit/zip/tidcb24)
* **TI Devices**

* [LMC555](http://www.ti.com/tool/PMP9335?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LMC555-MD8](http://www.ti.com/tool/PMP9335?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [LP2951](http://www.ti.com/tool/PMP9335?keyMatch=zynq&tisearch=tidesigns#tiDevice)

* [LP38855](http://www.ti.com/tool/PMP9335?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [TPS84320](http://www.ti.com/tool/PMP9335?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [More](http://www.ti.com/tool/PMP9335?keyMatch=zynq&tisearch=tidesigns#tiDevice)



**Design Parameters**

|  | **Vin (V) (Min)**  **Vin (V) (Min)** | **Vin (V) (Max)**  **Vin (V) (Max)** | **Vout (V) (Nom)**  **Vout (V) (Nom)** | **Iout (A) (Max)**  **Iout (A) (Max)** | **Output Power (W)**  **Output Power (W)** | **Isolated/Non-Isolated**  **Isolated/Non-Isolated** | **Input Type**  **Input Type** | **Topology**  **Topology** | **Designed for**  **Designed for** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PMP9335.1 (Output Voltage 1) | 12 | 12 | 1 | 3.7 | 3.7 | Non-Isolated | DC | Buck- Synchronous |  |
| PMP9335.2 (Output Voltage 2) | 12 | 12 | 1.8 | 3.7 | 6.66 | Non-Isolated | DC | Buck- Synchronous |  |
| PMP9335.3 (Output Voltage 3) | 12 | 12 | 1 | 10.6 | 10.6 | Non-Isolated | DC | Buck- Synchronous | FPGA |

**[Xilinx® Zynq®7000 series (XC7Z015) Power Solution, 5W - Reference Design](http://www.ti.com/tool/PMP10600?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 03 MAR 2016

**Description**

The PMP10600.1 reference design provides all the power supply rails necessary to power Xilinx® Zynq® 7000 series (XC7Z015) FPGA.   This design uses several LMZ3 series modules, LDOs, and a DDR termination regulator.  It also features one LM3880 for power up and power down (...)

**Key Features**

* Provides all the power supply rails needed for a Xilinx® Zynq® 7000 series (XC7Z015)
* Design optimized to support a 12V input
* On board power up and power down sequencing
* Supports DDR3 memory device
* Module design for ease of use

**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidrck2)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidrck3)
* [Technical Reference](http://www.ti.com/lit/pdf/tidu738)
* [Gerber Files](http://www.ti.com/lit/zip/tidc870)
* **TI Devices**

* [LM3880](http://www.ti.com/tool/PMP10600?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [LMZ31503](http://www.ti.com/tool/PMP10600?keyMatch=zynq&tisearch=tidesigns#tiDevice)

* [LP2998](http://www.ti.com/tool/PMP10600?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LP3991](http://www.ti.com/tool/PMP10600?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [TPS560200](http://www.ti.com/tool/PMP10600?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [More](http://www.ti.com/tool/PMP10600?keyMatch=zynq&tisearch=tidesigns#tiDevice)



**Design Parameters**

|  | **Vin (V) (Min)**  **Vin (V) (Min)** | **Vin (V) (Max)**  **Vin (V) (Max)** | **Vout (V) (Nom)**  **Vout (V) (Nom)** | **Iout (A) (Max)**  **Iout (A) (Max)** | **Output Power (W)**  **Output Power (W)** | **Isolated/Non-Isolated**  **Isolated/Non-Isolated** | **Input Type**  **Input Type** | **Topology**  **Topology** | **Designed for**  **Designed for** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PMP10600.1 (Output Voltage 1) | 10.8 | 13.2 | 1 | 3 | 3 | Non-Isolated | DC | Buck- Integrated Switch | FPGA |
| PMP10600.2 (Output Voltage 2) | 10.8 | 13.2 | 1.8 | 1.3 | 2.34 | Non-Isolated | DC | Buck- Integrated Switch | FPGA |

**[30A PMBus Reference Design for Xilinx Zynq Ultrascale+ ZU9EG MPSoC Core Rail for Base Stations](http://www.ti.com/tool/PMP11328?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 16 NOV 2015

**Description**

The PMP11328 is a high power density 30A PMBus power supply meeting the Xilinx Ultrascale+ ZU9EG FPGA core rail power specifications for Base Station Remote Radio Unit (RRU) applications. The power supply regulates 0.85V for the core rail at 25A in 55mm x 40mm total power supply PCB area. PMBus (...)

**Key Features**

* 12V input, 0.85V/25A PoL  in 40mm x 55mm PCB area
* High efficiency >82% at 0.85V/25A, 500kHz
* Adaptive Voltage Scaling (AVS), Voltage Margining, and Output Voltage/Current/Temperature monitoring through PMBus and TI's Fusion GUI
* 4W Power Loss at 12VIN, 0.85V/25A
* 12mV overshoot/undershoot during a 8A load (...)

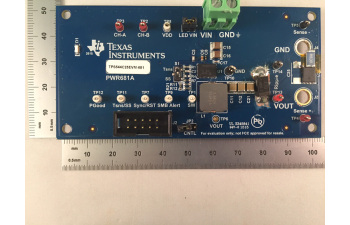
**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidri14)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidri15)
* [Technical Reference](http://www.ti.com/lit/pdf/tiduau9)

* [Layer plots (or PCB layout)](http://www.ti.com/lit/pdf/tidri17" \t "_blank)

* [Assembly Drawings](http://www.ti.com/lit/pdf/tidri16" \t "_blank)
* [Gerber Files](http://www.ti.com/lit/zip/tidcb67)
* **TI Devices**

* [TPS544C25](http://www.ti.com/tool/PMP11328?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)



**Design Parameters**

|  | **Designed for**  **Designed for** |
| --- | --- |
| PMP11328.1 (Output Voltage1) | FPGA |

**[Xilinx Zynq 7000 Series 5W Small Efficient Low-Noise Power Solution Reference Design](http://www.ti.com/tool/TIDA-00574?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 26 JUN 2015

**Description**

The TIDA-00574 shows small solution size and high curren density & low noise power solution.  It supports internal sequencing and high output voltage accuracy.

**Key Features**

* Small solution size
* High efficiency across load
* Internal power sequencing
* Multi channel configurability
* Low noise, high PSRR LDO

**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidrfm7)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidrfm8)

* [Reference Guide](http://www.ti.com/lit/pdf/tidua66" \t "_blank)
* [Gerber Files](http://www.ti.com/lit/zip/tidcak2)
* **TI Devices**

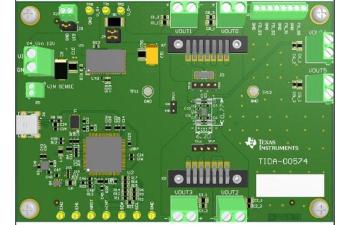
* [LM4132](http://www.ti.com/tool/TIDA-00574?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LMZ31503](http://www.ti.com/tool/TIDA-00574?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LP3990](http://www.ti.com/tool/TIDA-00574?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LP3996](http://www.ti.com/tool/TIDA-00574?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LP5907](http://www.ti.com/tool/TIDA-00574?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [More](http://www.ti.com/tool/TIDA-00574?keyMatch=zynq&tisearch=tidesigns#tiDevice)



**Design Parameters**

|  | **Designed for**  **Designed for** |
| --- | --- |
| TIDA-00574.1 (Output Voltage1) | FPGA |

**[Powering Xilinx Zynq 7015 FPGA with TPS65911 Power Management IC Reference Design](http://www.ti.com/tool/TIDA-00551?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 26 MAR 2015

**Description**

This TPS65911 based reference design is a compact, integrated power solution for Xilinx® Zynq® 7015 SoC/FPGAs (out of the Zynq® 7000 series family of products). This design showcases TPS65911 as an all-in-one PMIC solution capable of supplying eight rails to power the Zynq® 7015 (...)

**Key Features**

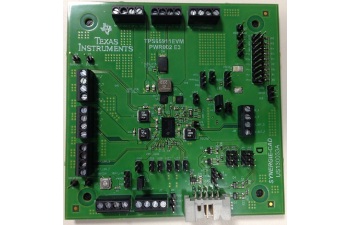
* TPS65911 comes equipped with 1 controller, 3 DCDC converters with integrated FETs, and 8 adjustable general purpose LDOs
* Provides 8 supply rails to the Zynq 7015 in a compact 2.095 in2 area (includes passive components)
* Includes an integrated, programmable sequencer for flexible power-up sequencing
* The (...)

**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidrdo2)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidrdo3)
* [Technical Reference](http://www.ti.com/lit/pdf/tidu872)

* [CAD Files](http://www.ti.com/lit/zip/tidrdo4" \t "_blank)
* **TI Devices**

* [TPS65911](http://www.ti.com/tool/TIDA-00551?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)



**Design Parameters**

|  | **Designed for**  **Designed for** |
| --- | --- |
| TIDA-00551.1 (Output Voltage1) | FPGA |

**[Power Reference Design for Xilinx® Zynq®-7000](http://www.ti.com/tool/PMP7877?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 27 JAN 2015

**Description**

The PMP7877 reference design provides all the rails necessary to power a Xilinx® Zynq®-7000 series SoC.  It operates from an input voltage range of 10.8Vin to 13.2Vin and has seven regulated outputs: 1Vout @ 5A, 1.8Vout @ 2.5A, 1.5Vout @ 6A, 3.3Vout @ 5A, 3.3Vout @ 5A, 5Vout @ 2A, and (...)

**Key Features**

• Provides all the power supply rails needed for a Xilinx® Zynq®-7000 series SoC  
• Design optimized to support a 12V input  
• On board power up and down sequencing  
• External clock frequency syncronization (500kHz)  
• Proven and tested design

**Available resources**

* [Schematic/Block Diagram](javascript:refDesignKeyword('schematicsimulation_9','downloadMultiplesimu_9','schematicdiv_9'))
* [Bill of Materials](javascript:refDesignKeyword('bomsimulation_9','downloadMultiplebom_9','bomsimulationdiv_9'))
* [Technical Reference](http://www.ti.com/lit/pdf/snvu252)
* [Gerber Files](http://www.ti.com/lit/zip/snvc087)
* **TI Devices**

* [LM21305](http://www.ti.com/tool/PMP7877?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

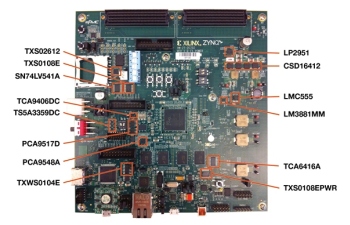
* [LM25119](http://www.ti.com/tool/PMP7877?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LM3881](http://www.ti.com/tool/PMP7877?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LMR12020](http://www.ti.com/tool/PMP7877?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LP2951](http://www.ti.com/tool/PMP7877?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [More](http://www.ti.com/tool/PMP7877?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)



**Design Parameters**

|  | **Vin (V) (Min)**  **Vin (V) (Min)** | **Vin (V) (Max)**  **Vin (V) (Max)** | **Vout (V) (Nom)**  **Vout (V) (Nom)** | **Iout (A) (Max)**  **Iout (A) (Max)** | **Output Power (W)**  **Output Power (W)** | **Isolated/Non-Isolated**  **Isolated/Non-Isolated** | **Input Type**  **Input Type** | **Topology**  **Topology** | **Designed for**  **Designed for** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PMP7877.1 (Output Voltage 1) | 10.8 | 13.2 | 1 | 5 | 5 | Non-Isolated | DC | Buck- Synchronous |  |
| PMP7877.2 (Output Voltage 2) | 10.8 | 13.2 | 1.8 | 2.5 | 4.5 | Non-Isolated | DC | Buck- Synchronous |  |
| PMP7877.3 (Output Voltage 3) | 10.8 | 13.2 | 1.5 | 6 | 9 | Non-Isolated | DC | Buck- Synchronous |  |
| PMP7877.4 (Output Voltage 4) | 10.8 | 13.2 | 3.3 | 5 | 16.5 | Non-Isolated | DC | Buck- Synchronous |  |
| PMP7877.5 (Output Voltage 5) | 10.8 | 13.2 | 3.3 | 5 | 16.5 | Non-Isolated | DC | Buck- Synchronous |  |
| PMP7877.6 (Output Voltage 6) | 10.8 | 13.2 | 5 | 2 | 10 | Non-Isolated | DC | Buck- Synchronous |  |
| PMP7877.7 (Output Voltage 7) | 10.8 | 13.2 | .75 | 1 | .75 | Non-Isolated | DC | Linear Regulator |  |
| PMP7877.8 (Output Voltage 8) | 10.8 | 14.4 | 3.3 | 12.45 | 5 | 62.25 | Non-Isolated | DC | Buck | FPGA |

**[Automotive ADAS Power Design Optimized for Xilinx® Zynq® 7020 SoC](http://www.ti.com/tool/TIDA-00390?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 15 JAN 2015

**Description**

The TIDA-00390 design is an optimized power solution for Xilinx® Zynq® 7020 FPGA/SoC (out of the Zynq® 7000 series family of products). It targets ADAS applications where customers opt to use FPGA instead of Multicore DSP or MPU.  This design runs from a single intermediate 3.3V or (...)

**Key Features**

* Provides all the power supply rails for a Xilinx® Zynq® 7020 based ADAS system
* Individual High efficiency switching regulators and LDO for best layout and IC placement flexibility and heat spreading on the board
* All switching regulators operate at >2MHz for optimized size and cost of external (...)

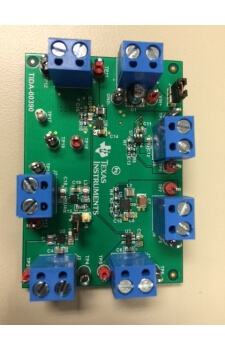
**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidrcl8)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidrcl9)
* [Technical Reference](javascript:refDesignKeyword('technicalReferencesimulation_10','downloadMultipletechnicalReference_10','technicalReferencesimulationdiv_10'))

* [Gerber Files](http://www.ti.com/lit/zip/tidc878" \t "_blank)
* **TI Devices**
* [LM3880-Q1](http://www.ti.com/tool/TIDA-00390?keyMatch=zynq&tisearch=tidesigns#tiDevice)
* [LP2998-Q1](http://www.ti.com/tool/TIDA-00390?keyMatch=zynq&tisearch=tidesigns#tiDevice)

* [TLV70018-Q1](http://www.ti.com/tool/TIDA-00390?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [TPS61240-Q1](http://www.ti.com/tool/TIDA-00390?keyMatch=zynq&tisearch=tidesigns#tiDevice)

* [TPS62090-Q1](http://www.ti.com/tool/TIDA-00390?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)
* [More](http://www.ti.com/tool/TIDA-00390?keyMatch=zynq&tisearch=tidesigns#tiDevice)



**Design Parameters**

|  | **Designed for**  **Designed for** |
| --- | --- |
| TIDA-00390.1 (Output Voltage1) | FPGA |

**[Automotive ADAS Power Design Optimized for Xilinx® Zynq® 7010 SoC](http://www.ti.com/tool/TIDA-00389?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

http://www.ti.com/assets/images/TIDesignsLogo.png   
Updated: 06 JAN 2015

**Description**

The TIDA-00389 design is an optimized power solution for Xilinx® Zynq® 7010 FPGA/SoC (out of the Zynq® 7000 series family of products). It targets ADAS applications where customers opt to use FPGA instead of Multicore DSP or MPU.  This design runs from a single intermediate 3.3V or (...)

**Key Features**

* Provides all the power supply rails for a Xilinx® Zynq® 7010 based  ADAS system
* Individual High efficiency switching regulators for low power consumption and heat generation
* All switching regulators operate at >2MHz for optimized size and cost of external components and to reduce noise in the AM radio (...)

**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/tidrce1)
* [Bill of Materials](http://www.ti.com/lit/pdf/tidrce2)

* [Software](http://www.ti.com/lit/zip/tidc844" \t "_blank)
* [Technical Reference](javascript:refDesignKeyword('technicalReferencesimulation_11','downloadMultipletechnicalReference_11','technicalReferencesimulationdiv_11'))
* **TI Devices**

* [LM26480-Q1](http://www.ti.com/tool/TIDA-00389?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

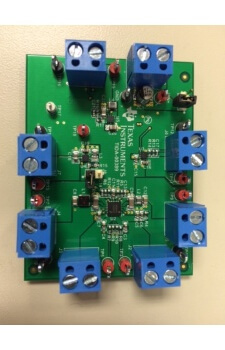
* [LM3880-Q1](http://www.ti.com/tool/TIDA-00389?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [LP2998-Q1](http://www.ti.com/tool/TIDA-00389?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [TPS61240-Q1](http://www.ti.com/tool/TIDA-00389?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [TPS62260-Q1](http://www.ti.com/tool/TIDA-00389?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [More](http://www.ti.com/tool/TIDA-00389?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)



**[Analog Solution for Zynq](http://www.ti.com/tool/PMP7975?keyMatch=zynq&tisearch=tidesigns" \t "_blank)**

Updated: 16 DEC 2014

**Description**

Xilinx chose TI as the power solution vendor to power Zynq FPGA (along with other analog solution from TI). You will find Schematic and bill of material fo the solution Xilinx used on the development kits.

**Available resources**

* [Schematic/Block Diagram](http://www.ti.com/lit/pdf/slura88a" \t "_blank)

* [Bill of Materials](http://www.ti.com/lit/pdf/slura89a" \t "_blank)

* [Technical Reference](http://www.ti.com/lit/pdf/sluub46" \t "_blank)

* [User's Guide](http://www.ti.com/lit/pdf/slyu019a" \t "_blank)
* **TI Devices**

* [LMZ12002](http://www.ti.com/tool/PMP7975?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [PTD08D210W](http://www.ti.com/tool/PMP7975?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [SN74LV541A](http://www.ti.com/tool/PMP7975?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [TPS51200](http://www.ti.com/tool/PMP7975?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)

* [UCD9248](http://www.ti.com/tool/PMP7975?keyMatch=zynq&tisearch=tidesigns" \l "tiDevice" \t "_blank)



**Design Parameters**

|  | **Vin (V) (Min)**  **Vin (V) (Min)** | **Vin (V) (Max)**  **Vin (V) (Max)** | **Vout (V) (Nom)**  **Vout (V) (Nom)** | **Iout (A) (Max)**  **Iout (A) (Max)** | **Output Power (W)**  **Output Power (W)** | **Isolated/Non-Isolated**  **Isolated/Non-Isolated** | **Input Type**  **Input Type** | **Topology**  **Topology** | **Designed for**  **Designed for** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PMP7975.1 (Output Voltage1) | 4.5 | 14 | 1 | 10 | 10 | Non-Isolated | DC | Buck- Synchronous | FPGA |