A New Three-Phase Power-Factor Correction (PFC) Scheme Using Two Single-Phase PFC Modules

Jaehong Hahn, *Student Member, IEEE*, Prasad N. Enjeti, *Fellow, IEEE*, and Ira J. Pitel, *Fellow, IEEE*

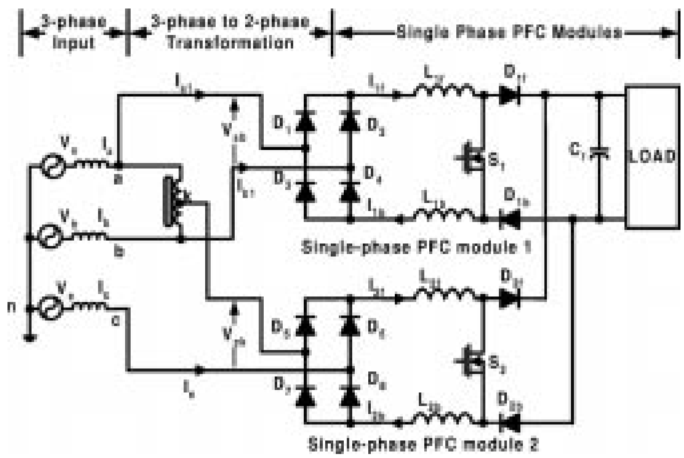
***Abstract*—In this paper, a new three-phase power-factor correction (PFC) scheme is proposed using two single-phase PFC modules. In this approach, the "three" phase input is first transformed to "two" phase by means of a 0.14-pu-rated autotransformer. Two standard single-phase PFC modules are then employed to process the "two" phase power to dc output. Split inductors and diodes are employed to limit interaction between the two PFC stages. Due to cascade operation of two PFC stages, low-frequency (120 Hz) ripple in the dc-link capacitor is cancelled. Detailed analysis and simulation results are presented. A 220-V 1.5-kVA design example along with experimental results is shown.**

***Index Terms*—Harmonics, power-factor correction, power quality.**

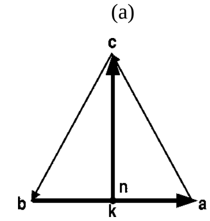
I. Introduction

THREE-PHASE switch-mode power supplies (SMPSs) employing diode-rectifier-type utility interface are widely used in telecommunications, data processing, and other industrial systems [1], [2]. The diode-rectifier-type utility interface generates lower order harmonics of the order 6k $\pm$ 1, i.e., 5, 7, 11, 13, etc. IEC 61 000-3-4 and IEEE 519-1992 detail acceptable limits [3], [4] of such nonlinear loads. Several approaches have been studied and summarized in [5]–[8] to improve the total harmonic distortion (THD). They are broadly categorized into two groups: 1) rectifier circuitry capable of producing low level of harmonic content or 2) conventional rectifier circuitry with additional filter. Three single-phase power-factor correction (PFC) stages for a three-phase system, a single-switch PFC with discontinuous mode (DCM) control, and a six-switch PWM rectifier can be considered in the first category. A single-switch PFC with DCM control suffers from high switch current rating and high electromagnetic interference (EMI) [6], [7]. A pulsewidth modulation (PWM) rectifier needs complicated measurements and feedback control [5].

This paper proposes a new three-phase PFC scheme using two standard single-phase PFC modules. "Two" phase is produced by means of a 0.14-pu-rated autotransformer from a "three" phase input. Two standard single-phase PFC modules are employed, one on each phase to process the power. Split inductors and diodes are used to limit interaction between the two PFC stages. The outputs of the two PFC modules are connected

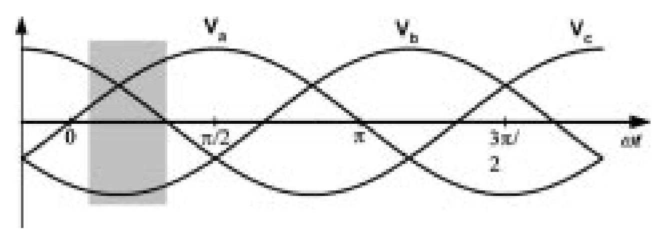


(a)

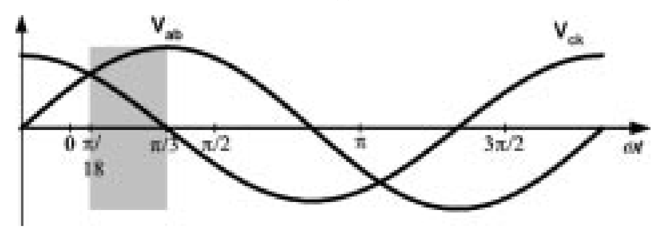


(b)

Fig. 1. Proposed three-phase PFC scheme using two single-phase PFC modules. (a) Topology of the proposed approach. (b) Vector diagram of the two phase.



(a)



(b)

Fig. 2. Input voltage waveforms and the interval $\pi/18 < \omega t < \pi/2$ considered in analysis. (a) Phase voltage. (b) Input voltages at each PFC.

Paper IPCSD 01–063, presented at the 2001 IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, March 4–8, and approved for publication in the IEEE Transactions on Industry Applications by the Industrial Power Converter Committee of the IEEE Industry Applications Society. Manuscript submitted for review March 1, 2001 and released for publication October 6, 2001.

J. Hahn and P. N. Enjeti are with the Power Electronics and Power Quality Laboratory, Department of Electrical Engineering, Texas A&M University, College Station, TX 77843-3128 USA (e-mail: jaehong@ee.tamu.edu; enjeti@ieee.org).

I. J. Pitel is with Magna-Power Electronics, Boonton, NJ 07005 USA (e-mail: i.pitel@ieee.org).

Publisher Item Identifier S 0093-9994(02)00605-9.

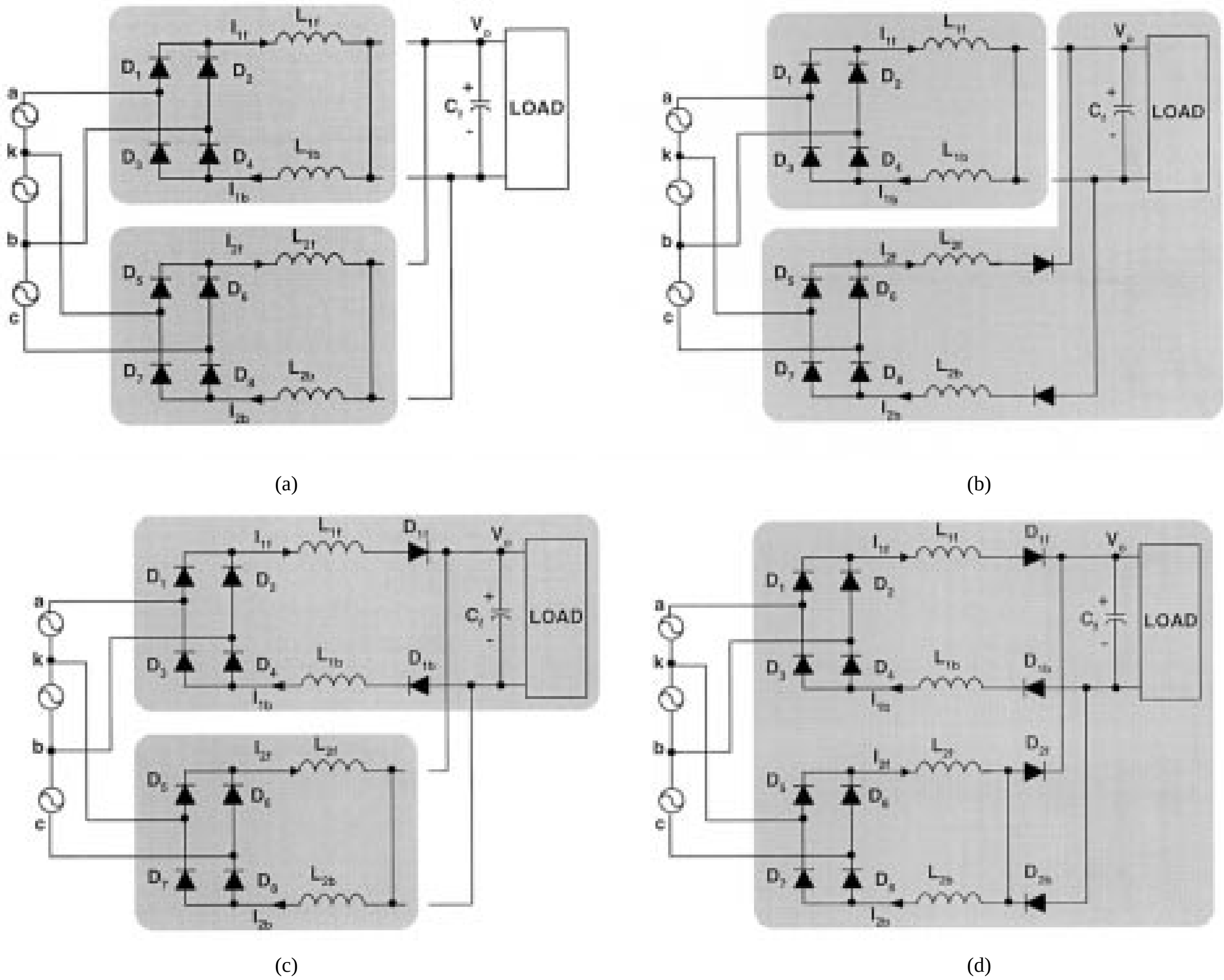


Fig. 3. Equivalent circuits at each switching period. (a) Equivalent circuit in which S_1 is on while S_2 is on. (b) Equivalent circuit in which S_1 is on while S_2 is off. (c) Equivalent circuit in which S_1 is off while S_2 is on. (d) Equivalent circuit in which S_1 and S_2 are off.

to the common dc output. Due to cascade operation of the two PFC stages, low-frequency (120 Hz) ripple components in the dc-link capacitor cancel each other. The advantages of the proposed scheme are as follows.

- The proposed approach is modular and employs two standard single-phase PFC modules. Input current waveforms are nearly sinusoidal at unity power factor and are in compliance with IEEE 519, IEC 1000-3, and IEC-6000-3-2 limits.
- In this scheme, the second-order harmonic current component in the dc-link capacitor is cancelled. This significantly reduces capacitor heating and improves its operating life.
- The voltampere (VA) rating of the autotransformer employed is low.
- The dc output is regulated and is immune to voltage sags and other power quality disturbances.

II. Proposed System

Fig. 1(a) shows the topology of the proposed approach. The three-phase input v_a, v_b, and v_c (120° phase shift) is first transformed to two phase v_{ab} and v_{ck} (90° phase shift) by means of a center-tapped autotransformer. From the vector diagram in Fig. 1(b), it is clear that voltage v_{ab} and v_{ck} are 90° apart.

Two single-phase boost PFC stages are connected to the "two" phase voltages v_{ab} and v_{ck}, as shown in Fig. 1(a). Single-phase PFC module 1 consists of a bridge rectifier, inductors L_{1f} and L_{1b}, and diodes D_{1f} and D_{1b}. Single-phase PFC module 2 consists of a bridge rectifier, inductors L_{2f} and L_{2b}, and diodes D_{2f} and D_{2b}. Split inductors and diodes are employed at the two PFC stages to limit interaction between the two when the output stages are combined [8].

Although $|V_{ab}| \neq |V_{ck}|$ [Fig. 1(b)], the two boost PFC stages are suitably controlled with different gains to supply one-half of the output power. This feature enables cancellation of low-frequency second-order harmonic current component in the capacitor.

A. Analysis

Fig. 2(a) shows the phase voltages. Single-phase PFC module 1 sees the voltage v_{ab} as in Fig. 2(b) and single-phase PFC module 2 sees the voltage v_{ck} in Fig. 2(b) via the autotransformer. Fig. 3 shows the possible equivalent circuits from the input to the output.

In the interval of $\pi/18 < \omega t < \pi/2$ (gray area in Fig. 2), the rectified output has the following relationship:

$$|v_{ab}| > |v_{ck}| \tag{1}$$

$$d_{ab} = 1 - \frac{|v_{ab}|}{V_o} \tag{2.a}$$

$$d_{ck} = 1 - \frac{|v_{ck}|}{V_o} \tag{2.b}$$

where d_{ab} and d_{ck} are the duty cycles of each converter.

When both S_1 and S_2 switches are on, there is no current path to the output and the two single-phase PFC modules work independently as in Fig. 3(a). Also, when one of the switches, i.e., S_1 or S_2 is off [the equivalent circuit is shown in Fig. 3(b) and (c)], the PFC modules operate independently. However, when both switches are off the two PFC modules are simultaneously connected to the output.

The equivalent circuit for this condition is shown in Fig. 3(d). For this equivalent circuit,

$$v_{ab} - L_{1f}\frac{di_{1f}}{dt} - V_o - L_{1b}\frac{di_{1b}}{dt} = 0 \tag{3.a}$$

$$v_{ck} - L_{2f}\frac{di_{2f}}{dt} - V_o - L_{2b}\frac{di_{2b}}{dt} = 0 \tag{3.b}$$

$$-\frac{v_{ab}}{2} + L_{1b}\frac{di_{1b}}{dt} - L_{2b}\frac{di_{2b}}{dt} = 0 \tag{3.c}$$

$$i_{1f} + i_{2f} - i_{1b} - i_{2b} = 0. \tag{3.d}$$

Assuming that $L = L_{1f} = L_{1b} = L_{2f} = L_{2b}$, the inductor current can be derived from (3.a)–(3.d).

$$\frac{di_{1f}}{dt} = \left(|v_{ab}| - \frac{|v_{ck}|}{2} - V_o\right)\frac{1}{2L} \tag{4.a}$$

$$\frac{di_{1b}}{dt} = \left(|v_{ab}| + \frac{|v_{ck}|}{2} - V_o\right)\frac{1}{2L} \tag{4.b}$$

$$\begin{aligned}\frac{di_{2f}}{dt} &= \left(|v_{ck}| + \frac{|v_{ck}|}{2} - V_o\right)\frac{1}{2L}\\ &= \left(\frac{3|v_{ck}|}{2} - V_o\right)\frac{1}{2L}\end{aligned} \tag{4.c}$$

$$\begin{aligned}\frac{di_{2b}}{dt} &= \left(|v_{ck}| - \frac{|v_{ck}|}{2} - V_o\right)\frac{1}{2L}\\ &= \left(\frac{|v_{ck}|}{2} - V_o\right)\frac{1}{2L}.\end{aligned} \tag{4.d}$$

Fig. 4 shows the inductor current waveforms for a switching period in the interval, S_1S_2 on, S_1 off S_2 on, S_1S_2 off. From this figure, it is clear that the two PFC stages interact during the S_1S_2 off region. To minimize this effect, a split inductor configuration is chosen in each PFC stage. By proper design of L_{1f}, L_{1b}, L_{2f}, and L_{2b}, the interaction can be kept to a minimum and the input current quality is not affected.

B. Staggered PWM

To overcome the interaction between phases, staggered PWM is used. The two single-phase PFC modules can work independently by avoiding the Fig. 3(d) period. If 180° phase-shifted PWM carrier signals are used and the duty ratio is higher than 0.5 when the two input voltages are the same, the interaction is virtually eliminated. Fig. 5 shows the gating signals of both switches.

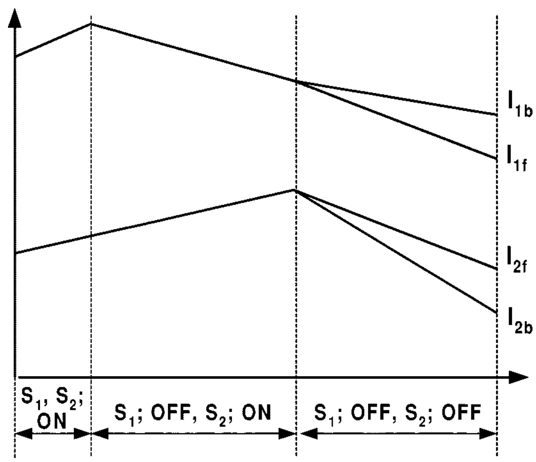


Fig. 4. Inductor current waveforms for a switching period.

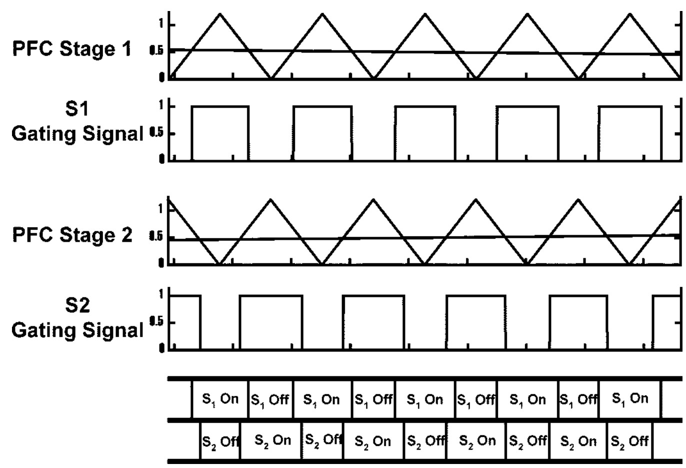


Fig. 5. Staggered PWM.

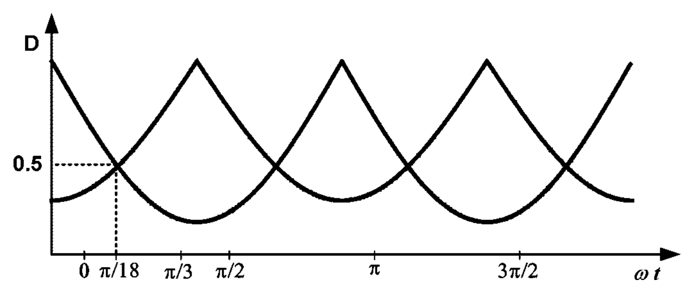


Fig. 6. Input voltage versus duty ratio.

The input voltages and the duty ratio have the relationship as in Fig. 6. Since the input voltages become the same at $\pi/18$, minimum output voltage for the staggered PWM is calculated as

$$V_o \geq \frac{1}{1-D} V_{\text{in}}\left(\frac{\pi}{18}\right) \tag{5.a}$$

or

$$V_o \geq 1.85 V_{LL}. \tag{5.b}$$

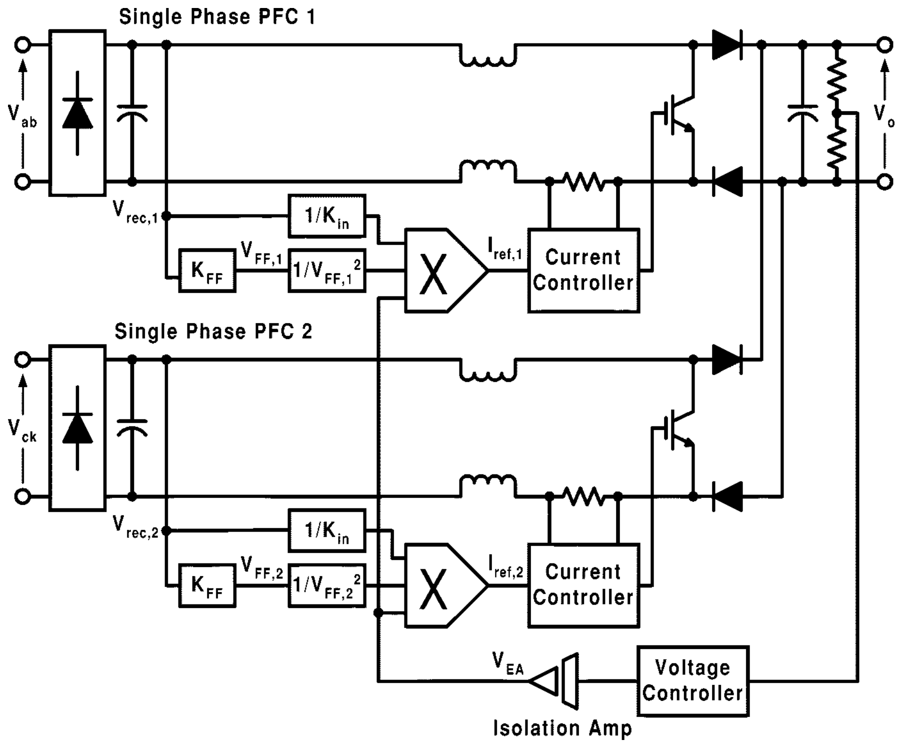


Fig. 7. Control block diagram of the system.

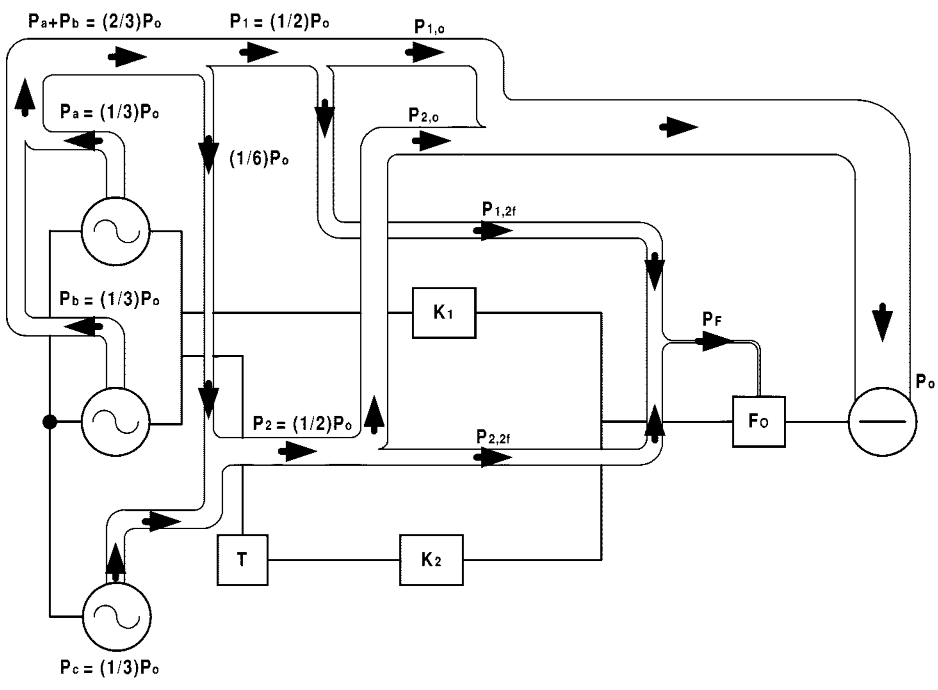


Fig. 8. Power-flow diagram of the proposed system.

C. Control Scheme

Fig. 7 shows the control block for the system. $V_{\mathrm{FF,i}}$ is dc voltage proportional to the rectified voltage $V_{\mathrm{rec},\,i}$. The rectified input current $I_{\mathrm{rec},\,i}$ and the current reference $I_{\mathrm{ref},\,i}$ can be represented as

$$I_{\mathrm{rec},\,i} = K_s I_{\mathrm{ref},\,i}, \qquad i = 1, 2 \tag{6}$$

$$I_{\mathrm{ref},\,i} = K_s K_M \frac{V_{\mathrm{rec},\,i}}{K_{\mathrm{in}}} \cdot \frac{1}{K_{\mathrm{FF}}^2 V_{\mathrm{rec},\,i}^2} V_{\mathrm{EA}} \tag{7}$$

where

- K_s PFC power stage gain;
- K_M multiplier gain;
- K_{FF} feedforward gain;
- K_{in} waveform input gain;
- V_{EA} voltage error amplifier output.

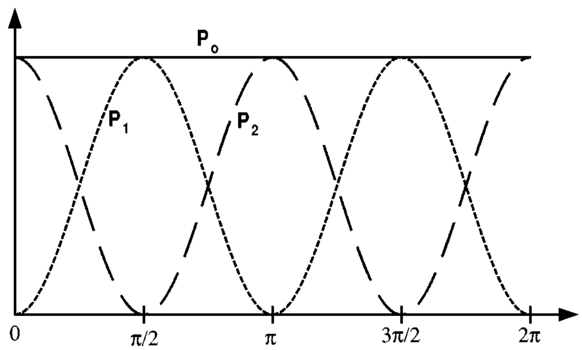


Fig. 9. Power processed at each PFC.

From (6) and (7), the rectified current $I_{\text{rec},\,i}$ is proportional to the reciprocal of $V_{\text{rec},\,i}$. Therefore, the input power P_i is

$$P_i = V_{\text{rec},\,i} I_{\text{rec},\,i} = \frac{K_s K_M}{K_{\text{in}} K_{\text{FF}}^2} V_{\text{EA}}, \qquad i = 1,\,2. \tag{8}$$

Each PFC module can carry the same amount of power simply by sharing the same voltage error amplifier output.

D. Power Flow and Autotransformer Rating

Fig. 8 shows the power-flow diagram in the proposed approach. K_1 and K_2 represent the boost block. F_o is the output filter and T the autotransformer. Each boost PFC module supplies the same power (P_1 and P_2), which flows to the dc side as dc power ($P_{1,\,o}$ and $P_{2,\,o}$) and to the filter F_o as the power oscillating at twice the line frequency ($P_{1,\,2f}$ and $P_{2,\,2f}$).

The relationship between the sources and each single-phase PFC module is

$$P_a + P_b = P_1 + \frac{1}{3} P_2 \tag{9}$$

$$P_c = \frac{2}{3} P_2. \tag{10}$$

Since the two input voltages v_{ab} and v_{ck} of the two single-phase PFC modules are in right angle, the second-order harmonic power components are cancelled each other. Therefore, the output filter capacitor F_o sees only switching frequency component (P_F).

The power processed in each module is shown in Fig. 9. The solid line represents output power. Dashed lines are the power via the single-phase PFC module 1 (P_1) and the power via the single-phase PFC module 2 (P_2).

The rms currents through the single-phase PFC module 1 and the single-phase PFC module 2 can be calculated as

$$P_1 = \frac{1}{2} P_{\text{in}} \tag{11}$$

$$V_{LL} I_1 = \frac{1}{2} \left(\sqrt{3}\, V_{LL} I_a \right) \tag{12}$$

or

$$I_1 = \frac{\sqrt{3}}{2} I_a = 0.8660 I_a. \tag{13}$$

From the vector diagram,

$$V_2 = \frac{\sqrt{3}}{2} V_{LL}. \tag{14}$$

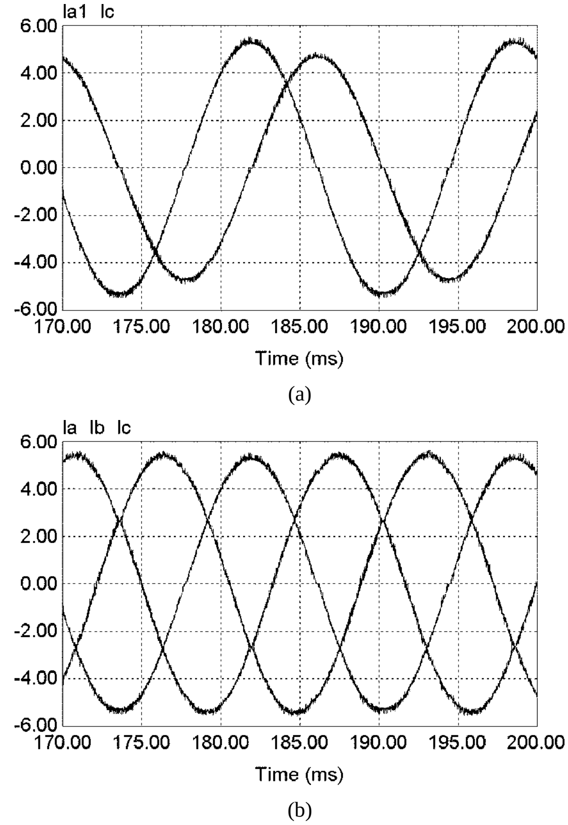


Fig. 10. Simulated waveforms. (a) Input current waveforms at each PFC. (b) Input line current I_a, I_b, and I_c.

Since the two PFC modules process the same power,

$$P_2 = \frac{1}{2} P_{\text{in}} \tag{15}$$

or

$$\left(\frac{\sqrt{3}}{2} V_{LL} \right) I_2 = \frac{1}{2} \left(\sqrt{3}\, V_{LL} I_a \right). \tag{16}$$

Therefore,

$$I_2 = I_a. \tag{17}$$

With high power factor, the voltage and current waveforms are in phase by definition. Thus, the instantaneous input powers of the single-phase PFC module 1 ($p_{\text{in},\,1}$) and the single-phase PFC module 2 ($p_{\text{in},\,2}$) are calculated as the following:

$$\begin{aligned} p_{\text{in},\,1} &= \left(\sqrt{2}\, V_{LL} \sin \omega t \right) \left(\sqrt{2} \frac{\sqrt{3}}{2} I_a \sin \omega t \right) \\ &= \sqrt{3}\, V_{LL} I_a \sin^2 \omega t \\ &= \frac{\sqrt{3}}{2} V_{LL} I_a (1 - \cos 2\omega t) \end{aligned} \tag{18}$$

$$\begin{aligned} p_{\text{in},\,2} &= \left(\sqrt{2}\, V_{LL} \cos \omega t \right) \left(\sqrt{2} \frac{\sqrt{3}}{2} I_a \cos \omega t \right) \\ &= \sqrt{3}\, V_{LL} I_a \cos^2 \omega t \\ &= \frac{\sqrt{3}}{2} V_{LL} I_a (1 + \cos 2\omega t). \end{aligned} \tag{19}$$

TABLE I
(a) VA RATING OF THE AUTO-TRANSFORMER (rms VALUE) AND (b) OPERATING CONDITION

Auto-transformer		Expression	rms value
Primary(secondary) winding current	I_{ak}	$0.5000\ I_a$	2.0 [A]
Primary(secondary) winding voltage	V_{ak}	$0.5000 V_{LL}$	110 [V]
VA rating	VA_{TR}	$0.1443\ P_o$	216.5 [VA]

(a)

Output power	750 [VA]
Input voltage range (V_{ab})	190 – 250 [V_{rms}]
Input voltage range (V_{ck})	165 – 217 [V_{rms}]
Output voltage	380 [V_{dc}]
Line frequency	60 [Hz]
Switching frequency	20 [kHz]

(b)

The output capacitor is considered to be large enough to hold the dc-link voltage $V_{\rm dc}$ fairly constant. The power outputs to the output capacitor from each boost PFC ($p_{\rm chg,\,1}$ and $p_{chg,\,2}$) are

$$p_{\rm chg,\,1} = V_{\rm dc} i_{\rm chg,\,1}. \tag{20}$$

Since $p_{\rm in,\,1} = p_{\rm chg,\,1}$,

$$\begin{aligned} i_{\rm chg,\,1} &= p_{\rm chg,\,1}/V_{\rm dc} \\ &= \left\{ \frac{\sqrt{3}}{2} V_{LL} I_a (1 - \cos 2\omega t) \right\} \Big/ V_{\rm dc}. \end{aligned} \tag{21}$$

$i_{\rm chg,\,2}$ can be calculated by the same way

$$i_{\rm chg,\,2} = \left\{ \frac{\sqrt{3}}{2} V_{LL} I_a (1 + \cos 2\omega t) \right\} \Big/ V_{\rm dc}. \tag{22}$$

Therefore, the current at the output capacitor $i_{\rm chg}$ can be calculated by adding these two current components

$$\begin{aligned} i_{\rm chg} &= i_{\rm chg,\,1} + i_{\rm chg,\,2} \\ &= \left(\sqrt{3} V_{LL} I_a\right) \Big/ V_{\rm dc}. \end{aligned} \tag{23}$$

Equation (23) shows that there is only dc current component at the output capacitor.

The current fed through the center-tapped autotransformer by phases a and b returns through phase c. Therefore, the rms value of the winding current is half of I_c. The voltage across the end of the autotransformer is line-to-line voltage. The power handled by the autotransformer is

$$P_{TR} = \frac{1}{2} \left\{ \left(\frac{1}{2} V_{LL} \right) * \left(\frac{1}{2} I_a \right) * 2 \right\} = \frac{1}{4} V_{LL} I_a. \tag{24}$$

Then, the VA rating of the autotransformer is

$$VA_{TR} = \frac{P_{TR}}{P_{\rm in}} = \frac{\frac{1}{4} V_{LL} I_a}{\sqrt{3} V_{LL} I_a} = 0.1443. \tag{25}$$

III. SIMULATION RESULTS

Fig. 10 shows the simulation result of the proposed system. A simple proportional plus integral (PI) controller is used for the inner current control loop. The voltage control loop feeds the current references of the two single-phase PFC modules forcing current sharing between them.

The amplitudes of input currents at each PFC [Fig. 10(a)] are different to carry the same power. The input line current waveforms are near sinusoidal [Fig. 10(b)], which demonstrates the proposed approach.

IV. DESIGN EXAMPLE

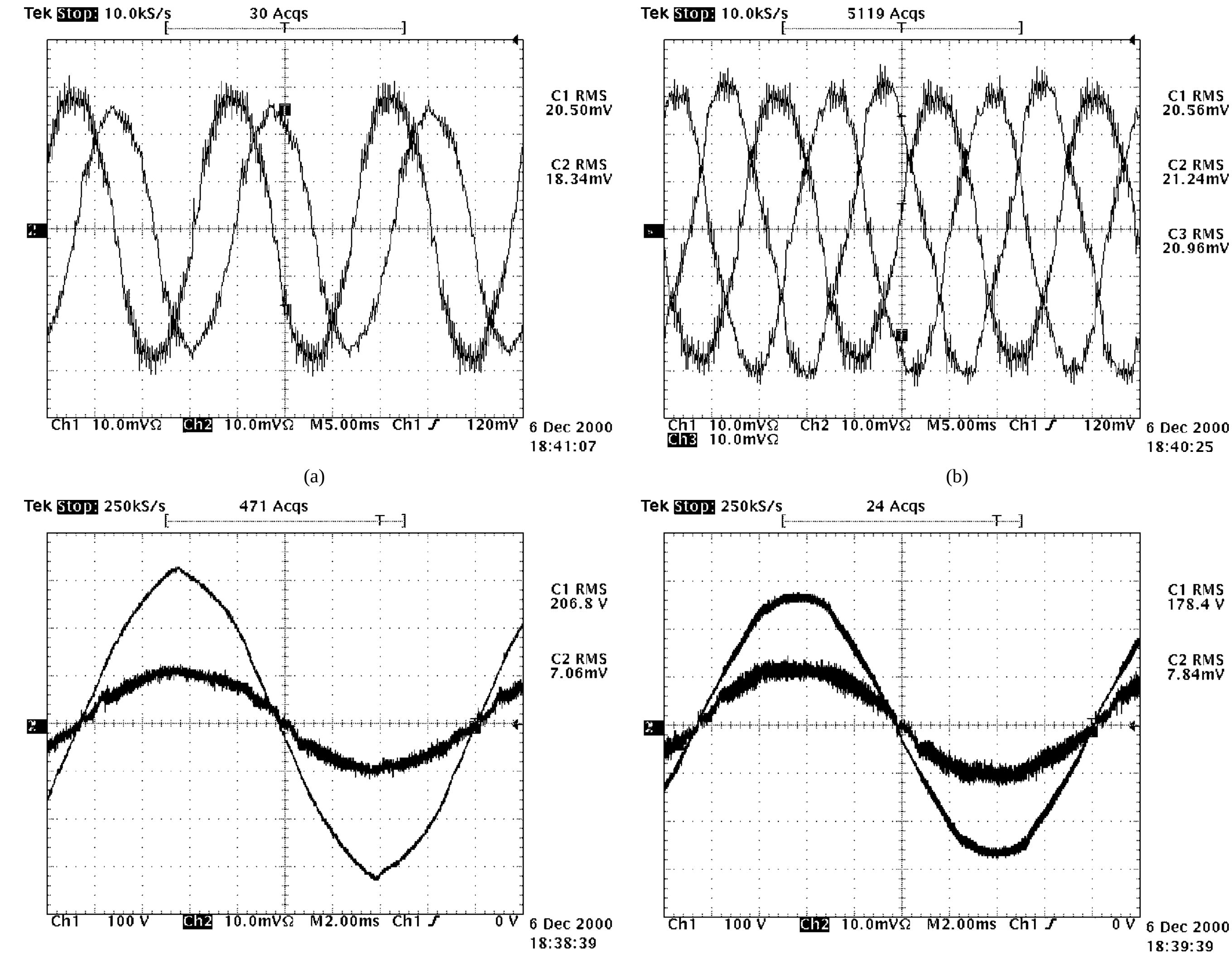
Table I summarizes the VA rating of the autotransformer and the operating condition of each PFC module. For an output power of 1.5 kVA, each PFC module supplies 750 VA. Design of each PFC modules follows the single-phase boost PFC operating in continuous conduction mode (CCM) [10]. Since the low-frequency power components cancel each other, the output capacitor handles only high-frequency ripple elements.

V. EXPERIMENTAL RESULTS

The proposed three-phase PFC rated at 220 V, 1.5 kVA (Fig. 1) has been implemented and the results are discussed in this section. Both PFC modules are controlled by Unitrode UC3854A controllers. Fig. 11(a) shows the input currents I_{a1} and I_c of each PFC which are 90° phase shifted and the amplitudes are different so that their respective output powers are equal. Fig. 11(b) shows the line currents I_a, I_b and I_c. They are nearly sinusoidal in shape. Fig. 11(c) and (d) shows the voltage V_{ab} and current I_{a1}; V_{ck} and current I_c, respectively. It is clear from the figure that each PFC stage operates in CCM at unity power factor.

VI. CONCLUSION

In this paper, a new three-phase PFC scheme using two standard single-phase PFC modules has been presented. Each PFC module is rated for half the output power and operates in CCM with unity power factor. With staggered PWM, the



(a) (b) (c) (d)

Fig. 11. Experimental results. (a) Current waveforms at each PFC (I_{a1} and I_c (2 A/div). (b) Line current waveforms (I_A, I_b, and I_c) (2 A/div). (c) PFC 1 input (V_{ab} and I_{a1}) (5 A/div). (d) PFC 2 input (V_{ck} and I_c) (5 A/div).

interaction between PFC modules is virtually eliminated. The resulting input line currents are nearly sinusoidal in shape. The experimental result from a laboratory prototype demonstrates the performance of the proposed system.

REFERENCES

[1] , "GALAXY switchmode rectifier 595 series catalog," Lucent Technologies, Murray Hill, NJ, 1999.

[2] "VS Series catalog," Astec America, Carlsbad, CA, 1999.

[3] *IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems*, IEEE Std. 519, 1992.

[4] *Limitations of Emission of Harmonic Current in Low-Voltage Power Supply Systems for Equipment With Rated Current Greater Than 16A*, IEC 61 000-3-4, 1998.

[5] P. Enjeti and I. Pitel, "Design of three-phase rectifier systems with clean power characteristics," presented at the IEEE PESC'99, Charleston, SC, 1999.

[6] H. Mao, F. C. Lee, D. Boroyevich, and S. Hiti, "Review of high performance three-phase power factor correction circuit," *IEEE Trans. Ind. Electron.*, vol. 44, pp. 437–446, Aug. 1997.

[7] Y. Jang and M. M. Jovanovic, "A comparative study of single-switch three-phase high-power-factor rectifiers," *IEEE Trans. Ind. Applicat.*, vol. 34, pp. 1327–1334, Nov./Dec. 1998.

[8] G. Spiazzi and F. C. Lee, "Implementation of single-phase boost power-factor-correction circuits in three-phase application," *IEEE Trans. Ind. Electron.*, vol. 44, pp. 365–371, June 1997.

[9] F. C. Lee, "Analysis and design of power factor correction circuits," presented at the Power Systems World Int. Conf., Professional Advancement Course, Las Vegas, NV, Sept. 1996.

[10] P. C. Todd, "UC3854 controlled power factor correction circuit design," Unitrode Corp., Merrimack, NH, Unitrode Application Note U-134, 1999.

Jaehong Hahn (S'99) received the B.S. degree from Seoul National University, Seoul, Korea, in 1989. He is currently working toward the Ph.D. degree in power electronics at Texas A&M University, College Station.

From 1989 to 1994, he was a Design Engineer at the Research and Development Center, Daewoo Heavy Industries, Incheon, Korea. From 1994 to 1995, he was a Field Application Engineer with Linear Technology Corporation. From 1995 to 1996, he was with Maxim Integrated Products Inc. as a Senior Field Application Engineer. His research interest is power electronics applications to power quality and clean power converters.

Prasad N. Enjeti (M'85–SM'88–F'00) received the B.E. degree from Osmania University, Hyderabad, India, the M.Tech degree from Indian Institute of Technology, Kanpur, India, and the Ph.D. degree from Concordia University, Montreal, QC, Canada, in 1980, 1982, and 1988, respectively, all in electrical engineering.

In 1988, he joined the Department of Electrical Engineering, Texas A&M University, College Station, as an Assistant Professor. In 1994, he was promoted to Associate Professor, and in 1998, he became a full Professor. His primary research interests are advance converters for power supplies and motor drives, power quality issues and active power filter development, and utility interface issues and "clean power" converter designs. He holds four U.S. patents and has licensed two new technologies to industry. He is the Lead Developer of the Power Quality Laboratory at Texas A&M University and is actively involved in many projects with industry while engaged in teaching, research, and consulting in the area of power electronics, motor drives, power quality, and clean power utility interface issues.

Prof. Enjeti was the recipient of numerous IEEE Industry Applications Society (IAS) Best Paper Awards, the Second Best Paper Award for papers published in mid-year 1994 to mid-year 1995 from the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the *IEEE Industry Applications Magazine* Prize Article Award in 1996. He is a member of the IAS Executive Board and the Chair of the Standing Committee on Electronic Communications. He is also the recipient of the select title "Class of 2001 Texas A&M University Faculty Fellow" Award for demonstrated achievement of excellence in research, scholarship, and leadership in the field. He is a Registered Professional Engineer in the State of Texas.

Ira J. Pitel (M'73–SM'82–F'99) received the B.S. degree from Rutgers—The State University of New Jersey, New Brunswick, the M.S. degree from Bucknell University, Lewisburg, PA, and the Ph.D. degree from Carnegie-Mellon University, Pittsburgh, PA, in 1972, 1975, and 1978, respectively.

From 1973 to 1976, he was with GTE Sylvania, researching high-frequency ballasting techniques for gaseous discharge lighting. He joined Bell Laboratories in 1978 and Exxon Enterprises in 1979. At Exxon, he was involved in high-power converter structures for ac motor drives, power processing for advanced battery systems, and controlled lighting. He was eventually transferred to one of Exxon's subsidiaries, Cornell-Dubilier Electronics, where he was Manager of Research and Development. In 1981, he founded Magna-Power Electronics, Boonton, NJ, a company specializing in custom and standard power conditioning products. As President, he is responsible for contract R&D and manufacturing of its line of 10–750-kW dc power supplies. In 1986, he joined Texas A&M University as an Adjunct Associate Professor. His research interests are high-power ac-to-dc converters, static inverters, spacecraft power supplies, and specialty lighting controls. He holds 21 patents in the field of power electronics.

Dr. Pitel is a co-recipient of the 1995 Society Prize Paper Award of the IEEE Industry Applications Society (IAS). He has served as Committee Chairman of the IAS Industrial Power Converter Committee in 1988–1989, Department Chairman of the IAS Industrial Power Conversion Systems Department in 1994–1995, and IAS Vice-President and President in 1998 and 1999, respectively. He is a member of Eta Kappa Nu and Tau Beta Pi.