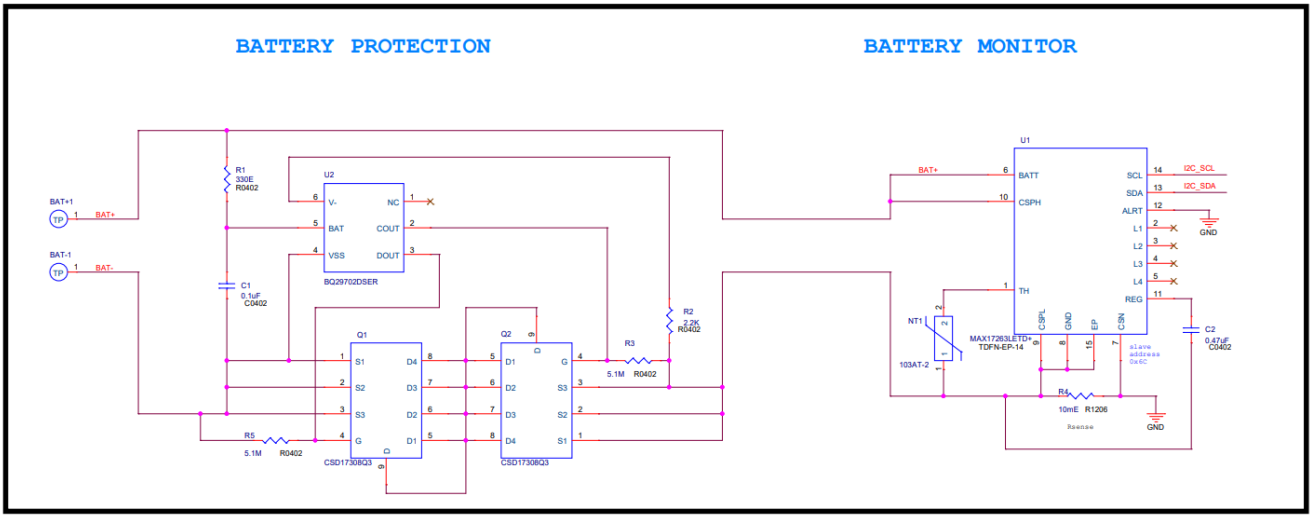
BATTERY PCB TEST REV1.2

Date:07-02-2024

Schematic of battery PCB



Protection IC- BQ29702DSER

MOSFET-CSD17308Q3

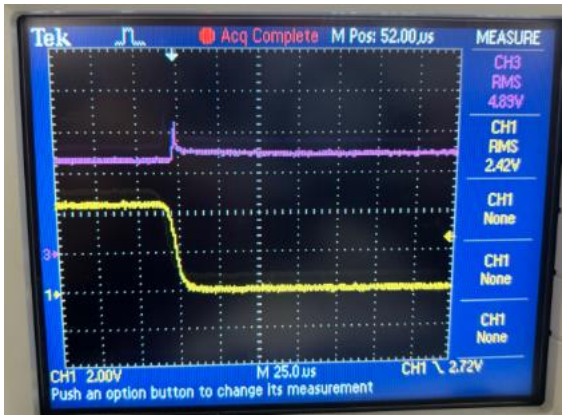
Monitoring IC-MAX17263LETD+

1) Overcharge detection voltage and overcharge release voltage (Test Circuit 1):

Expected: OVP=4.400 tolerance= –20 to 20 mV Measured tolerance: -40mV

Overcharge detection voltage

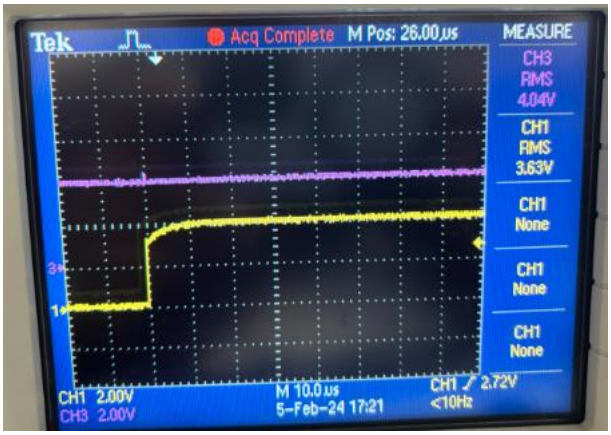
Once BAT to VSS voltage is increased up to **4.36**, the over-detection is triggered, COUT transitions from a high to low state.



Where in this image yellow line (channel 1) = Cout pin voltage level, purple line (channel 3) = BAT pin voltage level.

overcharge release voltage

overcharge release occurs when the BAT to VSS voltage will be 4.2V and CHG FET drive output goes from low to high.



Where in this image yellow line (channel 1) = Cout pin voltage level, purple line (channel 3) = BAT pin voltage level.

2) **Over-discharge detection voltage and over-discharge release voltage (Test Circuit 2):**

Expected: UVP= 2.800 tolerance= –50 to 50 mV Measured tolerance: -250mV

Over-discharge detection voltage

The Dout output goes from high to low when voltage between BAT and VSS becomes less than **2.55 V**.

Where in this image Sky-blue line (channel 2) = Dout pin voltage level, purple line (channel 3) = BAT pin voltage level.

over-discharge release voltage

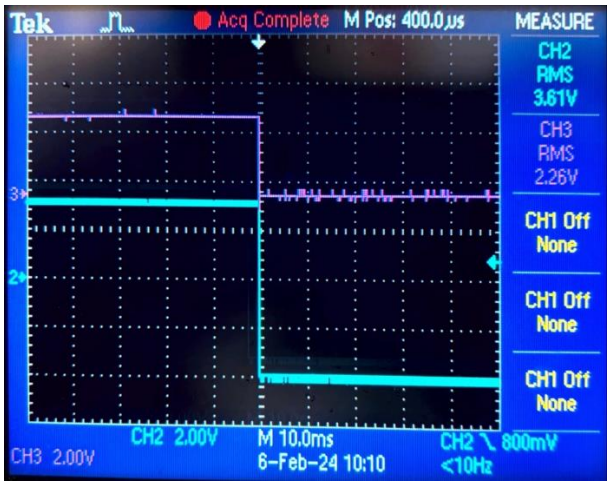
DOUT drive output transition from low to high when BAT to VSS voltage will become more than **3V**. Then DOUT output drive goes from low to high.

Where in this image Sky-blue line (channel 2) = Dout pin voltage level, purple line (channel 3) = BAT pin voltage level.

3) Discharge overcurrent detection voltage (Test Circuit 2):

Expected: OCD= 120mV tolerance = –15 to 15 mV Measured tolerance: 35mV

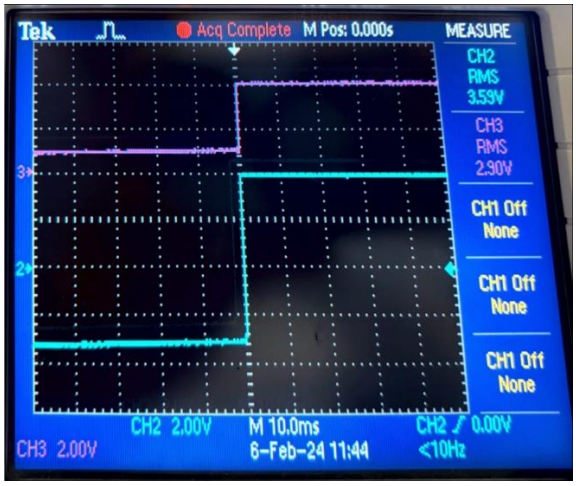
Discharge overcurrent detection voltage triggered when the voltage between V- and VSS is **155mV** (discharge current=**6A**). Then DOUT output drive transitions from high to low.



Where in this image Sky-blue line (channel 2) = Dout pin voltage level, purple line (channel 3) = BAT pin voltage level.

Release voltage

Release voltage is more than **100mV(4A)** between V- and VSS.

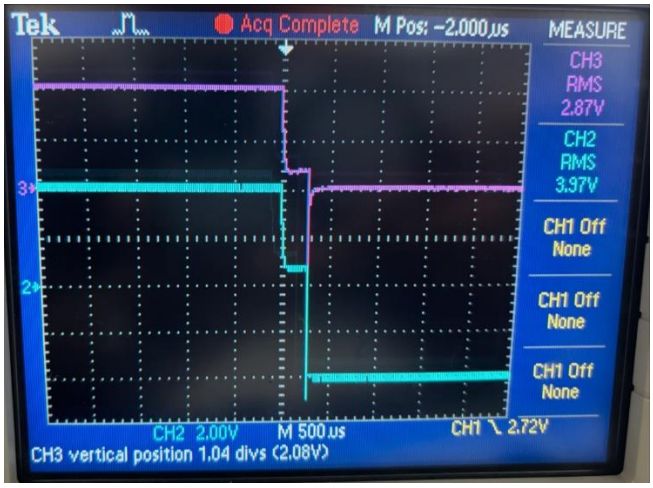


Where in this image Sky-blue line (channel 2) = Dout pin voltage level, purple line (channel 3) = BAT pin voltage level.

4) Load short circuit detection voltage (Test Circuit 2):

Expected: SCD=300mV tolerance= –100 to 100 mV Measured tolerance: within range

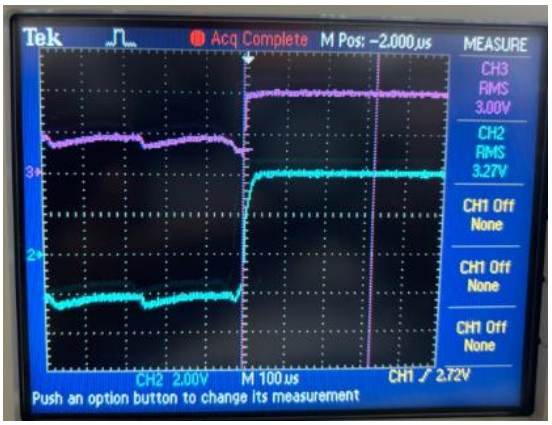
Load short-circuit detection voltage is triggered when the voltage between V- and VSS is more than **350mV** (Short) when DOUT output drive transitions from high to low.



Where in this image Sky-blue line (channel 2) = Dout pin voltage level, purple line (channel 3) = BAT pin voltage level.

Release voltage

When the voltage between V- and VSS is less than -30mV (no short present between battery terminal) when DOUT output drive transitions from high to low.

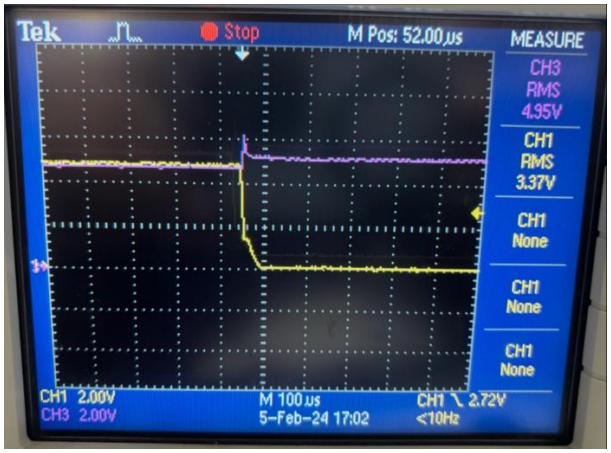


Where in this image Sky-blue line (channel 2) = Dout pin voltage level, purple line (channel 3) = BAT pin voltage level.

5) **Charge overcurrent detection voltage (Test Circuit 2):**

Expected: OCC= -100mv tolerance= –15 to 15 mV Measured tolerance: -50mV

The charge overcurrent detection voltage pins triggered when the voltage between VSS and V– is less than -150mV (Charge current =6.1A), Then COUT output drive transitions from high to low.



Where in this image yellow line (channel 1) = Cout pin voltage level, purple line (channel 3) = BAT pin voltage level.

Release voltage

when the voltage between VSS and V– is more than -100mV (charge current=5A),Then COUT output drive transitions from high to low.

Where in this image yellow line (channel 1) = Cout pin voltage level, purple line (channel 3) = BAT pin voltage level.

6) **Operating current consumption (Test Circuit 2):**

I_{NORMAL}= 4 to 5.5 µA Measured tolerance: -1.8uA

The operating current consumption $I_{BNORMAL}$ is **2.2uA** the current measured going into the BAT pin under the following conditions: V1 = 3.9 V and V2 = 0 V.

7) **Power down current consumption (Test Circuit 2):**

Expected: I_{Power_down} = 0.1 µA Measured tolerance: 1.6uA

The operating current consumption I_{Power_down} is **1.7uA** the current measured going into the BAT pin under the following conditions: V1 = 1.5 V and V2 = 1.5 V.

8) **Resistance between V– and BAT pin (Test Circuit 3):**

R_{V_D} =100 ,300, 550 kΩ Measured tolerance: 98 Ohm

Measure the resistance (RV_D) between V– and BAT pins is **2.133ohm** by setting the following conditions: V1 = 1.8 V and V2 = 0 V.

9) **Current sink between V– and VSS (Test Circuit 3):**

Expected: $I_{V–S}$ =8 to24 µA Measured tolerance: 7.5uA

Measure the current sink $I_{V–S}$ between V– and VSS pins is **0.5uA** by setting the following condition: V1 = 4 V.

10) **COUT current source when activated High (Test Circuit 4):**

Measure I_{COUT} current source is **10.7uA** on the COUT pin by setting the following conditions: V1 = 3.9 V, V2 = 0 V, and V3 = 3.4 V.

11) **COUT current sink when activated Low (Test Circuit 4):**

Measure I_{COUT} current sink is **10uA** on COUT pin by setting the following conditions: V1 = 4.5 V, V2 = 0 V, and V3 = 0.5 V.

12) **DOUT current source when activated High (Test Circuit 4):**

Measure I_{DOUT} current source is **0.4uA** on DOUT pin by setting the following conditions: V1 = 3.9 V, V2 = 0 V, and V3 = 3.4 V.

13) **DOUT current sink when activated Low (Test Circuit 4):**

Measure I_{DOUT} current sink is **1.3uA** on DOUT pin by setting the following conditions: V1 = 2.0 V, V2 = 0 V, and V3 = 0.4 V.

14) Overcharge detection delay (Test Circuit 5):

Expected: t_{OVPD} =0.25 s, 1.00 s, 1.25 s, 4.50 s tolerance= –20% to 20% s
Measured tolerance: -249.9ms

The overcharge detection delay time t_{OVPD} is the time delay before the COUT drive output transitions from high to low.

t_{OVPD}=18us

Where in this image yellow line (channel 1) = Cout pin voltage level, purple line (channel 3)= BAT pin voltage level.

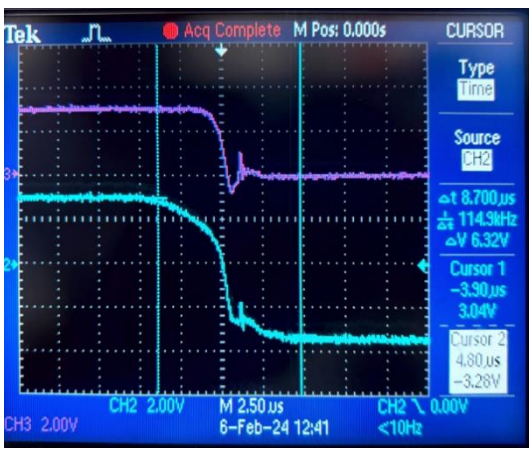
15) Over-discharge detection delay (Test Circuit 5):

Expected: t_{UVPD}= 20 ms, 96 ms, 125 ms, 144 ms tolerance= –20% to 20% ms

Measured tolerance: -19.9ms

The over-discharge detection delay time t_{UVPD} is the time delay before the DOUT drive output transitions from high to low once the voltage on V1 decreases to V_{UVP} threshold.

t_{UVPD}=8.7us



Where in this image Sky-blue line (channel 2) = Dout pin voltage level, purple line (channel 3) = BAT pin voltage level.

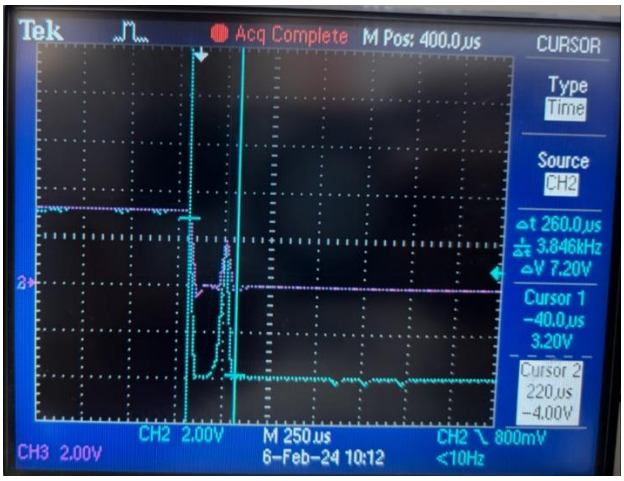
16) Discharge overcurrent detection delay (Test Circuit 5):

Expected: t_{OCDD}= 8 ms, 16 ms, 20 ms, 48 ms tolerance= –20% to 20% ms

Measured tolerance: -7.75us

The discharge overcurrent detection delay time t_{OCDD} is the time for DOUT drive output to transition from high to low after the voltage on V2 is increased from 0 V to 0.35 V.

t_{OCDD}=260us



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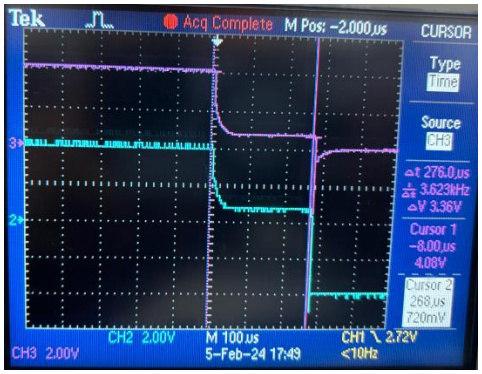
17) Load short circuit detection delay (Test Circuit 5):

Expected: t_{SCCD}= 250 µs tolerance= –50% to 50% us

Measured tolerance: within range.

The load short-circuit detection delay time t_{SCCD} is the time for DOUT drive output to transition from high to low after the voltage on V2 is increased from 0 V to V1 – 1 V.

t_{SCCD}=276us



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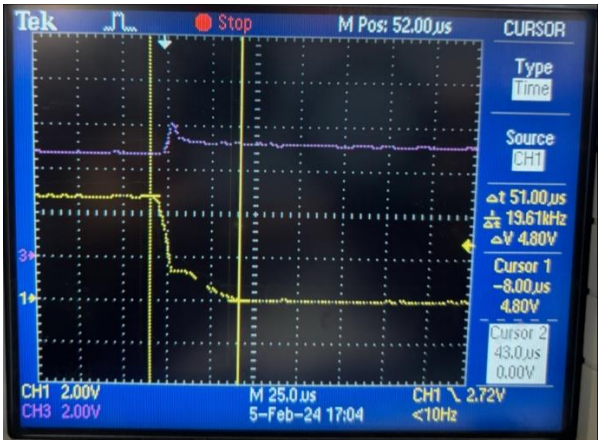
18) Charge overcurrent detection delay (Test Circuit 5):

Expected: t_{OCCD}= 4 ms, 6 ms, 8 ms, 16 ms tolerance= –20% to 20% ms

Measured tolerance: -3.5us

The charge overcurrent detection delay time t_{OCCD} is the time for COUT drive output to transition from high to low after the voltage on V2 is decreased from 0 V to –0.3 V.

t_{OCCD}=51us



Where in this image yellow line (channel 1) = Cout pin voltage level, purple line (channel 3)= BAT pin voltage level.