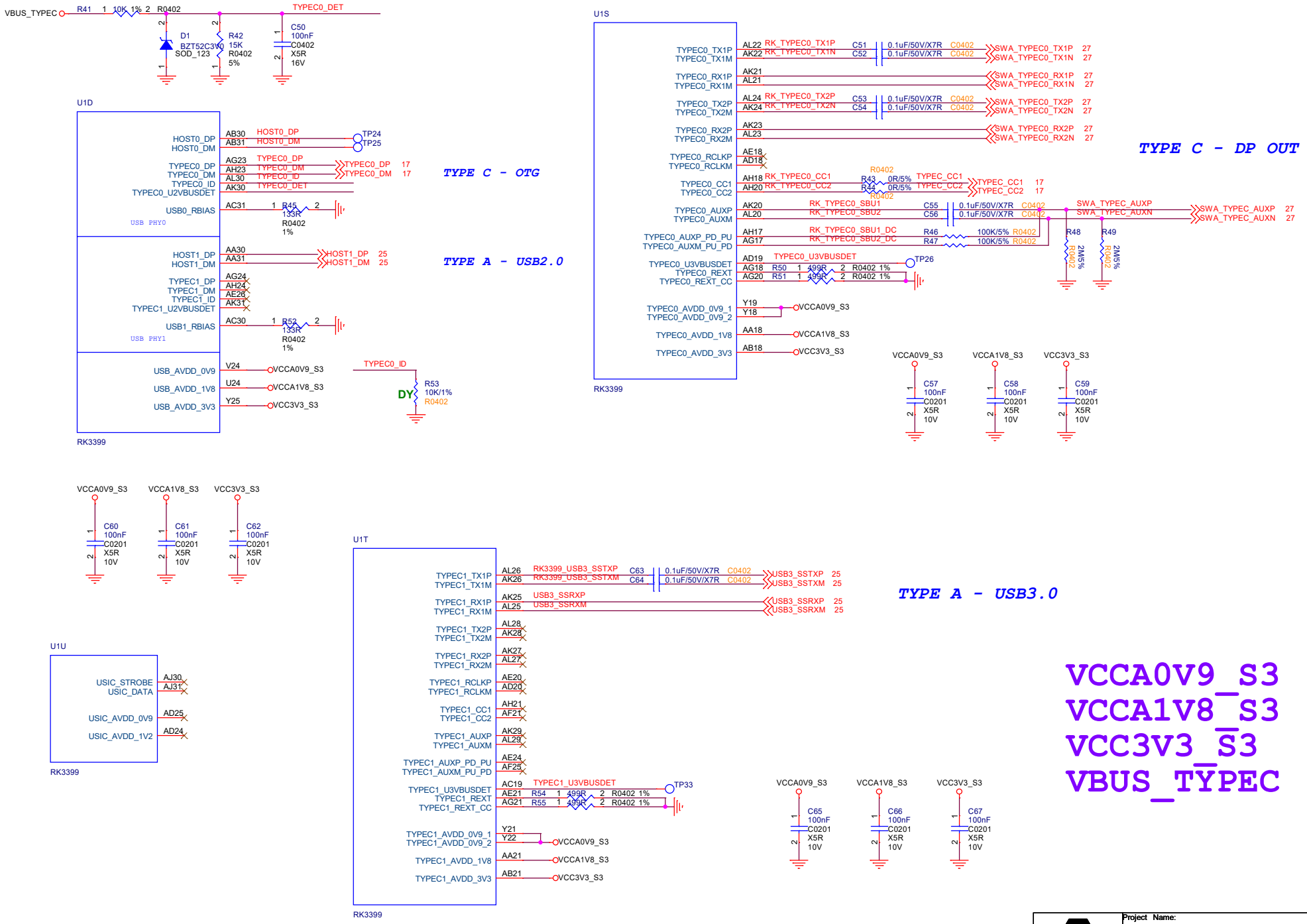

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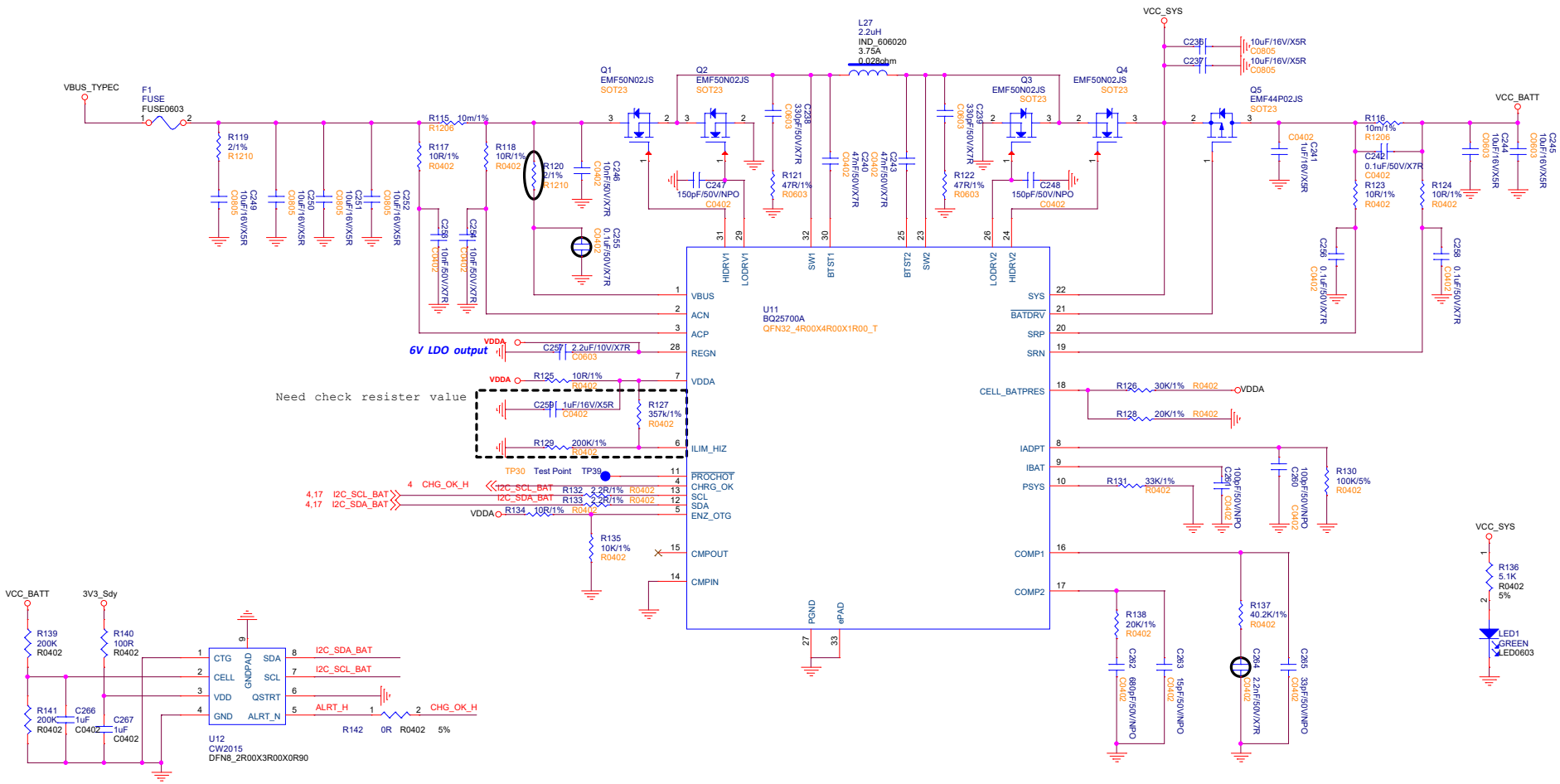
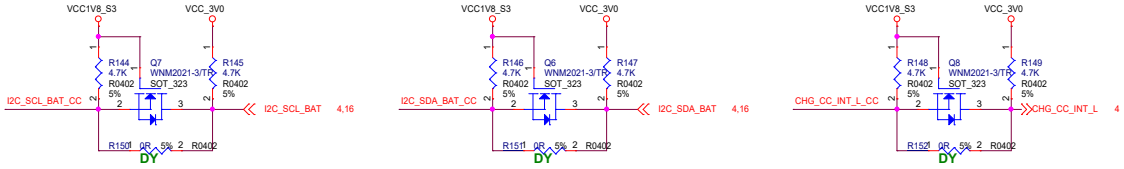


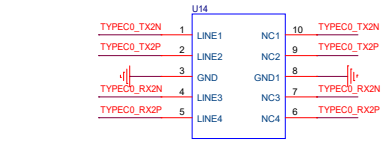
8.3.2.3 *Battery Cell Configuration*

CELL_BATPRESZ pin is biased with resistors from REGN to CELL_BATPRESZ to GND. After VDDA LDO is activated, the device detects the battery configuration through CELL_BATPRESZ pin bias voltage. Refer to *Electrical Characteristics* for CELL setting thresholds.

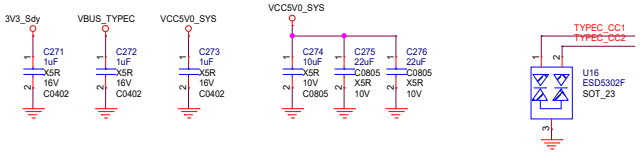
Table 1. Battery Cell Configuration

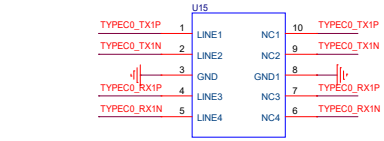
CELL COUNT	PIN VOLTAGE w.r.t. VDDA	BATTERY VOLTAGE (REG0x15)	SYSOVP
4S	75%	16.800V	19.5V
3S	55%	12.592V	19.5V
2S	40%	8.400V	12V
1S	25%	4.192V	5V



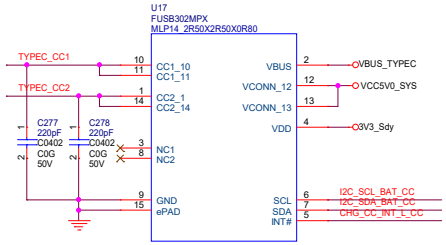


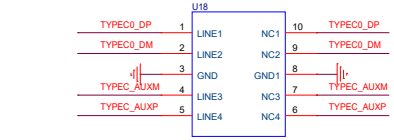
TVS DIODE 5VWM 15VC 10SLP RCLAMP0524PCT-ND (Inactive) replace by 1700000025





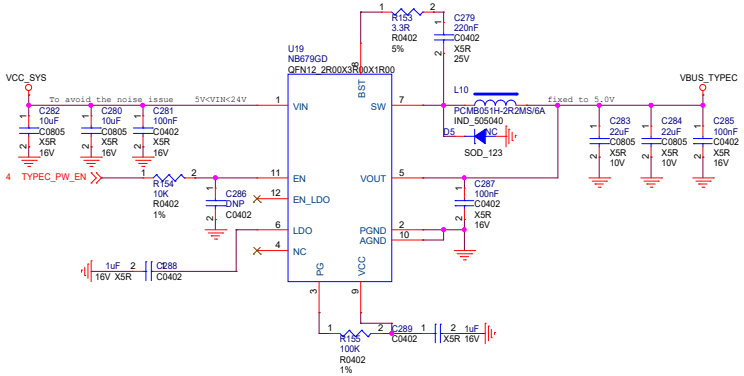
TVS DIODE 5VWM 15VC 10SLP RCLAMP0524PCT-ND (Inactive) replace by 1700000025



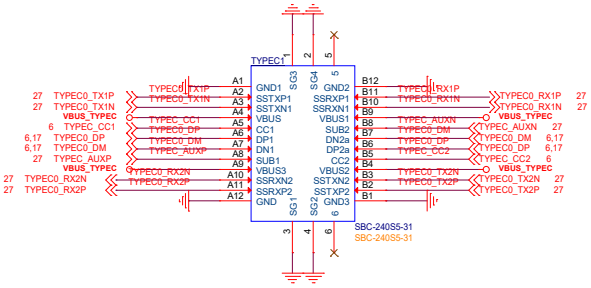


TVS DIODE 5VWM 15VC 10SLP RCLAMP0524PCT-ND (Inactive) replace by 1700000025

TYPE C power out enable when CC PIN on Battery MODE



USB Type C Receptable



VBUS_TYPEC
VCC5V0_SYS
VCC_3V0
VCC1V8_S3

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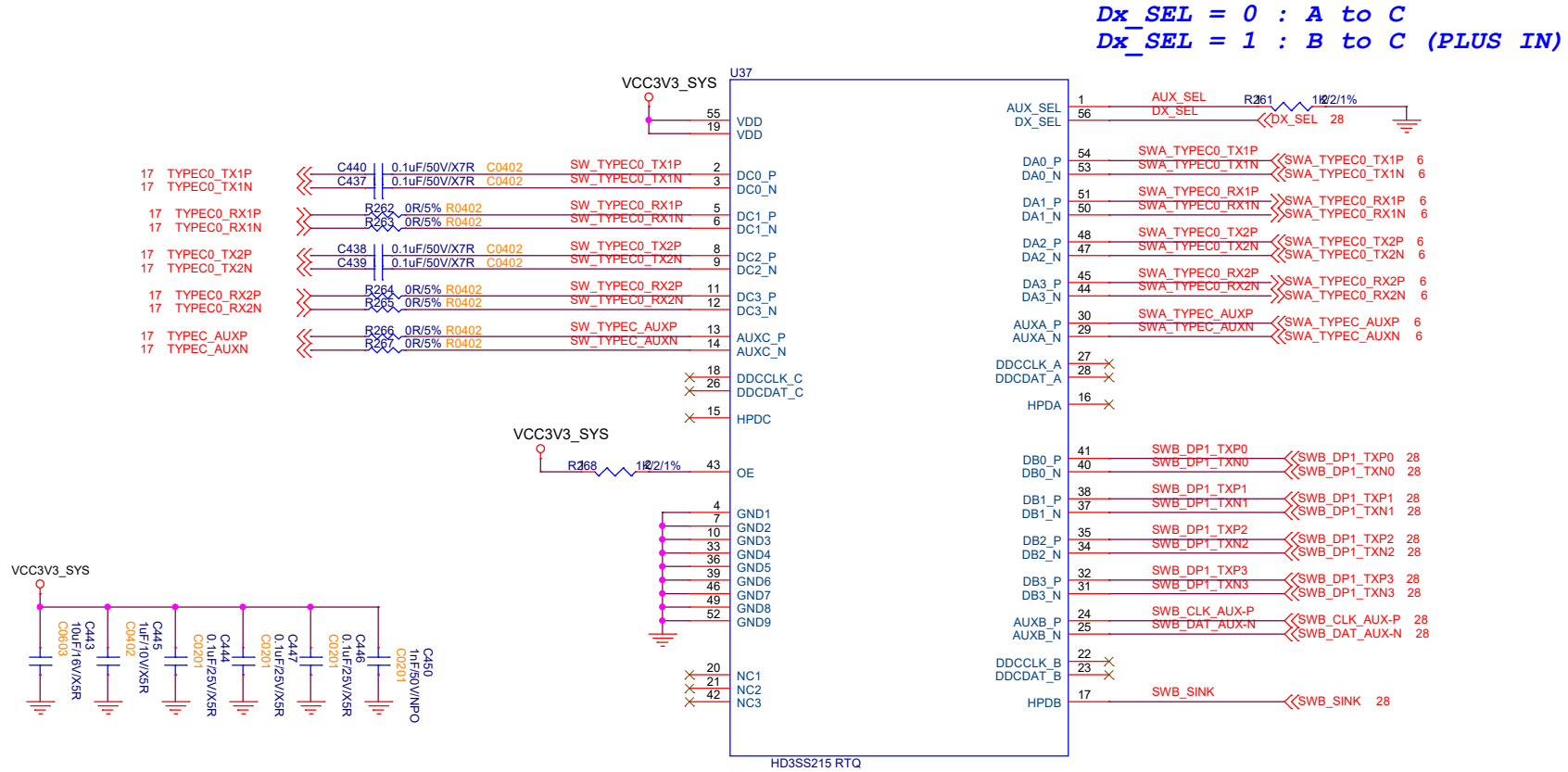

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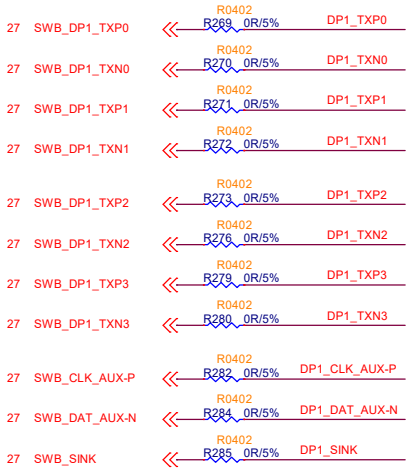
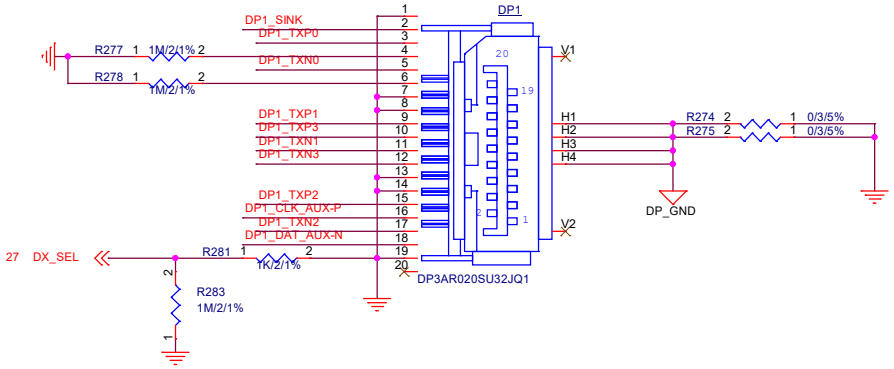
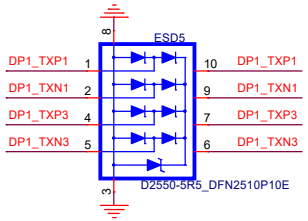
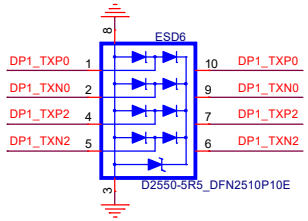
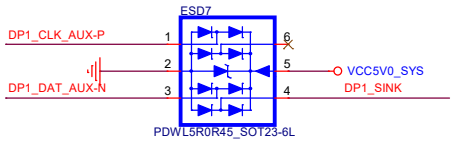
Mini DP

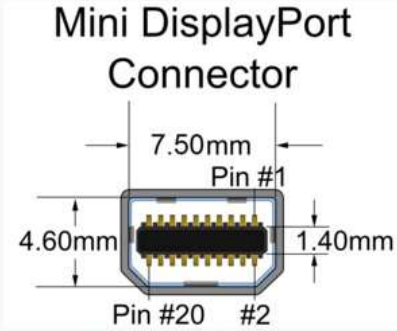












External Mini DisplayPort Connector

Pin 1	GND	Ground
Pin 2	Hot Plug Detect	Hot Plug Detect
Pin 3	ML_Lane 0 (p)	Lane 0 (positive)
Pin 4	CONFIG1	CONFIG1
Pin 5	ML_Lane 0 (n)	Lane 0 (negative)
Pin 6	CONFIG2	CONFIG2
Pin 7	GND	Ground
Pin 8	GND	Ground
Pin 9	ML_Lane 1 (p)	Lane 1 (positive)
Pin 10	ML_Lane 3 (p)	Lane 3 (positive)
Pin 11	ML_Lane 1 (n)	Lane 1 (negative)
Pin 12	ML_Lane 3 (n)	Lane 3 (negative)
Pin 13	GND	Ground
Pin 14	GND	Ground
Pin 15	ML_Lane 2 (p)	Lane 2 (positive)
Pin 16	AUX_CH (p)	Auxiliary Channel (positive)
Pin 17	ML_Lane 2 (n)	Lane 2 (negative)
Pin 18	AUX_CH (n)	Auxiliary Channel (negative)
Pin 19	GND	Ground
Pin 20	DP_PWR	Power for connector

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