bq40z60 Charging Voltage Compensation

Thomas Cosby   *Battery Management Solutions*

The bq40z60 integrated charger is a NVDC buck architecture and the charging voltage range is set by the feedback resistors and a set of charging parameters.

Hardware configuration:

The charger feedback resistors set the maximum output voltage for the charger. The charger is an NVDC architecture, so the gauge dynamically adjusts the feedback voltage from 610mV V to 1220mV as the cells charge.

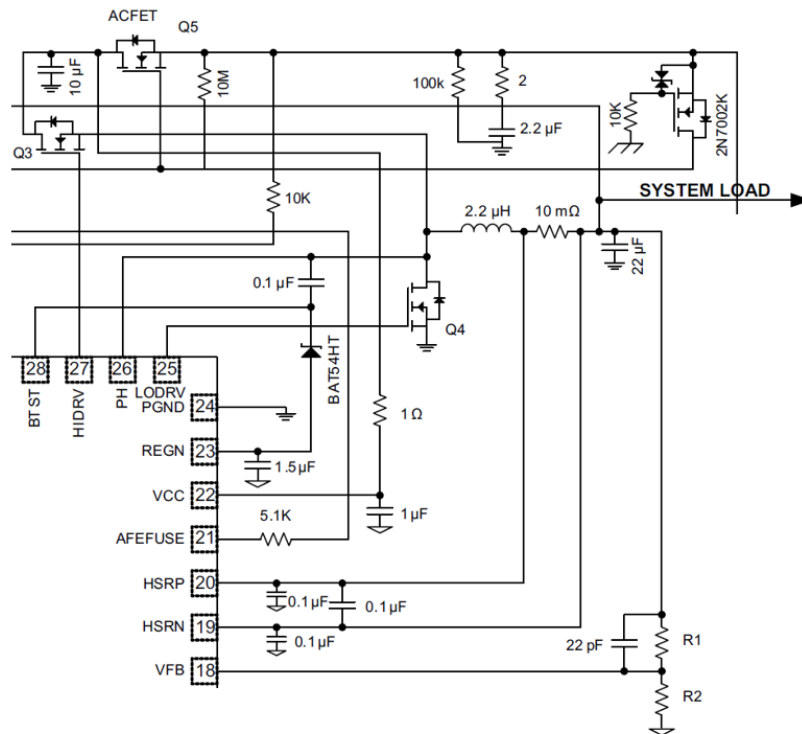The equation to set the feedback voltage is: Maximum output voltage = 1220mV * (1 + R1 / R2)

Figure 1: bq40z60 Charger

Firmware Configuration:

The bq40z60 firmware charging algorithm sets the charging voltage range. You do not have to change the feedback resistors to reduce the charging voltage. The device can adjust for this, but there is a resolution issue that we have to compensate. The issue is that the **Voltage Resolution** register accepts an integer, so the calculated value must be rounded.

Charging Voltage
Sets the maximum pack charging voltage. Multiply the data flash *Voltage* parameter by the number of series cells.

Minimum Output Voltage
Sets the minimum voltage for NVDC charging voltage range.

Voltage Resolution
Sets the step size that the firmware uses for the NVDC charging voltage.

Assumptions for this example:
Cell configuration: 3S
Desired **Charging Voltage**: 12300mV (4100mV per cell)

The formula for the *Minimum Output Voltage* = 610mV * (1 + R1 / R2), where we set R1=332k and R2 = 35.7k for a 3S configuration. So, the *Minimum Output Voltage* = 6283mV

The formula for the *Voltage Resolution* = (610mV * (1 + R1 / R2)) / 256.
So, *Voltage Resolution* = 6283mV / 256 = 24.54mV

The device only accepts an integer for the *Voltage Resolution*, so we enter 24mV to be conservative. This is the firmware limitation that causes a mismatch between the desired maximum **Charging Voltage** and the actual maximum charging voltage. The *Voltage Resolution* parameter will be set in uV in the next firmware revision to allow better resolution.

The charger has an internal Voltage Register that sets the number of *Voltage Resolution* steps required to reach the **Charging Voltage.** The full scale range of the Voltage Register is 256 steps.

Charging Voltage = *Minimum Output Voltage* + *Voltage Resolution* * Voltage Register

12300mV = 6283 + 24 * Voltage Register
Voltage Register = (12300 – 6283) / 24 = 250.7 $\Rightarrow$ 250

This is where the *Voltage Resolution* data entry limitation affects the results.

The desired maximum **Charging Voltage** = 6283 + 24*250 = 12283mV, but the hardware control loop uses the actual voltage resolution of 24.54mV. Therefore, the actual maximum **Charging Voltage** = 6283 + 24.54 * 250 = 12418mV, which exceeds the desired maximum **Charging Voltage**.

The firmware should set it to 245 based on the true charging voltage range.

Voltage Register = (12300 – 6283) / 24.54 = 245.2 $\Rightarrow$ 245

Charging Voltage = 6283 + 24.54*245 = 12295mV

The device will use the entered Voltage Resolution setting (24mV) to set the internal Voltage Register.

We need to set the **Charging Voltage** lower to force the Voltage Register to 245 to match the hardware control loop.

Therefore, you should reduce the **Charging Voltage** parameters to compensate for this mismatch.

Charging Voltage = 6283 + 24*245 = <u>12163mV</u>

Therefore, set the data flash *Voltage* (cell based) to 12163mV / 3 = <u>4054.3mV</u> $\Rightarrow$ 4054mV.

If we set the *Voltage* to 4054mV. (12162mV stack), then the device will set the Voltage Register to (12300 − 6283) / 24.54 = <u>245.2</u> $\Rightarrow$ 245

This should allow the control loop voltage range to be 6283mV to 12295mV (6283 + 24.54 * 245). The pack should switch to CV mode at this voltage and taper the current. You can follow the same process, if you want to set the peak charging voltage a slightly higher.