bq77915 Cell Balancing

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bq77915 cell balancing information

- See the data sheet www.ti.com/lit/gpn/bq77915 section 9.3.4
- This references various sections and diagrams
- Look for a future cell balance apnote

Cell balance control pin

V_{CBIL}	CBI low threshold		0.5	V

- Cell balance is controlled by the CBI pin.
  - CBI has an internal pull up
  - It is current limited
  - If controlled it should be pulled low with an open drain/open collector output
    - It should not be driven high, this can force current into the part and voltage on the AVDD pin which powers the circuit
  - If always enabled CBI may be tied to VSS
  - If stacked, CBI should have a resistor

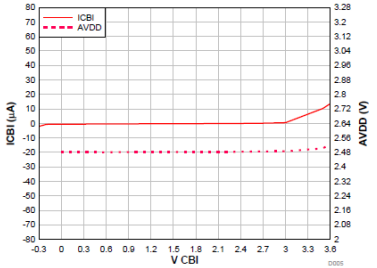


Figure 5. CBI Input Current vs. VCBI

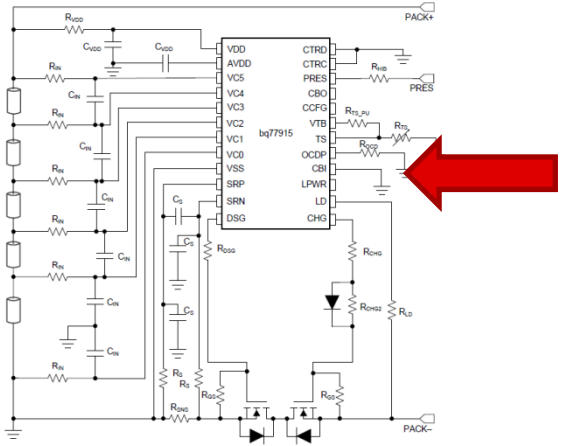


Figure 29. The bq77915 Device with Five Cells

Cell balancing general

- Cell balancing requires charge current, voltage qualification, and absence of certain faults
  - Current must be above the state comparator threshold
    - ~ 1.875 mV to ~ 0.625 mV
  - Voltage expected to rise during charge
    - A cell voltage must be above the start threshold
    - Cell voltage must be sufficiently separated during charge
    - A VFC target defined from OV changes balance behavior

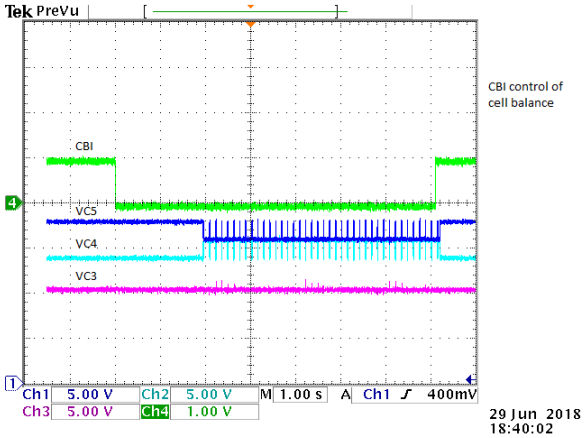
CURRENT STATE COMPARATOR				
V_{STATE_D}	Discharge qualification threshold1	Measured at SRP-SRN	–1.875	mV
$V_{STATE\_D\_HYS}$	Discharge qualification threshold1 hysteresis	Measured at SRP-SRN	–1.25	mV
V_{STATE_C}	Charge qualification threshold1	Measured at SRP-SRN	1.875	mV
$V_{STATE\_C\_HYS}$	Charge qualification threshold1 hysteresis	Measured at SRP-SRN	1.25	mV
t_{STATE}	State detection qualification time		1.2	ms

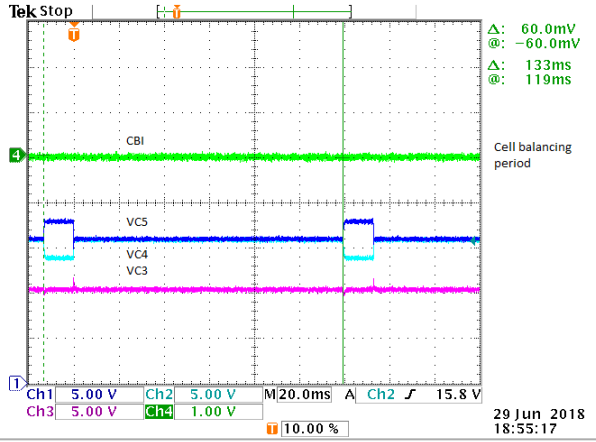
Table 2. Cell Balancing Threshold Summary

NAME	Description	Options
V_{START}	Start Threshold for Cell Balancing	3.5 V, 3.8 V
V_{HYST}	Hysteresis between overvoltage and full charge voltage range (VOV — VFC)	50 mV, 100 mV, 150 mV, 200 mV
V_{STEP}	Difference between the cell balancing threshold voltages (VCBTH — VCBTL)	50 mV, 100 mV, 150 mV, 200 mV

Cell balance mechanism

- As other BMS devices, pins pull together
  - Current through input filter resistors bypasses the cell and power is dissipated
  - Internal resistance is small
  - Bypassed current is small during high current charge, becomes more significant portion as charge current tapers
  - Duty cycle is fixed by device timing





R_{BAL}	Cell balancing internal FET resistance	Cell1 through Cell5 = 4 V, VDD = 20 V	8	12	20	Ω
D_{BAL}	Cell balancing duty cycle	Only one cell balanced in the stack		90 %		

External balancing

- Internal balance current is high, but limited, reduces input filter resistance
- External balancing allows higher current or more filter, can be done similar to other BMS ICs
- N or P channel
  - N-channel shown in data sheet

ABS MAX

I_O	Output current	Cell Balancing current (VC5, VC4, VC3, VC2, VC1, VC0)	50	mA

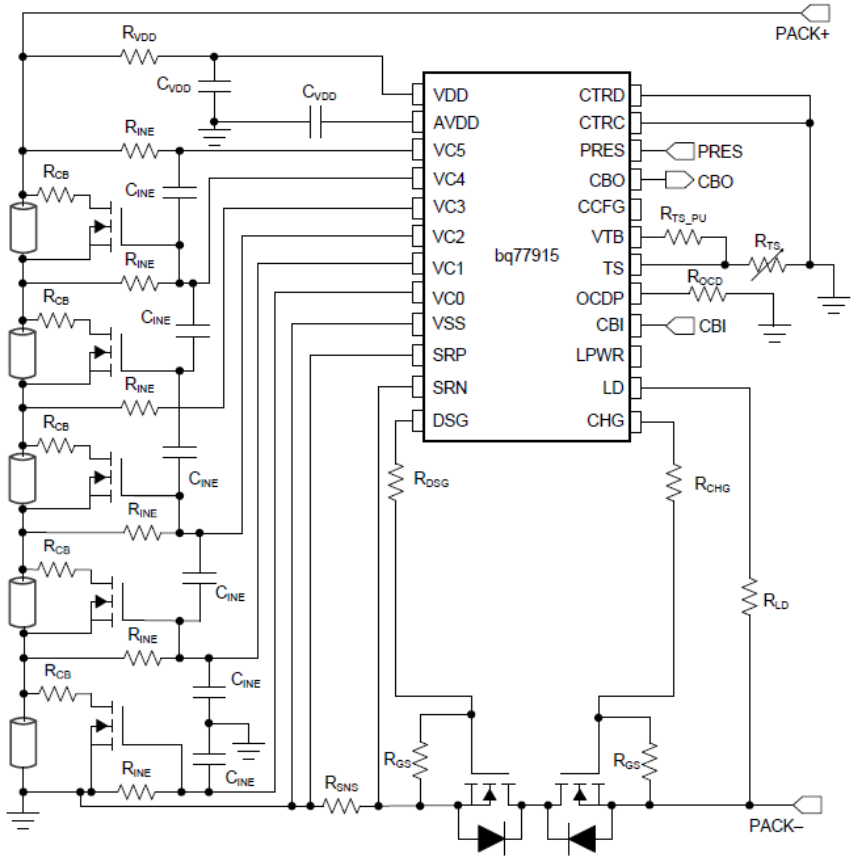


Figure 8. Cell Balancing with External MOSFETs

Cell balance start with voltage

- At lower voltages, cells must be separated by the threshold or greater

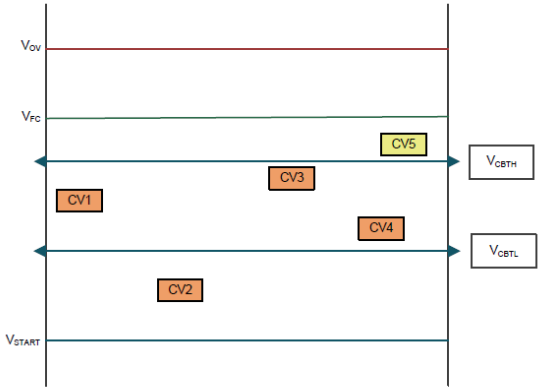
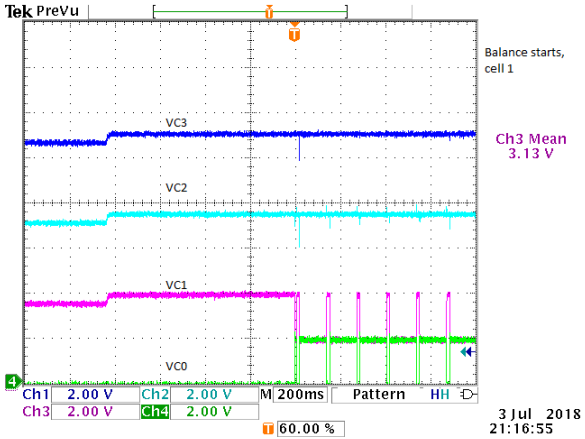
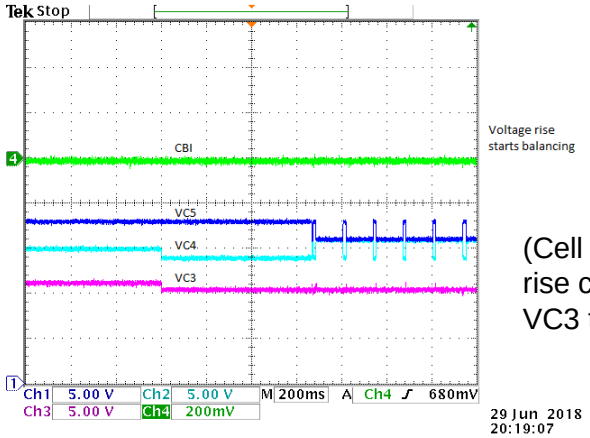


Figure 7. Cell-Balancing Algorithm

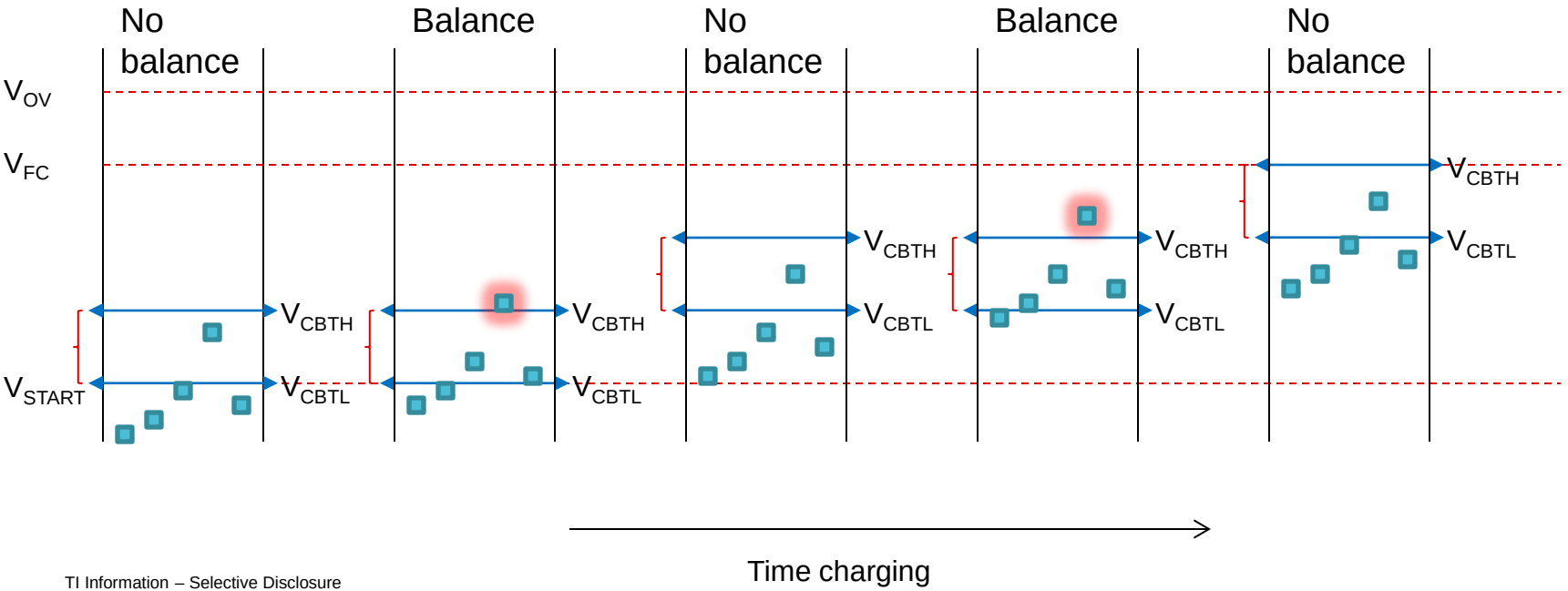




(Cell 5 voltage rise causes VC4, VC3 to drop)

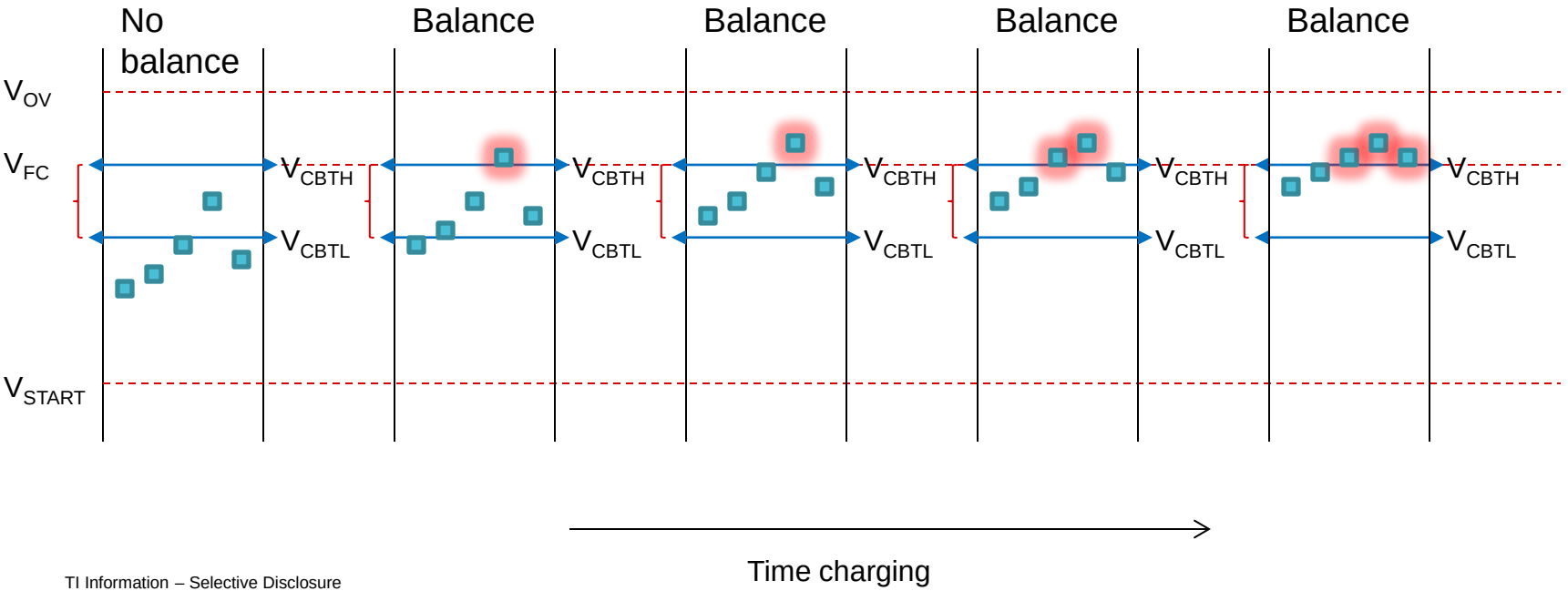
Thresholds will advance as cell voltages rise

- Balance may start and stop during charge



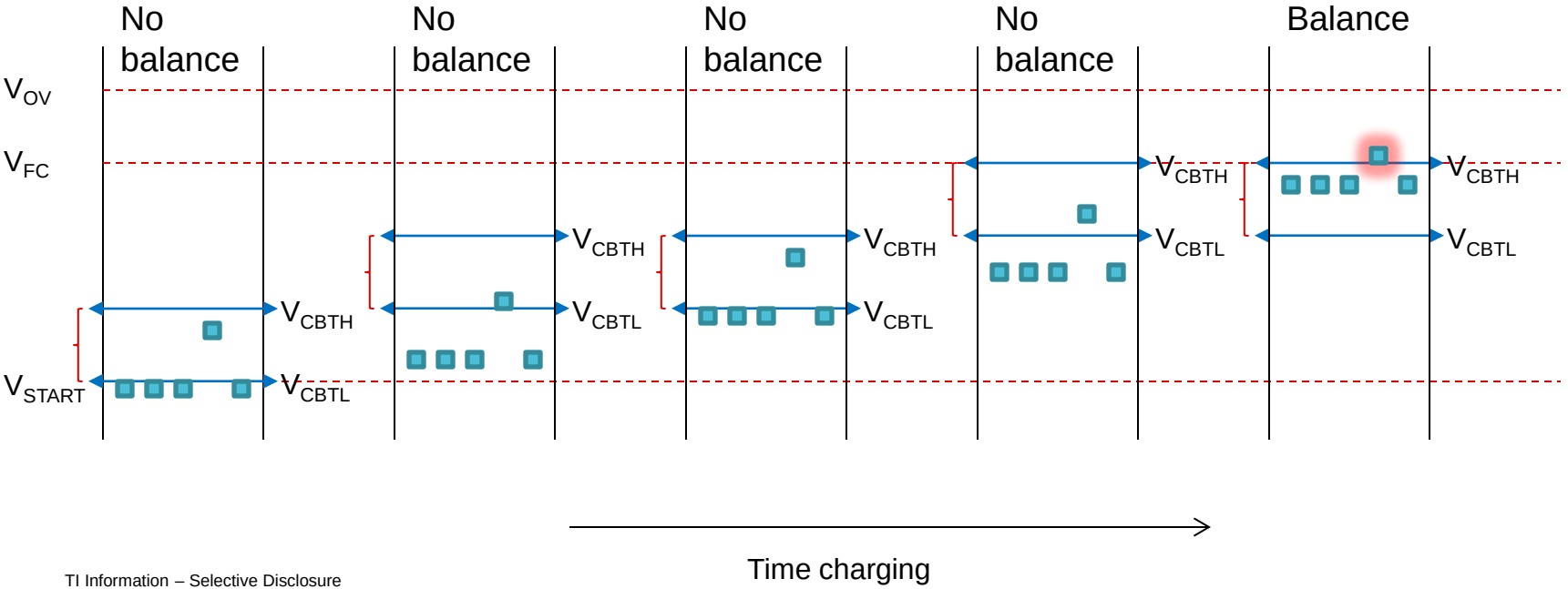
Cells above V_{FC} balance

- Balance continues with charge current



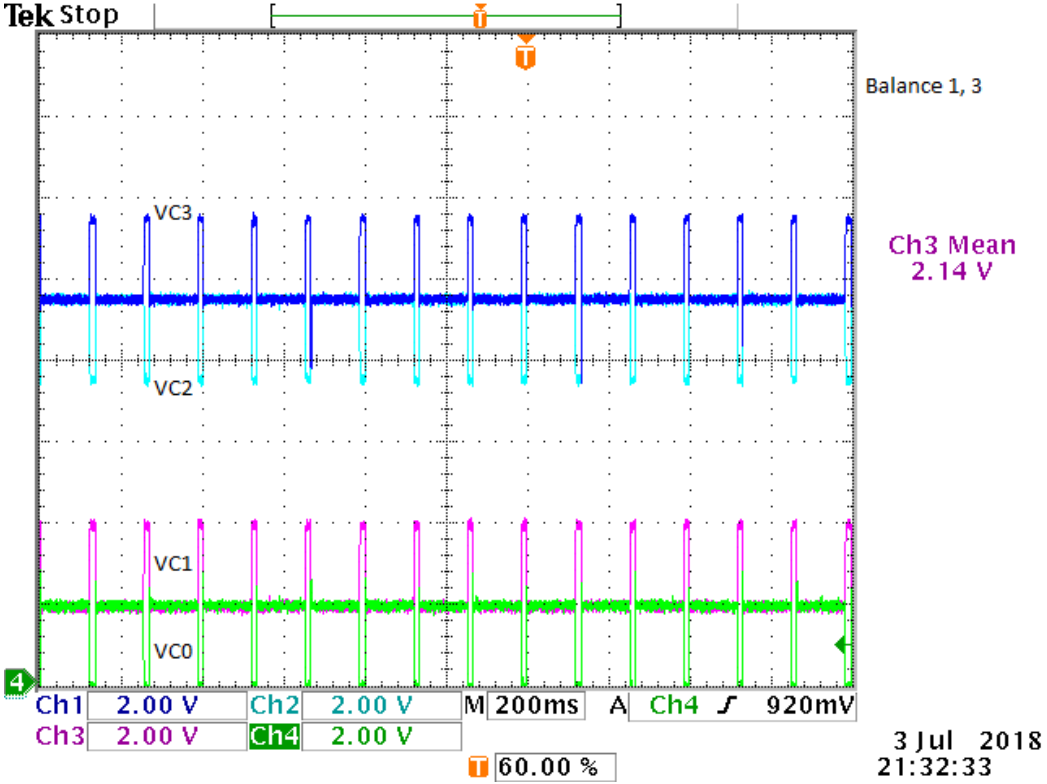
Well matched cells don’t balance

- Cells above V_{FC} will balance
- Balance stops when current drops sufficiently



Non-adjacent cell balancing

- Cells will balance simultaneously when not adjacent
  - Any 1, 3, 5
  - 2 and 4



Adjacent cells balancing

- Adjacent cells won't balance simultaneously
  - Typically important for differential voltage limit on inputs, but bq77915 does not have such limit
  - Important to allow signal for external balancing
- The part will duty cycle between odd and even cells when balancing adjacent cells is required

			MIN	MAX	UNIT
V_I	Input voltage	VDD, VC5, VC4, VC3, VC2, VC1, CTRD, CTRC	–0.3	36	V
		LD	–30	20	V
		PRES	–0.3	36	V

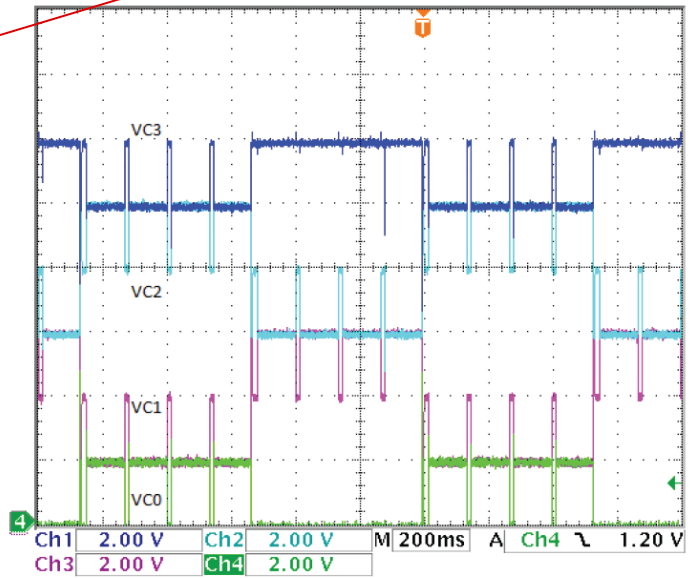
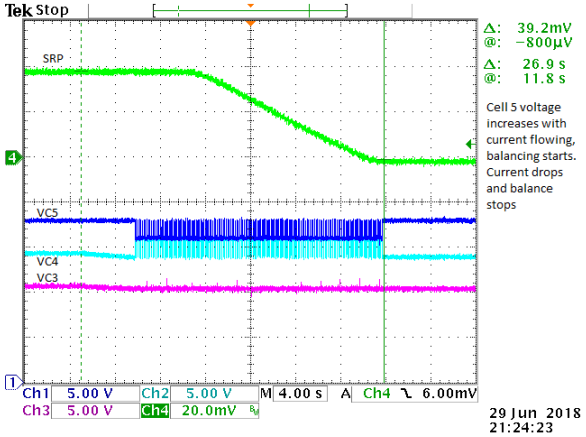


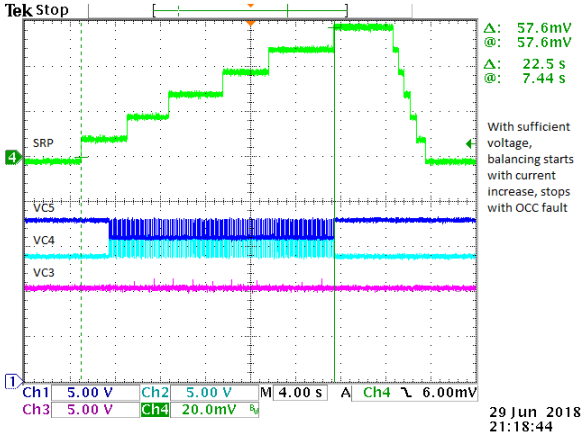
Figure 6. Balancing cells 1, 2, and 3

t_{BAL}	Odd and even cell group balancing duration		521	ms

Balance stop

- Balance will start with current and sufficient voltage difference
  - Stops when current drops below state comparator level
- With sufficient voltage difference
  - Balance starts with current application
  - Stops with certain faults, here simulated OCC
  - Does not resume on current drop, fault must be recovered





Balance control when stacking

- Balance is manually controlled by bottom part CBI
- Balance command is communicated up the stack by CBO to next CBI
  - CBO is a current sink, current is limited
  - Use 10k nominal resistor for isolation

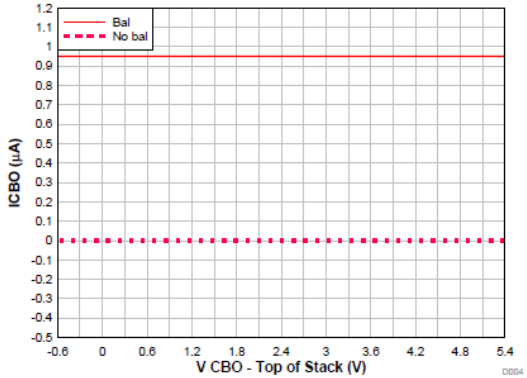
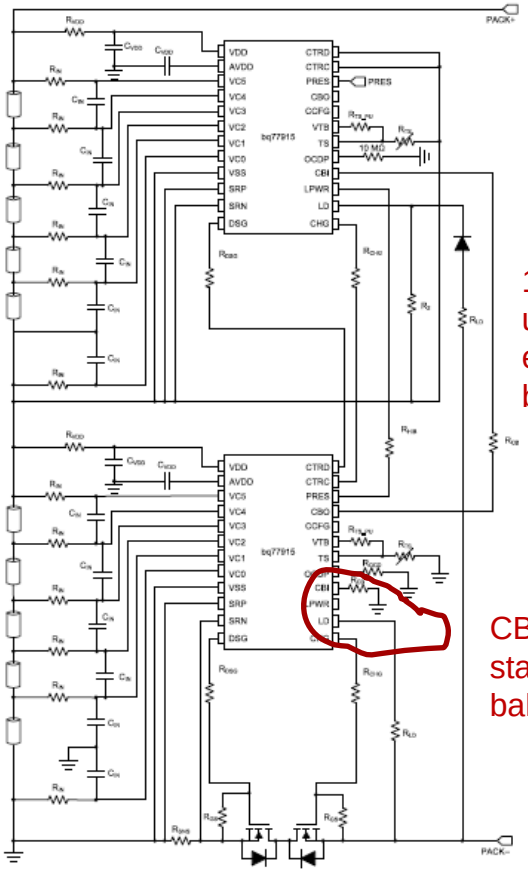


Figure 4. CBO Current Input at 18 V



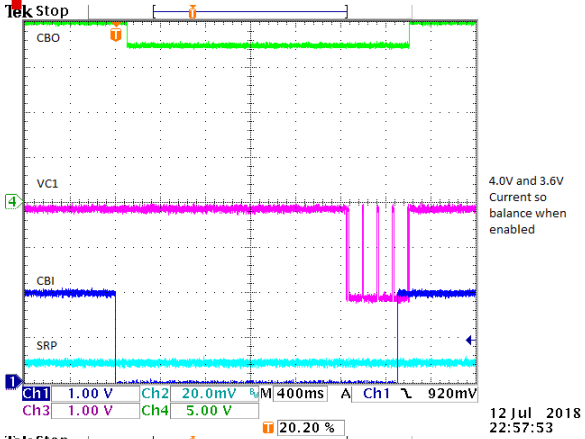
10k CBO to upper CBI enables balancing up

CBI enables stack balancing

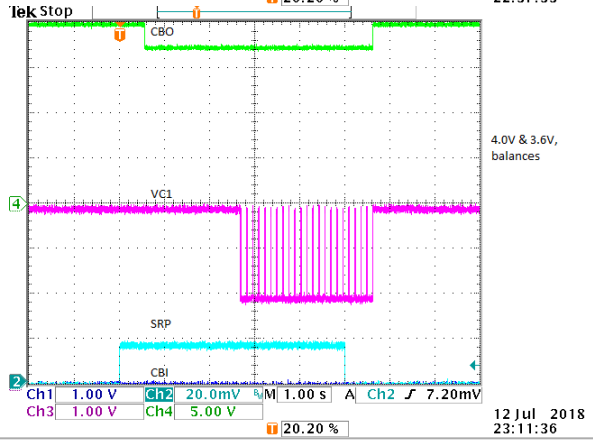
Figure 19. 10-Series Configuration with Internal Cell Balancing and HIBERNATE Mode Enabled

CBO output control for upper part

- When no faults
- CBI signals CBO with charge current

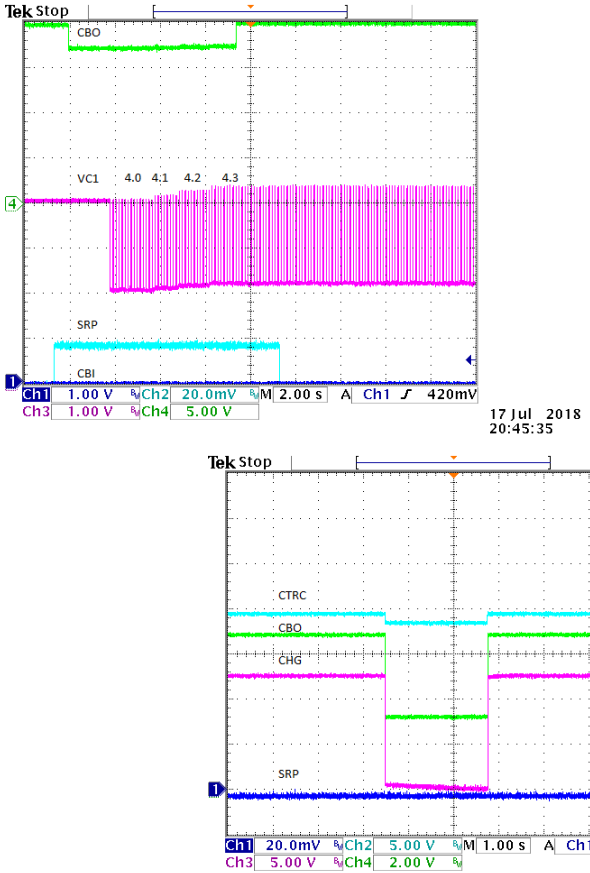


- Charge current flow signals CBO with CBI low



Balance in OV

- OV will stop balance for upper devices
- Cell will balance in OV
  - CBI required
  - Current not required
  - Balance continues until the cell voltage drops to V_{FC} or $V_{OV} - V_{HYS\_OV}$, whichever occurs earlier.
- If upper device has OV, CHG low
  - CTRC low on lower device sets CBO low even with no current so upper device can balance the OV cell(s)



Cells above OV balance

- Balance continues until V_{FC} or OV removed
- Current stops with OV