

Sample &

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CSD18535KCS

SLPS531 - MARCH 2015

CSD18535KCS 60 V N-Channel NexFET™ Power MOSFET

T₄ = 25°C

Technical

Documents

1 Features

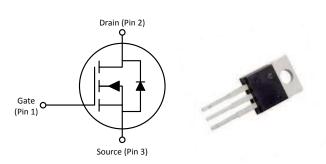
- Ultra-Low Q_q and Q_{qd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 60 V, 1.6 m Ω , TO-220 NexFETTM power MOSFET is designed to minimize losses in power conversion applications.



Product Summary TYPICAL VALUE UNIT

Support &

Community

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Tools &

Software

- A	-			
V _{DS}	Drain-to-Source Voltage	60		V
Qg	Gate Charge Total (10 V)	63	nC	
Q _{gd}	Gate Charge Gate-to-Drain	10.4	nC	
Б	Drain-to-Source On-Resistance	$V_{GS} = 4.5 V$	2.3	mΩ
R _{DS(on)}	Drain-to-Source On-Resistance	$V_{GS} = 10 V$	1.6	mΩ
V _{GS(th)}	Threshold Voltage	1.9		V

Ordering Information⁽¹⁾

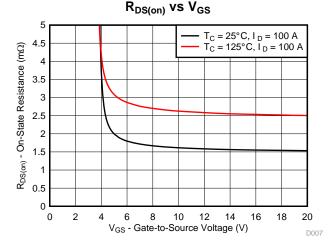
Device	Package	Media	Qty	Ship
CSD18535KCS	TO-220 Plastic Package	Tube	50	Tube

(1) For all available packages, see the orderable addendum at the end of the data sheet.

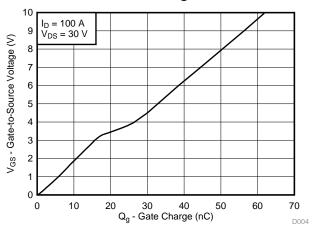
Absolute Maximum Ratings

T _A = 2	5°C	VALUE	UNIT				
V_{DS}	Drain-to-Source Voltage	60	V				
V_{GS}	Gate-to-Source Voltage	±20	V				
	Continuous Drain Current (Package limited)	200					
I _D	Continuous Drain Current (Silicon limited), $T_{C} = 25^{\circ}C$	279	A				
	Continuous Drain Current (Silicon limited), $T_{C} = 100^{\circ}C$	197					
I _{DM}	Pulsed Drain Current ⁽¹⁾	400	А				
PD	Power Dissipation	300	W				
T _J , T _{stg}	Operating Junction and Storage Temperature Range	-55 to 175	°C				
E _{AS}	Avalanche Energy, single pulse I _D = 111 A, L = 0.1 mH, R _G = 25 Ω	616	mJ				

(1) Max $R_{\theta JC} = 0.5^{\circ}C/W$, pulse duration $\leq 100 \ \mu s$, duty cycle $\leq 1\%$



Gate Charge



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

TEXAS INSTRUMENTS

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4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
STATIC	CHARACTERISTICS		i		
BV _{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 V, I_D = 250 \mu A$	60		V
I _{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0 V, V_{DS} = 48 V$		1	μA
I _{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0 V, V_{GS} = 20 V$		100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.4 1.9	2.4	V
Р	Drain to Source On Registeres	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 100 \text{ A}$	2.3	2.9	mΩ
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 10 V, I _D = 100 A	1.6	2.0	mΩ
9 _{fs}	Transconductance	V _{DS} = 6 V, I _D = 100 A	263		S
DYNAMI	C CHARACTERISTICS		i.		
C _{iss}	Input Capacitance		5090	6620	pF
C _{oss}	Output Capacitance	V _{GS} = 0 V, V _{DS} = 30 V, <i>f</i> = 1 MHz	890	1150	pF
C _{rss}	Reverse Transfer Capacitance		24	31	pF
R _G	Series Gate Resistance		0.8	1.6	Ω
Qg	Gate Charge Total (10 V)		63	81	nC
Q _{gd}	Gate Charge Gate-to-Drain		10.4		nC
Q _{gs}	Gate Charge Gate-to-Source		15.7		nC
Q _{g(th)}	Gate Charge at V _{th}		9.4		nC
Q _{oss}	Output Charge	V _{DS} = 30 V, V _{GS} = 0 V	140		nC
t _{d(on)}	Turn On Delay Time		9		ns
t _r	Rise Time	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 10 \text{ V},$	3		ns
t _{d(off)}	Turn Off Delay Time	$I_{DS} = 100 \text{ A}, \text{ R}_{G} = 0 \Omega$	19		ns
t _f	Fall Time		3		ns
DIODE C	HARACTERISTICS		·		
V _{SD}	Diode Forward Voltage	I _{SD} = 100 A, V _{GS} = 0 V	0.9	1.0	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 30 V, I _F = 100 A,	214		nC
t _{rr}	Reverse Recovery Time	di/dt = 300 A/µs	63		ns

5.2 Thermal Information

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

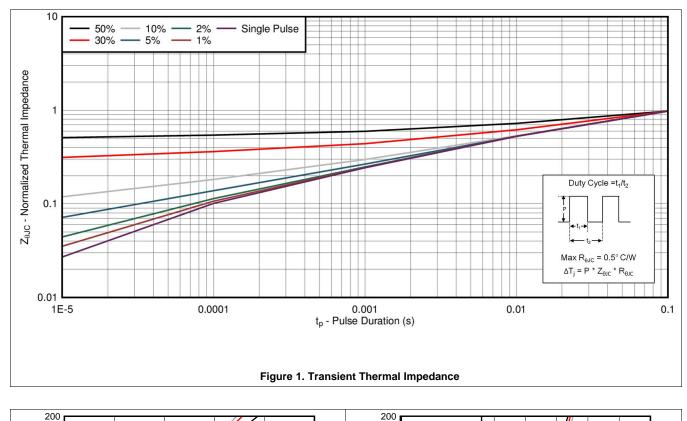
	THERMAL METRIC	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			0.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	°C/w

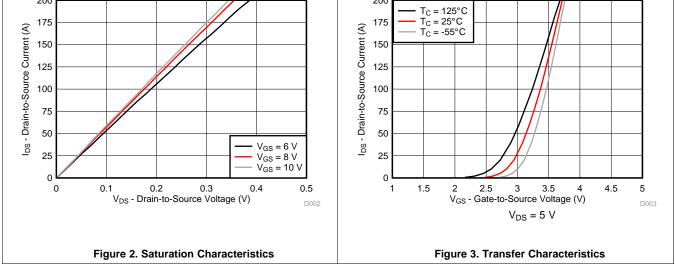
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5.3 Typical MOSFET Characteristics

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$





Product Folder Links: CSD18535KCS

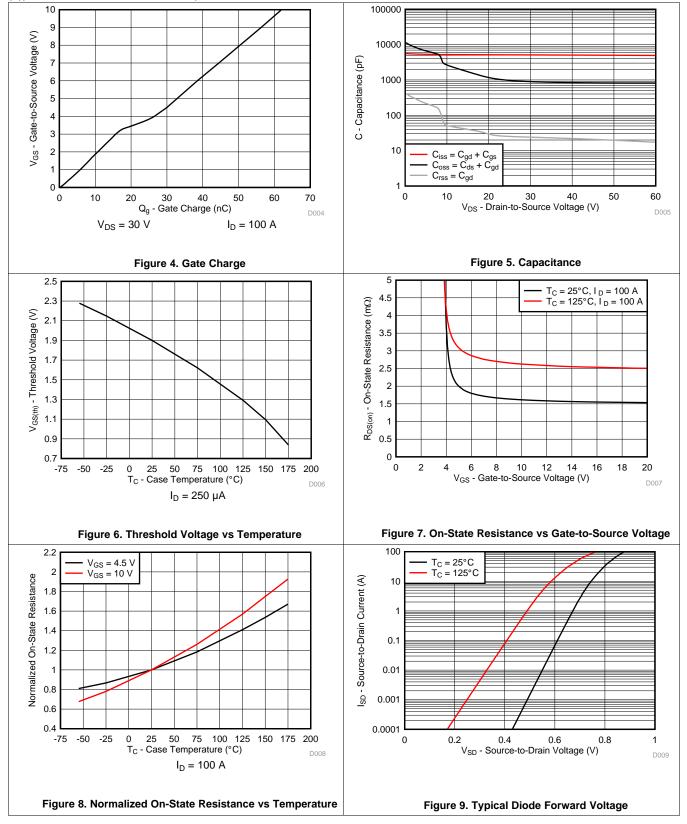


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Typical MOSFET Characteristics (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$



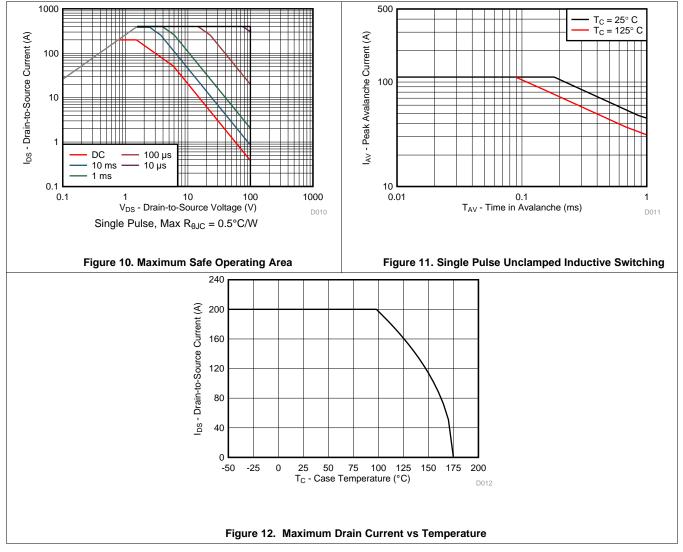


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Typical MOSFET Characteristics (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$





6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.



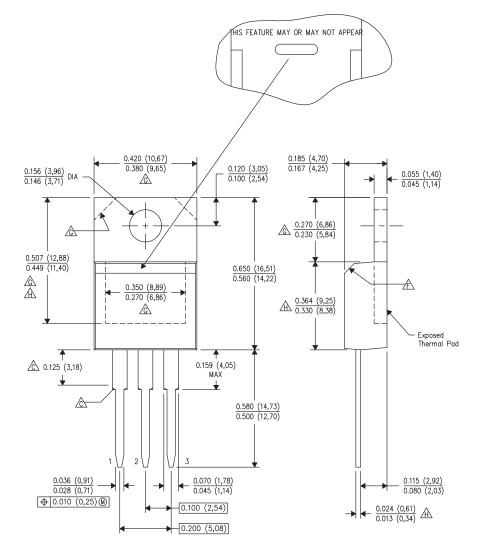
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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Lead dimensions are not controlled within this area. Chamfer may or may not appear D. All lead dimensions apply before solder dip.
- D. All lead dimensions apply before solder dip.
 E. The center lead is in electrical contact with the mounting tab.
- \triangle The chamfer is optional.
- Thermal pad contour optional within these dimensions.
- A Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

Pin	Configuration	n

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Position	Designation							
Pin 1	Gate							
Pin 2 / Tab	Drain							
Pin 3	Source							



9-Apr-2015

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CSD18535KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS Exempt)	CU SN	N / A for Pkg Type		CSD18535KCS	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

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