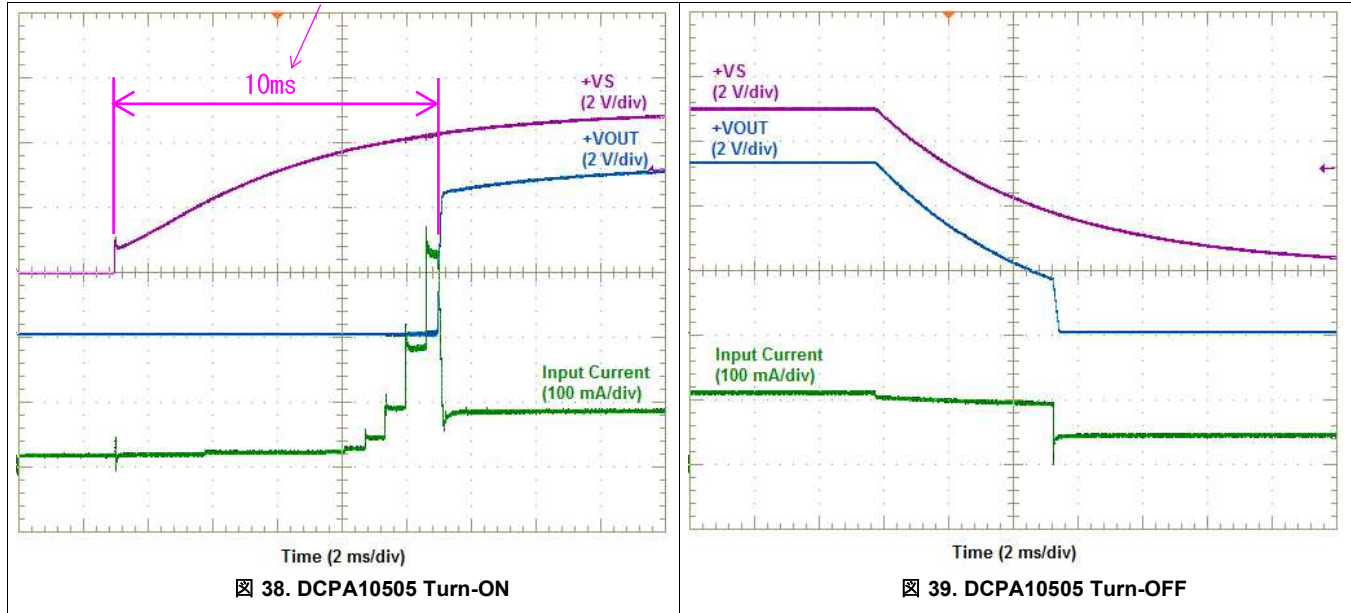


8.2.2 DCPA10505 Application Curves

delay of typically 10 ms before the output voltage begins to rise



8.2.3 Detailed Design Procedure

8.2.3.1 Input Capacitor

For all DCPA1, 5-V input voltage designs, select a 2.2- μ F low-ESR ceramic input capacitor to ensure a good startup performance.

8.2.3.2 Output Capacitor

For any DCPA1 design, select a 1.0- μ F low-ESR ceramic output capacitor to reduce output ripple.

8.2.3.3 SYNC_{IN} Pin

In a stand-alone application, it is recommended to connect this pin to the input side common, $-V_S$.

8.2.4 PCB Design

The copper losses (resistance and inductance) can be minimized by the use of mutual ground and power planes where possible. If that is not possible, use wide traces to reduce the losses. If several devices are being powered from a common power source, a star-connected system for the traces must be deployed. Do not connect the devices in series, because that type of connection cascades the resistive losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses. See the [PCB Layout](#) section for more details.

9 Power Supply Recommendations

The DCPA1 is a switching power supply, and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to connect the power to the input of DCPA1 device. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.