A Novel Control Method For Interleaved Transition Mode PFC

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Abstract- **Interleaving architecture extends high performance, low cost, transition mode PFC to higher power levels. Because the existing Master Slave interleaving control requires a slave channel operating in DCM mode, switching loss and EMI noise are increased. In this paper, a novel interleaving control method is proposed without using the Master Slave concept. The proposed method is able to realize 180 degrees phase-shift as well as true transition mode operation to achieve the optimal system performance.**

I.   INTRODUCTION

In low power AC/DC applications, transition mode (TM) power factor correction (PFC) (also known as critical conduction mode (CRM) PFC) is widely used [1][2]. It utilizes the boost topology, as shown in Fig 1, operating at the boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In each switching cycle, the boost inductor starts charging from zero current. In this way, the diode reverse recovery problem can be solved and the diode reverse recovery related EMI noise also be reduced. Therefore, low cost, standard diodes can be used while maintaining low switching loss. At the same time, because of the large inductor ripple, less boost inductance is required. These low cost components makes transition mode PFC particularly attractive for commercial products.
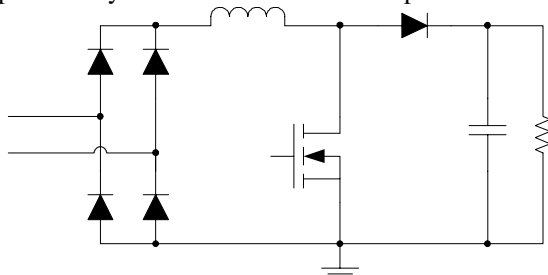

Figure 1. Transition Mode PFC

Because inductor current returns to zero in each switching cycle, constant on-time control can be used to achieve power factor correction. In this control method, MOSFET on-time is constant through the whole line cycle and each switching cycle is initiated by the inductor current zero crossing. Therefore, the inductor current is triangular in each switching cycle, as shown in Fig. 2. Based on the inductor current waveform shown in Fig. 2, the average inductor current can be calculated as

$$I_{avg}(t) = \frac{1}{2} I_{pk}(t) = \frac{1}{2} \frac{v_{in}(t)}{L} t_{on}$$

By keeping on-time constant through the whole line cycle, inductor average current is proportional to the input voltage along the whole line cycle, thus the power factor correction can be realized automatically without current sensing or close loop control.
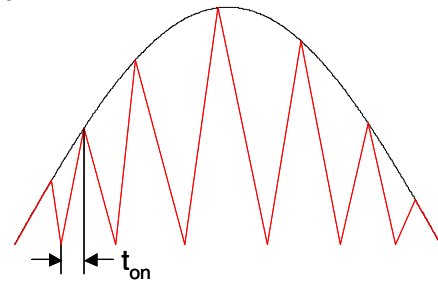

Figure 2. Typical TM PFC inductor current

Because the inductor operates at the boundary of CCM and DCM, its peak current will be two times as the input current, which gives extra current stress on both the power stage and the input EMI filter. Due to the large peak current and the associated large input EMI filter, TM PFC is limited to lower power levels, normally less than 300W. When higher power levels are required, CCM PFC becomes the natural choice, because of much less ripple current and less stress on the switching devices [3]. However, CCM PFC suffers from the high switching loss caused by the diode reverse recovery current. To ensure high efficiency, expensive SiC diodes, or lossless snuber circuits are required, which results in much higher system cost and less attractive in cost sensitive applications.

Instead of using a different topology, the power capability of TM PFC can be easily extended by paralleling two converters together. Furthermore, controlling two modules' inductor currents 180 degrees out of phase, the input and output ripple current can be greatly reduced. As shown in Fig 3, comparing to a single transition mode PFC, interleaving two transition mode PFC circuits reduces input current ripple by 75% and output current ripple by 35%. This ripple current cancellation effect allows the circuit to use smaller input and output filters, which further reduces system cost [4-6].
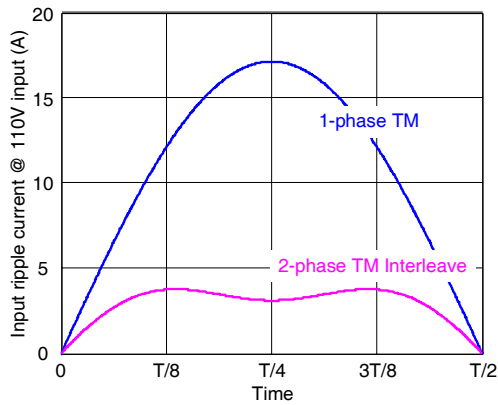
(a) Input ripple current at 100V input
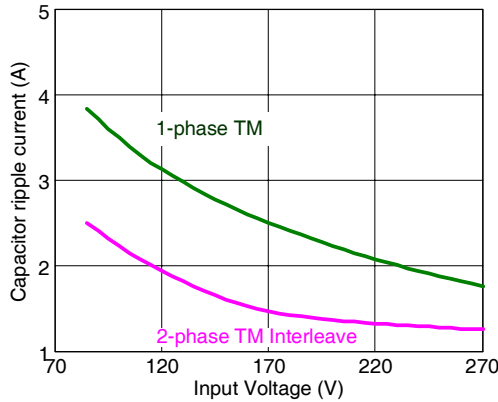
(b) Output ripple current at different input voltage

Figure 3. Ripple cancellation effects (calculation based on 600W design)

With the advancement of technology, high density and low profile became standard requirements for many applications, such as flat screen TVs and high-density adapters. The interleaving architecture uses two smaller inductors to replace the one bulky inductor in the single channel design. This dramatically improves the power supply form factor and makes it easier to meet low profile requirements. Moreover, at light load conditions, one of the power stages can be shut down to improve the light load efficiency. This makes interleaving more attractive to meet the stringent ENERGY STAR ® and 80 PLUS ® requirements.

II. CONTROL METHODS OF INTERLEAVED TM PFC

Interleaving control has been widely used in low power VRM applications to improve the power density and transient response. Because of the fixed switching frequency, interleaving control in low power DC/DC applications is relatively straightforward and easy to implement. Simply delaying half of the switching cycle, 180 degrees phase-shift can be realized. However, in TM PFC circuit, switching frequency varies along the whole line cycle. There is no fixed time relationship between two channel gate signals. Many research efforts have been performed to find a suitable method for interleaving control method in TM PFC. The most popular approach is the Master Slave approach [7-10].

A. MASTER SLAVE APPROACH

As mentioned in its name, the Master Slave approach distinguishes the two parallel PFC channels as a master channel and a slave channel. The master channel is controlled by its own constant on-time controller to achieve transition mode operation and power factor correction. At the same time, the slave channel is controlled with the same on-time and is synchronized with the master channel with a 180 degrees delay. Because of variable switching frequency, the major challenge of this approach is to find the correct delay time to realize 180 degrees phase-delay.

The concept of Master Slave control is to detect the switching cycle of the master channel and translate it into a half switching cycle delay time. And use this delay time to synchronize the slave channel. The control block diagram of the Master Slave approach is shown in Fig. 4. A master channel TM PFC is operating as an independent converter with its own fixed on-time controller. A computation block stores the master channel switching cycle information, and divide by two to create a half switching cycle delay time. After the half switching cycle delay time, the slave channel MOSFET is turned on with the same amount of on-time as the master channel. Considering the adjacent two switching cycles are nearly identical, this control method turns on the Slave channel with 180 degrees delay from the Master channel.
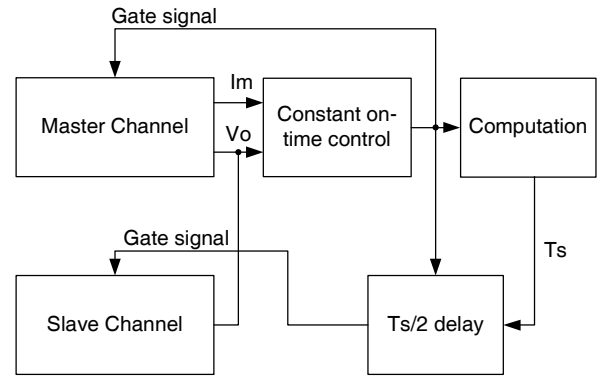
(a) Block diagram
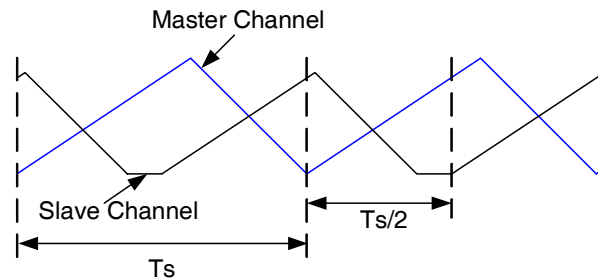
(b) Typical inductor currents waveforms

Figure 4. Master Slave interleaving control

This Master Slave control strategy, while relatively straightforward, has some clear drawbacks. Because of practical circuit component tolerances, two channels on-time can not be exactly the same. Because the master channel is controlled by its own constant on-time controller, it can always operate in transition mode. However, the slave channel

is forced to have the same switching frequency as the master channel. If slave channel has an on-time longer than the master channel, due to components tolerances, the slave channel won't have enough time to discharge the inductor and inductor current becomes continuous conducting. This not only increases the switching loss of the slave channel, the current sharing between two channels becomes unpredictable and the slave channel could have much larger current stress. To prevent slave channel from entering CCM mode, which is also extremely dangerous for transition mode PFC due to the low cost diode, the slave channel has to use less on-time. In this way, slave channel always demands higher switching frequency comparing with the master channel, and the slave channel always operates under DCM conditions.

In TM PFC circuits, due to the resonance between the boost inductor and MOSFET junction capacitors, the energy stored in the MOSFET junction capacitor can be recovered. In DCM mode, all the energy stored in the junction capacitor will be dissipated in the MOSFET, which causes extra switching loss and reduces the overall system efficiency. Moreover, in DCM mode, the discharge of the junction capacitor through MOSFET causes much higher dv/dt and generates extra EMI noise and further detriments to the system performance.

From the above discussion, the major issue of the Master Slave architecture is that because the slave channel is forced to have the same switching frequency as the master channel, and the slave channel operates under DCM condition.

B. Natural Interleaving^{TM} Approach

With the constant on-time control, TM PFC has its own natural switching frequency, which can be defined as

$$f_s(t) = \frac{1}{t_{on}} * d(t)$$

Here, $d(t)$, is the duty cycle along the power line cycle. According to the volt-second balancing of the boost inductor, this duty cycle can be calculated as

$$d(t) = 1 - \frac{v_{in}(t)}{V_o}$$

Here, $v_{in}(t)$, is the instantaneous value of the rectified input voltage and V_o is the output voltage.

Based on these two equations, the switching frequency of transition mode PFC is only determined by the input voltage, output voltage and on-time. Because the two channels share the same input and output voltage, as well as the same on-time, theoretically, they should be running at the same switching frequency along the line cycle, and the phase relationship between these two channels should remain unchanged. However, due to the slight differences in MOSFET on-state resistance, inductor ESR, diode voltage drop, etc, the duty cycle of these two channels can't be exactly the same. Furthermore, because of design tolerance, the on-time of these two channels can't be exactly the same, either. All of these errors give two channels different natural switching frequencies. With different switching frequencies, 180 degrees

phase-shift between these two channels can't be maintained. Thus, the key of the control strategy is to make these two channels has identical natural switching frequencies. Once the frequencies are the same, the phase relationship is going to be fixed, so that 180 degrees phase-shift can be realized.

From the above equations, the natural switching frequency can be adjusted either by the on-time or duty cycle. For constant on-time control, the duty cycle is determined by boost inductor volt-second balancing, and it couldn't be adjusted with transition mode operation. The only way of adjusting the switching frequency is to adjust two channels on-times individually.

According to this concept, the new control strategy, "Natural Interleaving", is proposed [11]. The control block diagram is shown in Fig.5. It is constructed from three blocks: phase relationship detector, gain modulator and on-time generator.

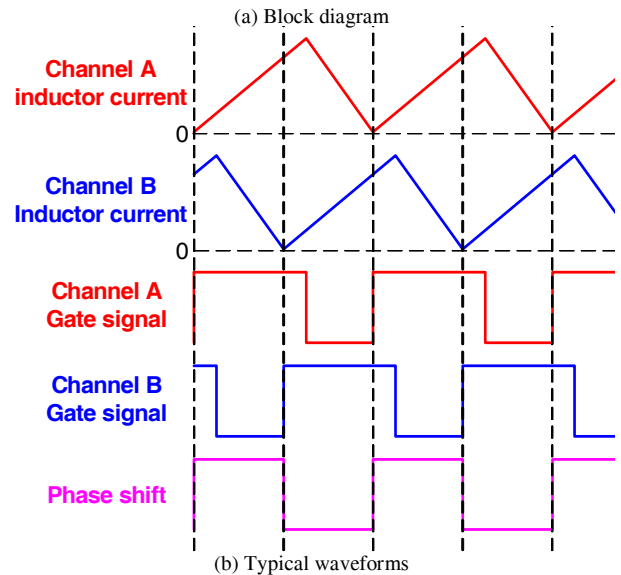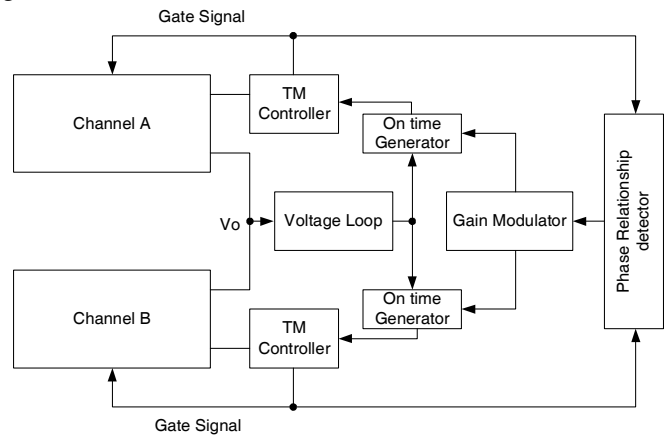(a) Block diagram

(b) Typical waveforms
Figure 5. Natural Interleaving Control (patent pending)

Initially, two PFC channels operate independently with its own transition mode controller. The MOSFET turning on is triggered by the inductor zero crossing signal and the MOSFET turning off is controlled by the on-time generator. As shown in Fig. 5 (b), the turn-on edge of each channel gate signal is used to generate a phase-shift signal. When

the channel A MOSFET turns on, this phase-shift signal becomes high; when the channel B MOSFET turns on, the phase-shift signal becomes low. This phase-shift signal will have both a variable frequency and variable average DC level if channel A and channel B are operating at different switching frequencies. However, if the two gate signals are 180 degrees out of phase, phase-shift signal would have a 50% duty cycle. Once the phase-shift signal continuously achieves 50% duty cycle, the two channels operate with same switching frequency and operate 180 degrees out of phase. Therefore, the control target is to maintain the phase-shift signal a constant 50% duty cycle.

As shown in Fig. 5 (a), the phase relationship detector generates the phase-shift signal based on two channels gate signals. Then, the phase-shift signal is filtered into a DC voltage. For 5V logic and 50% duty cycle, this DC voltage should be 2.5V. After filtering, this DC voltage is compared with a 2.5V reference to adjust the two channels on-times through the gain modulator. By increasing one channel's on-time and decreasing the other channel's on-time, the switching frequency of these two channels can be slightly modified, and in turn, the phase relationship can be adjusted. Through this compensation, the final results are two channels have exactly the same switching frequency and the phase relationship keeps 180 degrees.

Without the differentiation of master and slave channel, "Natural Interleaving" allows both channels to operate in transition mode to realize the full benefits of TM PFC: no diode reverse recovery loss, recovering energy from the MOSFET junction capacitor, and less EMI noise.

Because both channels operate under transition mode conditions, with same on-time, the current sharing between two channels is purely determined by inductor tolerances. By controlling the tolerance of boost inductors, good current sharing can be achieved.

III. EXPERIMENTAL RESULTS

To verify the theory of operation, this Natural Interleaving control method has been implemented in a 600W PFC design, with universal input voltage range. Because of interleaving, the total ripple current is greatly reduced, as shown in Fig. 6 (a), (b). There is slightly difference in two channel inductor values. Therefore, the inductor currents are not exactly the same. Expanding these waveforms, showing in Fig 6. (c), (d), we can see that both channels operate in transition mode condition and keep 180 degrees phase-shift along the whole line cycle.

(a) 100V input (2ms.div)

(b) 230V input (2ms/div)

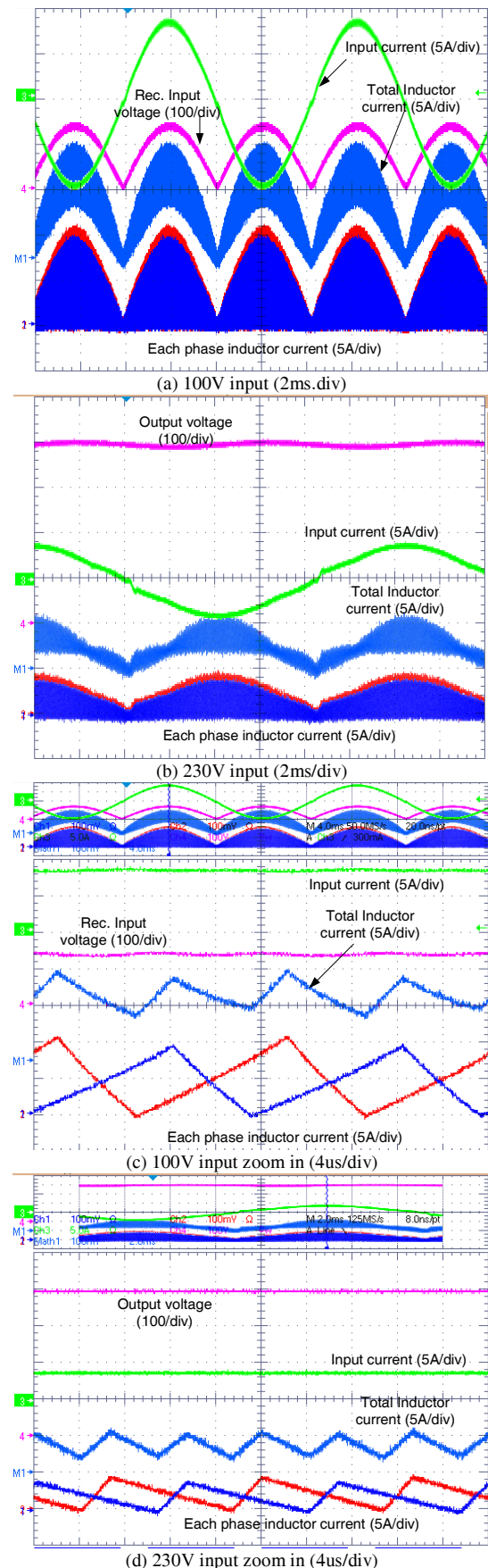(c) 100V input zoom in (4us/div)

(d) 230V input zoom in (4us/div)

Figure 6. Experimental waveforms of interleaved TM PFC

Interleaving control not only reduces input and output ripple current, it also allows the system to implement phase management, shutting down one of the channels to improve light load efficiency. As shown in Figure 7, more than 5% efficiency improvement can be achieved at both high and low input line conditions by using the phase management, which is quite useful for meeting 80 PLUS® design requirements.
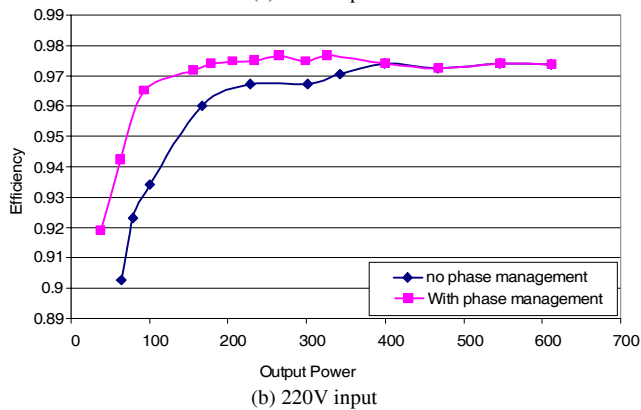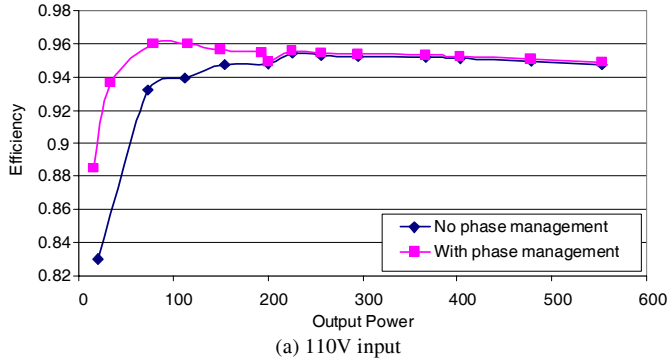

(a) 110V input

(b) 220V input

Figure 7. Efficiency measurement with phase management

IV. SUMMARY

Interleaving technology allows power supply designers to use high performance low cost transition mode PFC circuits to higher power levels. However, the variable switching frequency makes it difficult to control the phase relationship of two interleaved channels. For the conventional Master Slave interleaving method, the slave channel always operates in DCM mode and suffers extra switching losses and higher EMI noise. In this paper, a new Natural Interleaving method has been proposed. Through adjusting the on-time of two interleaved channels, the natural switching frequency of each channel can be slightly adjusted. In turn, the switching frequency of two channels becomes the same as the average of two natural switching frequencies, allowing TM operation with a well-controlled phase relationship at 180-degree for optimum ripple cancellation and system efficiency.

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