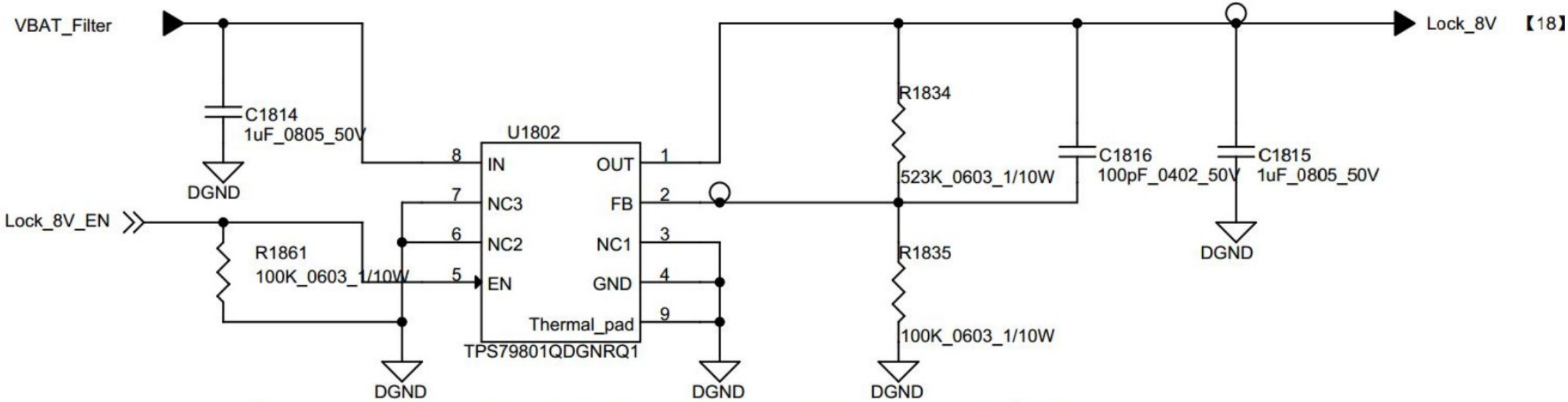
VOUT is existed before EN enabled, can you explain?



VOUT = [(523 +100)/100] * 1.275 + (523/5000) = 8V

Jason Song *2 天前*

TI__Mastermind 20210 points

Hi Lin,

How fast is the Vin rising in the scope-shot? It seems to me that the rising edge of Vin is coupling to the output of the LDO. One way to confirm this is to try to create a slower ramp on the Vin of the LDO and observe if Vout is still doing this. Do you think that is something you could try on your board?

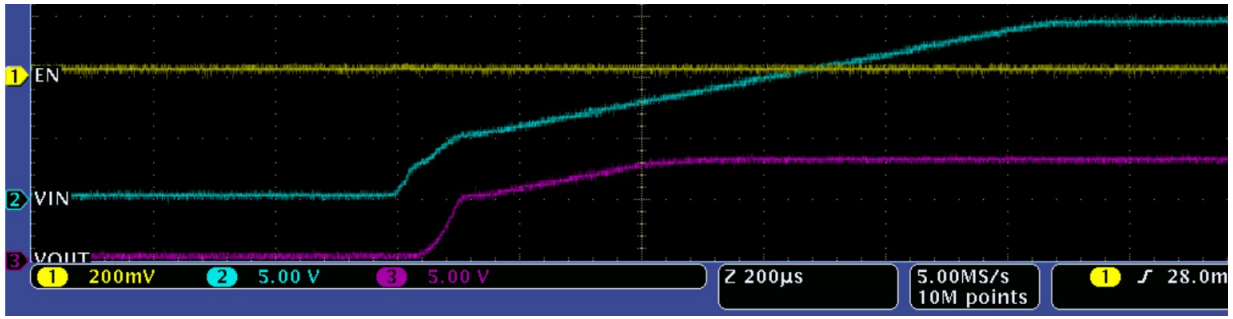
In addition, is there any other possible charging path that could be turned on with the input of the Vin?

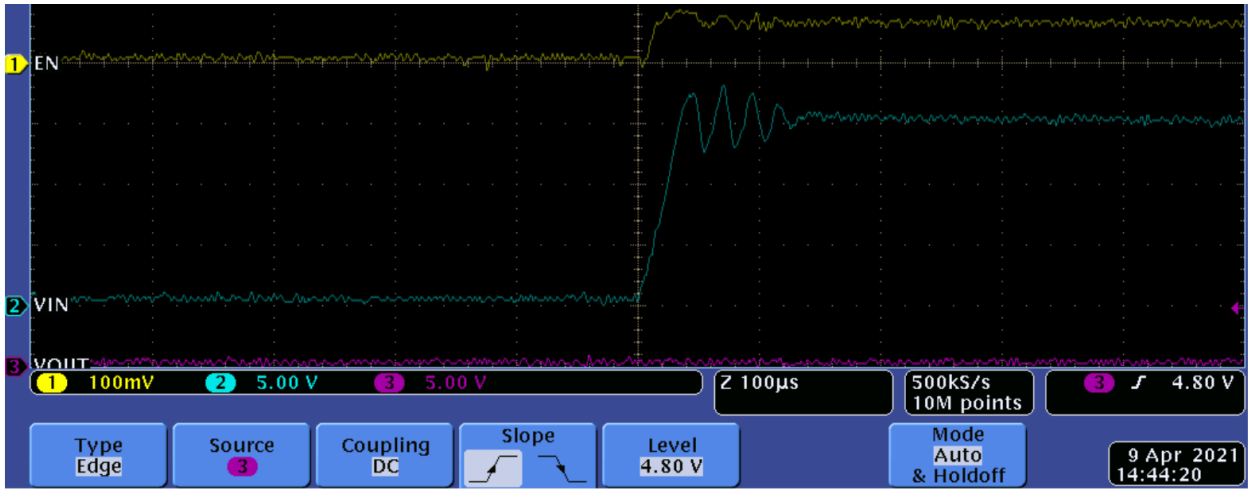
Do you have any type of load on the output during the startup? If so, what's the load?

Regards,
Jason Song

[SL] To verify Vin rising, power net(VBAT_filter) and load are now removed. LDO Vin is supplied directly through 15V DC source and Cin. Results are listed below:

Cin (uf)	Vin rising	Vout existed before EN enabled ?
4700	12 ms	Not existed
500	1 ms	Existed, see left figure
47	150 us	Not existed, see right figure





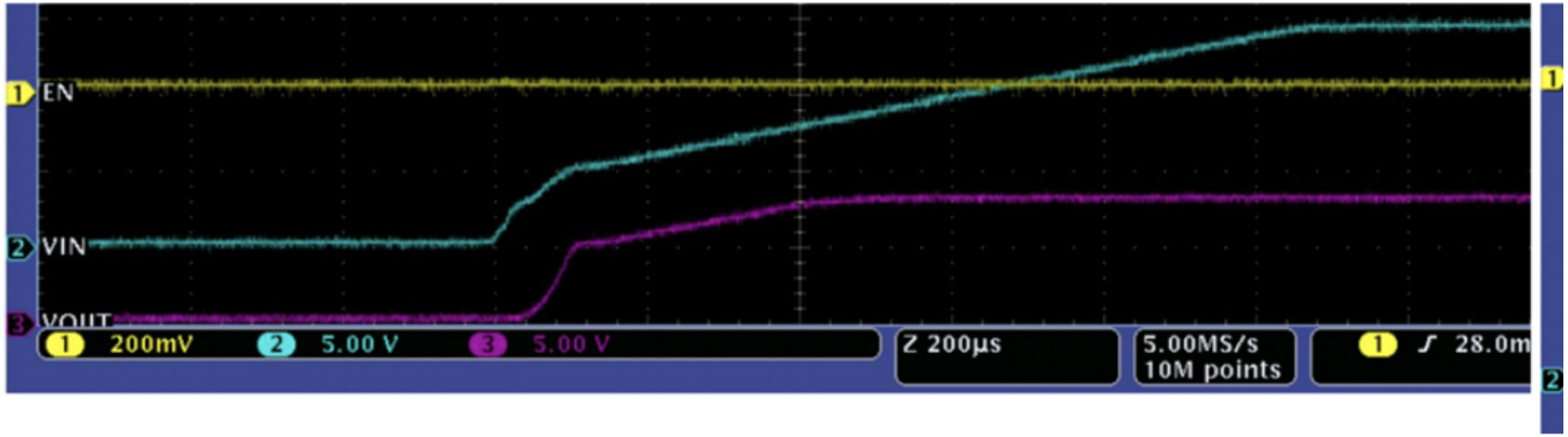
[SL] Cin seems critical, can you explain this? Are there any application hints about Cin selection?

Can you share Vih,min and Vil,max of EN pin?

Jason Song *4 小时前 in reply to LIN SUN* — TI__Mastermind 20240 points

Hi Lin,

Thanks for taking additional mesasurements. I have a question about the latest scope shot you provided.



For this one, it's very different than the previous one you shared, it seems to me that Vin and EN are connected together, and the output is doing a normal startup and the output has reached the set target. Will you help me to understand the difference between this one and the previous one?

One suggestion is to try to remove R1861 to see if it makes a difference.

Regards.

[SL] In this figure, EN is rising from 0V to 60mV(can be found in below figures, so R1861 is not removed). Vin is rising from 0V to 15V, Vout is rising from 0V to 8V. Obviously abnormal startup behavior. I'm afraid you have misunderstanding of this scope?

[SL] You once mentioned that Vin rising maybe the reason. So different Vin rising is tested. Results are listed below:

Cin (uf)	DC source V/I setup	Vin rising	Vout existed before EN enabled ?
4700uf	13V/0.2A	240ms	Not existed
4700uf	13V/2A	27ms	Not existed
4700uf	13V/5A	13.3ms	Not existed, see figure20
4700uf	9V/0.2A	192ms	Not existed
4700uf	9V/2A	18ms	Not existed
4700uf	9V/5A	7ms	Not existed, see figure21

This table shows that:

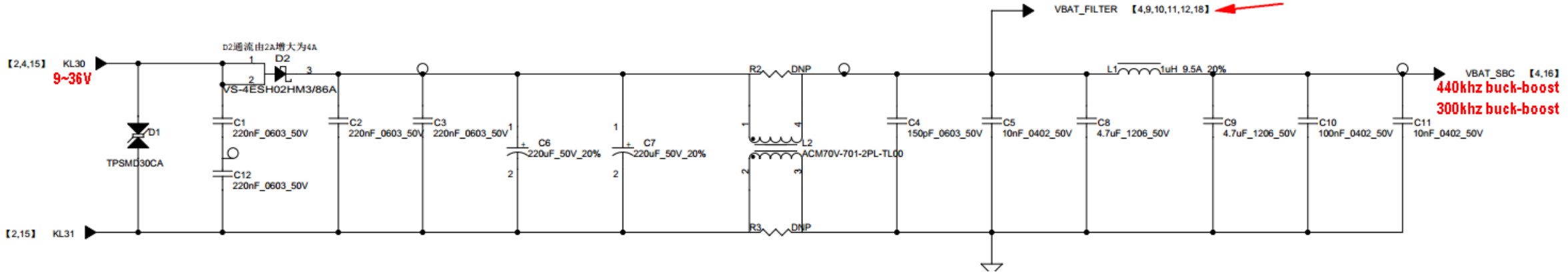
- ✓ *Vout is not existed for 4700uf capacitance.*
- ✓ *Even Vin rising is varying when DC source V/I setup changes, it has no influence on Vout existence.*
- ✓ *I think Vin rising seems to have nothing to do with Vout. Cin Capacitance maybe the reason. Capacitors varying from 1uf to 2200uf are tested in next table. Their results also support this idea.*

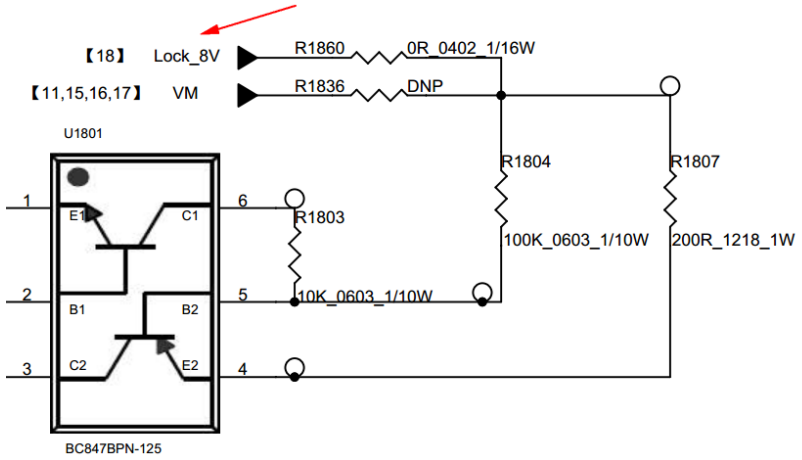
Cin (uf)	DC source V/I setup	Vin rising(ms)	Vout existed before EN enabled ?
2200uf	13V/0.2A	146	Not existed, see figure22
2200uf	9V/5A	3.4	Not existed, see figure23
1000uf	13V/0.2A	67	Not existed
1000uf	9V/5A	1.68	Not existed, see figure24
720uf	13V/0.2A	45	Existed 0.04V, see figure29
720uf	9V/5A	1.1	Existed 0.04V, see figure28
500uf	13V/0.2A	31	Existed 1.5V, see figure25
500uf	9V/5A	0.74	Existed 4V, see figure26
220uf	13V/0.2A	10	Existed 5V, see figure39
220uf	9V/5A	0.2	Existed 7V, see figure31
110uf	13V/0.2A	4.1	Existed 2V, see figure33
110uf	9V/5A	0.074	Existed 6V, see figure32
47uf	13V/0.2A	Vin has occalication, appro 0.12	Not existed, see figure34
47uf	9V/5A	Vin has occalication, appro 0.1	Not existed, see figure38
10uf	13V/0.2A	Vin has occalication, appro0.2	Not existed, see figure37
10uf	9V/5A	0.06	Not existed, see figure36
1uf	13V/0.2A	Vin is strange	Not existed, see figure41
1uf	9V/5A	Vin is strange	Not existed, see figure42

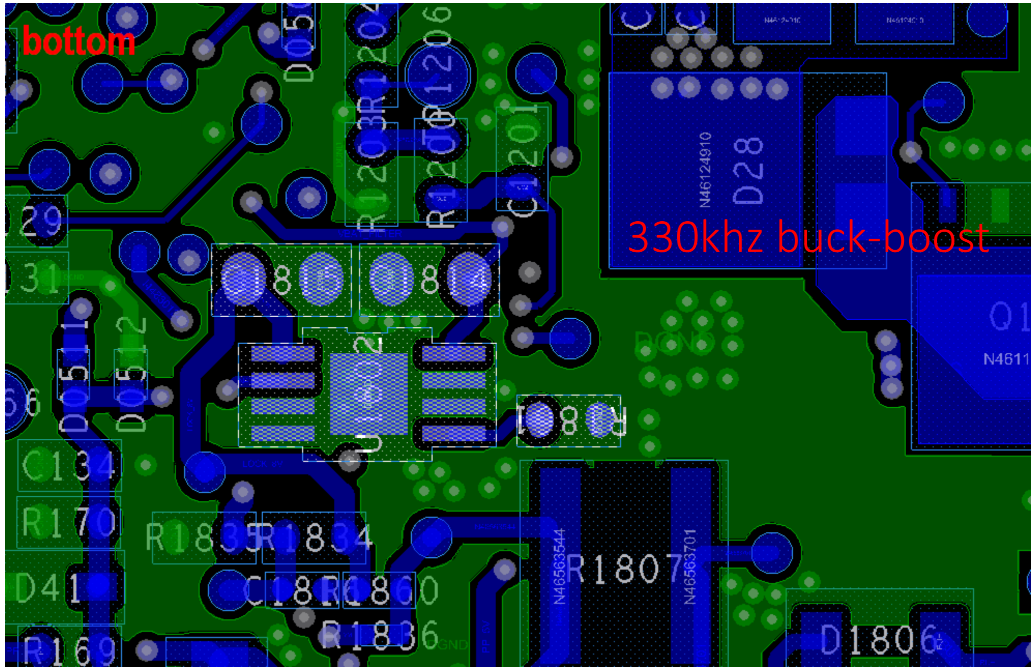
[SL] In my board, ldo Vin is supplied via net VBAT_FILTER. VBAT_FILTER comes from 9~36V KL30.

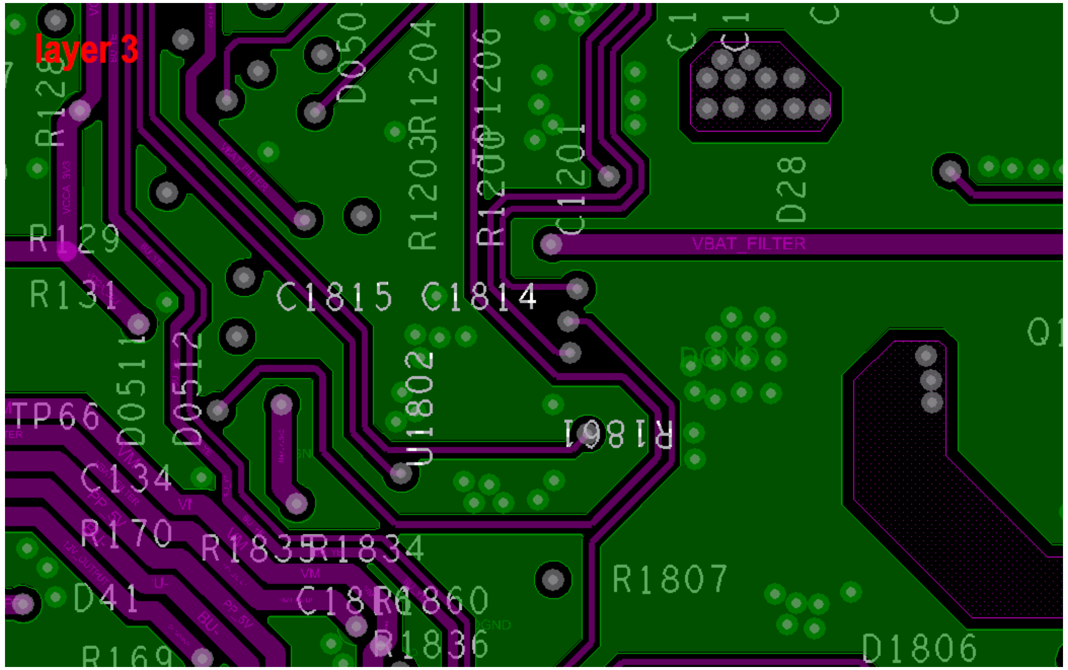
LDO load is mcu controlled pnp, it is used for detecting motor existence, load current is 8mA. This pnp works with LDO EN pin, simultaneously.

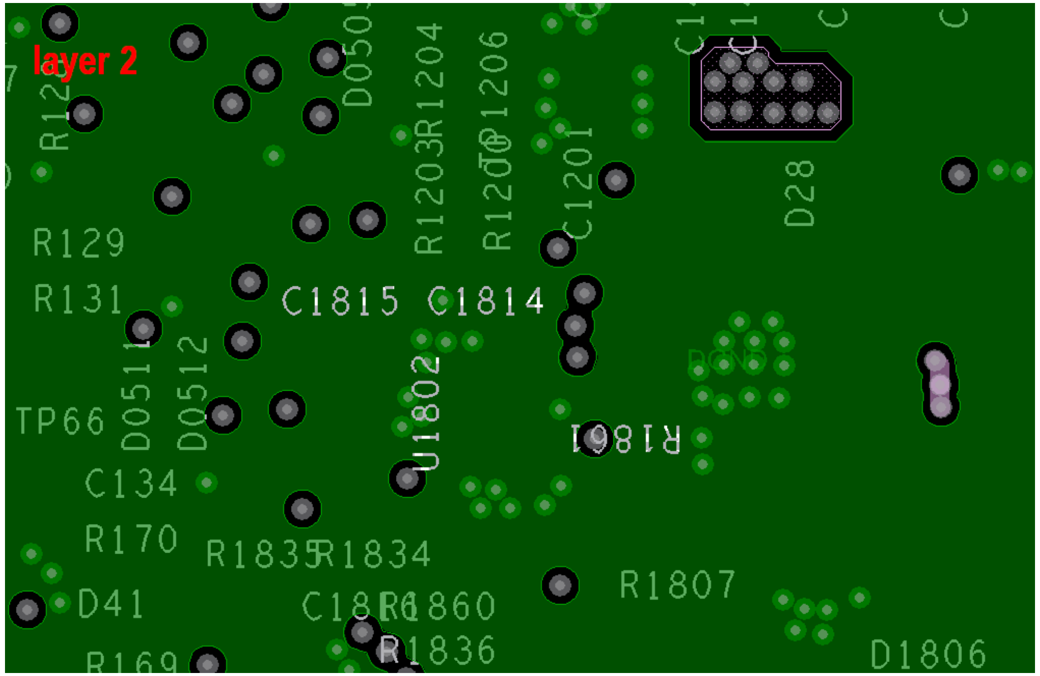
Layout also added in next page.






bottom
330khz buck-boost
D28
R1807
D1806
R1835
R1834
R1836
R170
C134
D41
R169
U1802


layer 3
R129
R131
C1815
C1814
R1861
TP66
C134
R170
R1835
R1834
R1807
D41
R1836
R169
D1806
U1802
D28
VBAT_FILTER


layer 2
R129
R131
C1815
C1814
TP66
C134
R170
R1835
R1834
R1807
D41
R1836
R169
D1806
U1802
R1861
D28

[SL] In brief, I think Cin capacitance is the reason. Can you explain and test on your develop board?

Can you share Vih,min and Vil,max of EN pin?

Please also have a look at Layout.

Hope to speak on phone if you can speak Chinese.