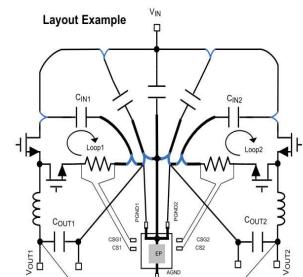
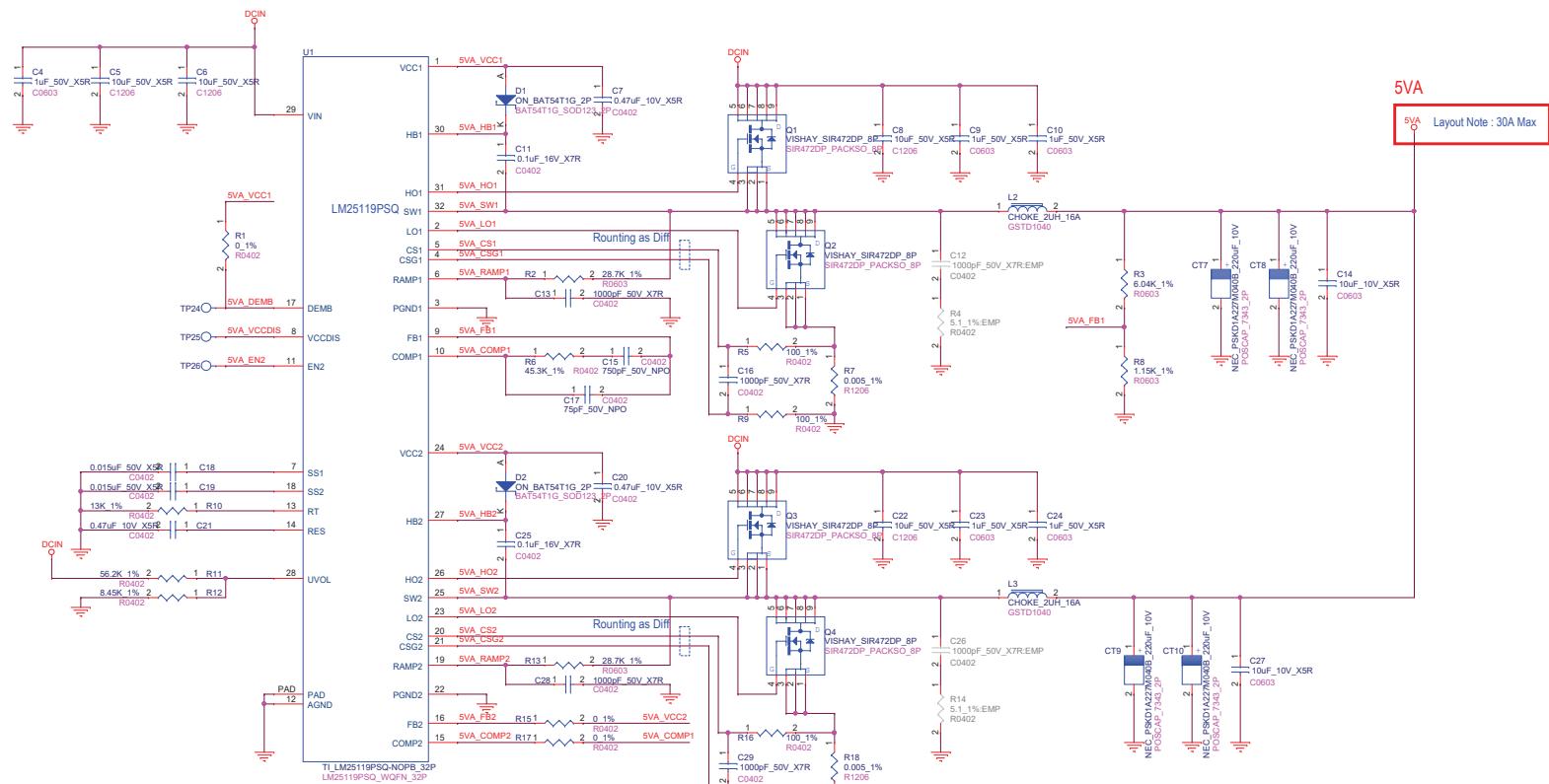


R1 =	59	kΩ
R2 =	11.30	kΩ
R3 =	3.48	kΩ
Rs =	15.00	kΩ
R5=	0	kΩ
C _{Timer} =	100.00	nF
C _{in} =	100	nF
C _{Gate} =	31	nF
C _{Load} =	220	μF

OVP Protect IC

Settings	Units
Typical Over-Current Threshold	16.00 A
Startup Delay Time	33.33 ms
Over-Current Fault Delay	18.18 ms
Upper OVLO Threshold	42.73 V
Lower OVLO Threshold	37.64 V
Upper UVLO Threshold	8.31 V
Lower UVLO Threshold	7.59 V



The bold lines indicate a solid ground plane. Make the traces to the widest and the shortest and use the star ground technique.

These lines indicate the high current paths. Make the traces as wide and short as possible.

These lines indicate the small signal paths. The traces can be narrow but keep them away from any radiated noise and away from traces that may couple noise capacitively.

These points require the maximum bypassing of the high frequency switching noise. Isolate each channel from the high frequency switching noise of the other channel.

Figure 23. Recommended PCB Layout