WIDE V_{IN} DC/DC Power Solutions
Reliable Power for Demanding Systems

LM5176 DC/DC Controller Design Tool

About | = Input Box | http://www.ti.com/product/lm5176 | TERMS OF USE

Step 1: Operating Specifications

Input Voltage - Min, $V_{IN(min)}$	**53.3**	**V**
Input Voltage - Nom, $V_{IN(nom)}$	**53.3**	**V**
Input Voltage - Max, $V_{IN(max)}$	**55**	**V**
Output Voltage, V_{OUT}	**52.65**	**V**
Full Load Output Current, $I_{OUT(max)}$	**2**	**A**
Switching Frequency	**250**	**kHz**
Frequency Set Resistor, R_T	33.2	kΩ

Step 2: Filter Inductor

Recommended Filter Inductance	5.0	µH
Inductance, L_F	**4.7**	**µH**
Inductor DCR	**3.5**	**mΩ**
Pk-to-Pk Ripple Current at $V_{IN(min)}$, ΔI_{L1}	0.5	A_{pk-pk}
Pk-to-Pk Ripple Current at $V_{IN(nom)}$, ΔI_{L2}	0.5	A_{pk-pk}
Pk-to-Pk Ripple Current at $V_{IN(max)}$, ΔI_{L3}	1.9	A_{pk-pk}
ΔI_L as a % at $V_{IN(min)}$	27	%
ΔI_L as a % at $V_{IN(nom)}$	27	%
ΔI_L as a % at $V_{IN(max)}$	96	%

Step 3: OCP, Sense Resistors, Slope Comp

Required $I_{OCP(MIN)}$ Setpoint at $V_{IN(nom)}$	**8.3**	**A**
Recommended Sense Resistance	10.0	mΩ
Sense Resistance, R_S	**10**	**mΩ**
Peak Inductor Current, I_{LPK}	9.9	A
Power Loss in Rs at Full Load (Max VIN)	0.00	W
Recommended SLOPE Capacitance	180	pF
SLOPE Capacitance, C_{SLOPE}	**270**	**pF**
$V_{IN(min)}$	8.3	A
$I_{OUT(typ)}$ at OCP Inception: $V_{IN(nom)}$	8.3	A
$V_{IN(max)}$	9.0	A
Set Const Current Loop Setpoint (?)	**2**	**A**
Output Leg Shunt Resistance, $R_{CS(out)}$	25	mΩ

Step 4: Output Capacitor

Output Voltage Ripple Spec	**120**	**mV_{pk-pk}**
Minimum Output Capacitance	22.0	µF
Output Capacitance, C_{OUT}	**60**	**µF**
Maximum Permitted ESR	219.4	mΩ
Output Capacitor ESR	**2**	**mΩ**
Resulting Output Voltage Ripple (max)	16	mV_{pk-pk}
Output Capacitor RMS Current (max)	0.6	A (rms)

Step 5: Input Capacitor

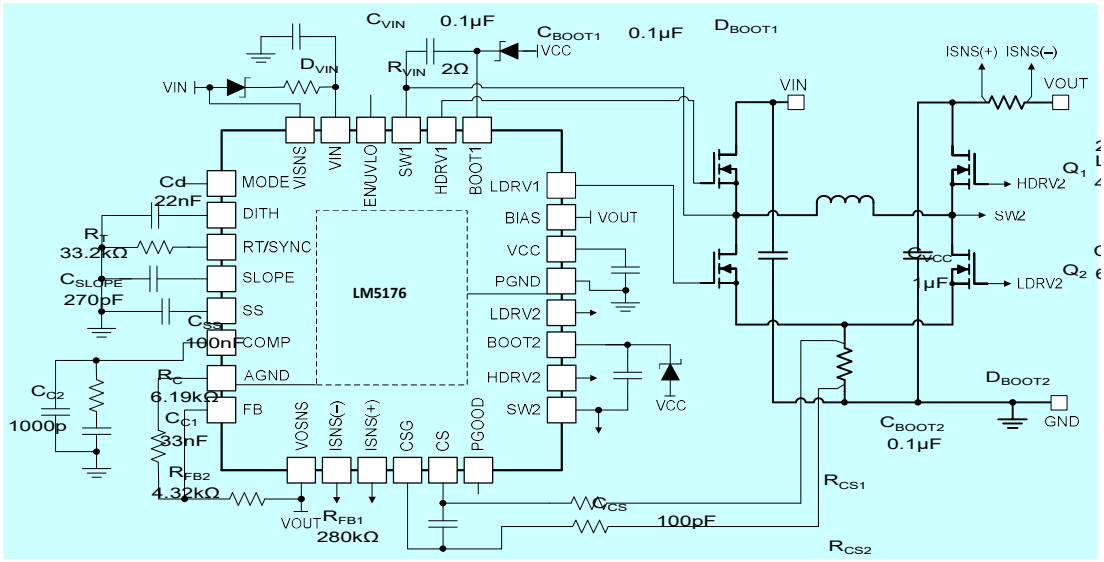
Input Voltage Ripple Spec	**180**	**mV_{pk-pk}**
Minimum Input Capacitance	10.0	µF
Input Capacitance, C_{IN}	**33**	**µF**
Maximum Permitted ESR	57.5	mΩ
Input Capacitor ESR	**2**	**mΩ**
Resulting Input Voltage Ripple (max)	16	mV_{pk-pk}
Input Capacitor RMS Current (max)	0.4	A (rms)

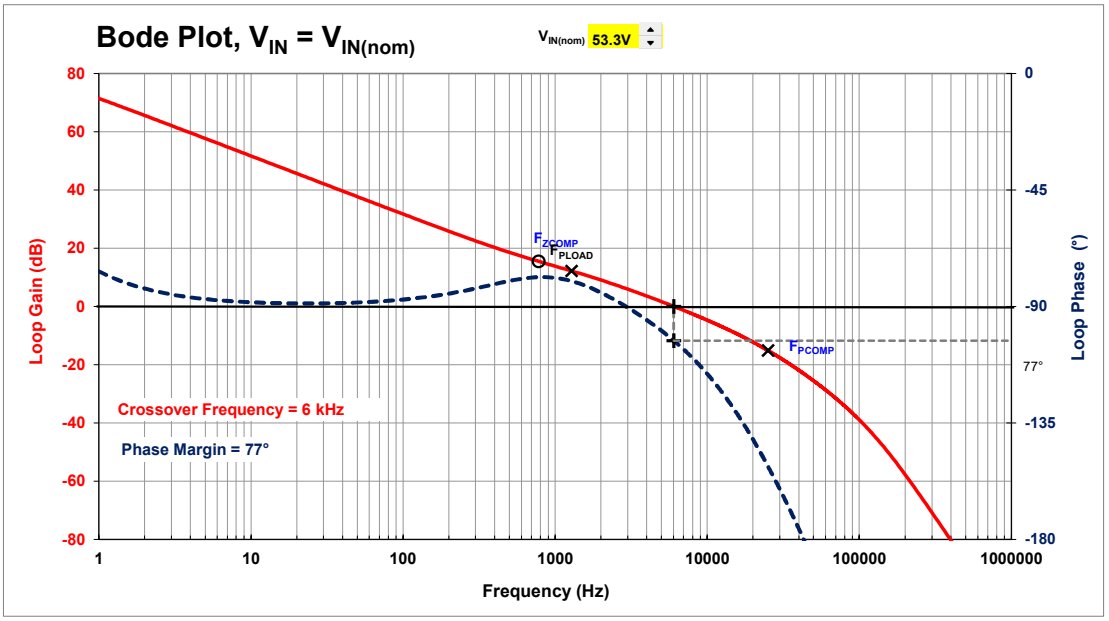
Step 6: Soft-start, Dither, UVLO

Soft-Start Time, t_{SS}	**15**	**ms**
Soft-Start Capacitance, C_{SS}	100	nF
DITHER Enabled **Modulating Frequency**	**2**	**kHz**
DITH Capacitance, Cd	22	nF
Required Input Voltage UVLO On	**52.5**	**V**
Input Voltage UVLO Off	51.48	V
Upper UVLO Resistor, R_{UV1}	**249**	**kΩ**
Lower UVLO Resistor, R_{UV2}	5.9	kΩ

Step 7: Compensation Design

Load Pole Frequency	1280	Hz
C_{OUT} ESR Zero Frequency	1326	kHz
Boost RHP Zero Frequency	0	kHz
Desired Crossover Frequency	**4**	**kHz**
Error Amp Pole Frequency	0	Hz
Upper Feedback Resistor, R_{FB1}	**280**	**kΩ**
Lower Feedback Resistor, R_{FB2}	4.32	kΩ





Compensation Components

	Calculated / Std Values		Selected		Actual P/Z Frequencies
R_C	3.9	3.92	**6.19**	**kΩ**	0 Hz (F_{PEA})
C_{C1}	21.2	22	**33**	**nF**	0.8 kHz (F_{ZCOMP})
C_{C2}	1430	1500	**1000**	**pF**	25 kHz (F_{PCOMP})

Min COMP Voltage	**1.55V**
Max COMP Voltage	**1.59V**