2.2nV/√Hz, Low-Power, 36V, Operational Amplifier

Check for Samples: OPA209, OPA2209, OPA4209

FEATURES

- **LOW VOLTAGE NOISE: 2.2nV/√Hz at 1kHz**
- **0.1Hz to 10Hz NOISE: 130nV$_{PP}$**
- **LOW QUIESCENT CURRENT: 2.5mA/Ch (max)**
- **LOW OFFSET VOLTAGE: 150µV (max)**
- **GAIN BANDWIDTH PRODUCT: 18MHz**
- **SLEW RATE: 6.4V/µs**
- **WIDE SUPPLY RANGE: ±2.25V to ±18V, +4.5V to +36V**
- **RAIL-TO-RAIL OUTPUT**
- **SHORT-CIRCUIT CURRENT: ±65mA**
- **AVAILABLE IN SOT23-5, MSOP-8, SO-8, AND TSSOP-14 PACKAGES**

APPLICATIONS

- **PLL LOOP FILTERS**
- **LOW-NOISE, LOW-POWER SIGNAL PROCESSING**
- **LOW-NOISE INSTRUMENTATION AMPLIFIERS**
- **HIGH-PERFORMANCE ADC DRIVERS**
- **HIGH-PERFORMANCE DAC OUTPUT AMPLIFIERS**
- **ACTIVE FILTERS**
- **ULTRASOUND AMPLIFIERS**
- **PROFESSIONAL AUDIO PREAMPLIFIERS**
- **LOW-NOISE FREQUENCY SYNTHESIZERS**
- **INFRARED DETECTOR AMPLIFIERS**
- **HYDROPHONE AMPLIFIERS**

DESCRIPTION

The OPA209 series of precision operational amplifiers achieve very low voltage noise density (2.2nV/√Hz) with a supply current of only 2.5mA (max). This series also offers rail-to-rail output swing, which helps to maximize dynamic range.

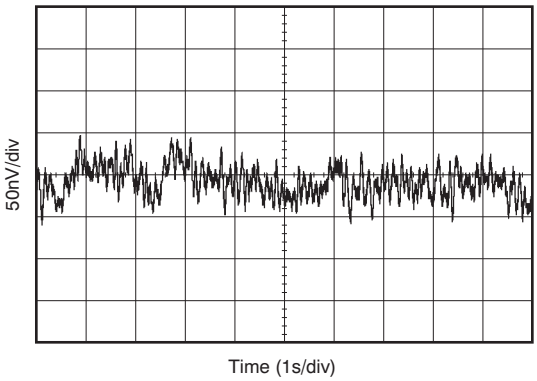
In precision data acquisition applications, the OPA209 provides fast settling time to 16-bit accuracy, even for 10V output swings. This excellent ac performance, combined with only 150µV (max) of offset and low drift over temperature, makes the OPA209 very suitable for fast, high-precision applications.

The OPA209 is specified over a wide dual power-supply range of ±2.25 to ±18V, or single-supply operation from +4.5V to +36V.

The OPA209 is available in the SOT23-5, MSOP-8 and the standard SO-8 packages. The dual OPA2209 comes in both MSOP-8 and SO-8 packages. The quad OPA4209 is available in the TSSOP-14 package.

The OPA209 series is specified from –40°C to +125°C.

0.1Hz to 10Hz NOISE



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA209	SOT23-5	DBV	OOBQ
	MSOP-8	DGK	OOAQ
	SO-8	D	OPA209A
OPA2209	MSOP-8	DGK	OOJI
	SO-8	D	O2209
OPA4209	TSSOP-14	PW	OPA4209

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		OPA209, OPA2209, OPA4209	UNIT
Supply Voltage	V_S = (V+) – (V–)	40	V
Signal Input Terminal, Voltage(2)		(V–) – 0.5 to (V+) + 0.5	V
Signal Input Terminal, Current (except power-supply pins)(2)		10	mA
Output Short-Circuit(3)		Continuous	
Operating Temperature	T_A	–55 to +150	°C
Storage Temperature	T_A	–65 to +150	°C
Junction Temperature	T_J	+200	°C
ESD Ratings:	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) For input voltages beyond the power-supply rails, voltage or current must be limited.
(3) Short-circuit to ground, one amplifier per package.

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ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA209, OPA2209, OPA4209 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±15, V_{CM} = 0V		±35	±150	µV
Drift	**dV_{OS}/dT**			**1**	**3**	**µV/°C**
vs Power Supply	PSRR	V_S = ±2.25V to ±18V		0.05	0.5	µV/V
over Temperature		**V_S = ±2.25V to ±18V**			**1**	**µV/V**
Channel Separation, dc (dual and quad versions)				1		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = 0V		±1	±4.5	nA
over Temperature, -40°C to +85°C		V_{CM} = 0V			±8	nA
over Temperature, -40°C to +125°C		**V_{CM} = 0V**			**±15**	**nA**
Input Offset Current	I_{OS}	V_{CM} = 0V		±0.7	±4.5	nA
over Temperature, -40°C to +85°C		V_{CM} = 0V			±8	nA
over Temperature, -40°C to +125°C		**V_{CM} = 0V**			**±15**	**nA**
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz	e_n			0.13		$µV_{PP}$
Noise Density, f = 10Hz				3.3		$nV/\sqrt{Hz}$
Noise Density, f = 100Hz				2.25		$nV/\sqrt{Hz}$
Noise Density, f = 1kHz				2.2		$nV/\sqrt{Hz}$
Input Current Noise Density, f = 1kHz	I_n			500		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) + 1.5V		(V+) – 1.5V	V
Common-Mode Rejection Ratio, over Temperature	**CMRR**	**(V–) + 1.5V < V_{CM} < (V+) – 1.5V**	**120**	**130**		**dB**
INPUT IMPEDANCE						
Differential				200 || 4		kΩ || pF
Common-Mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–) + 0.2V < V_O < (V+) – 0.2V, R_L = 10kΩ	126	132		dB
over Temperature		**(V–) + 0.2V < V_O < (V+) – 0.2V, R_L = 10kΩ**	**120**			**dB**
		(V–) + 0.6V < V_O < (V+) – 0.6V, R_L = 600Ω(1)	114	120		dB
over Temperature		**(V–) + 0.6V < V_O < (V+) – 0.6V, R_L = 1kΩ**	**110**			**dB**
FREQUENCY RESPONSE						
Gain Bandwidth Product	GBW			18		MHz
Slew Rate	SR			6.4		V/µs
Phase margin	θm	R_L = 10kΩ, C_L = 25pF		80		Degrees
Settling Time, 0.1%	t_S	G = –1, 10V Step, C_L = 100pF		2.1		µs
Settling Time, 0.0015% (16-bit)		G = –1, 10V Step, C_L = 100pF		2.6		µs
Overload Recovery Time		G = –1		< 1		µs
Total Harmonic Distortion + Noise	THD+N	G = +1, f = 1kHz, V_O = $20V_{PP}$, 600Ω		0.000025		%

(1) See the Thermal Information table for additional information.

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ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA209, OPA2209, OPA4209			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage Output Swing		R_L = 10kΩ, A_{OL} > 130dB	(V–) + 0.2V		(V+) – 0.2V	V
		R_L = 600Ω, A_{OL} > 114dB	(V–) + 0.6V		(V+) – 0.6V	V
over Temperature		**R_L = 10kΩ, A_{OL} > 120dB**	**(V–) + 0.2V**		**(V+) – 0.2V**	**V**
Short-Circuit Current	I_{SC}	V_S = ±18V		±65		mA
Capacitive Load Drive (stable operation)	C_{LOAD}		See Typical Characteristics			
Open-Loop Output Impedance	Z_O		See Typical Characteristics			
POWER SUPPLY						
Specified Voltage	V_S		±2.25		±18	V
Quiescent Current (per amplifier)	I_Q	I_O = 0A		2.2	2.5	mA
over Temperature					**3.25**	**mA**
TEMPERATURE RANGE						
Specified Range	T_A		–40		+125	°C
Operating Range	T_A		–55		+150	°C

THERMAL INFORMATION

THERMAL METRIC(1)		OPA209AID	OPA209AIDBV	OPA209AIDGK	UNITS
		D	DBV	DGK	
		8	5	8	
θ_{JA}	Junction-to-ambient thermal resistance(2)	135.5	204.9	142.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	73.7	200	46.9	
θ_{JB}	Junction-to-board thermal resistance	61.9	113.1	63.5	
ψ_{JT}	Junction-to-top characterization parameter	19.7	38.2	5.3	
ψ_{JB}	Junction-to-board characterization parameter	54.8	104.9	62.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

THERMAL INFORMATION

THERMAL METRIC(1)		OPA2209AID	OPA2209AIDGK	OPA4209AIPW	UNITS
		D	DGK	PW	
		8	8	14	
θ_{JA}	Junction-to-ambient thermal resistance(2)	134.3	132.7	112.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	72.1	38.5	26.1	
θ_{JB}	Junction-to-board thermal resistance	60.7	52.1	61.0	
ψ_{JT}	Junction-to-top characterization parameter	18.2	2.4	0.7	
ψ_{JB}	Junction-to-board characterization parameter	53.8	52.8	59.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

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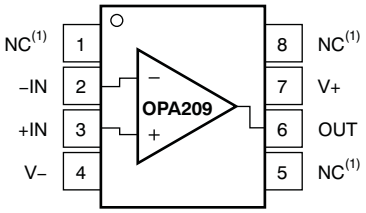
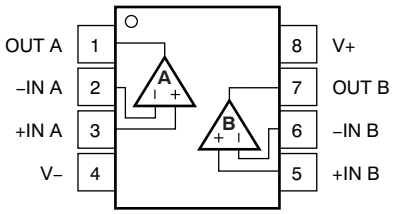
PIN CONFIGURATIONS

OPA209
MSOP-8, SO-8
(TOP VIEW)

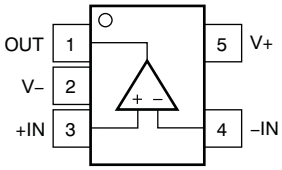


(1) NC = no internal connection

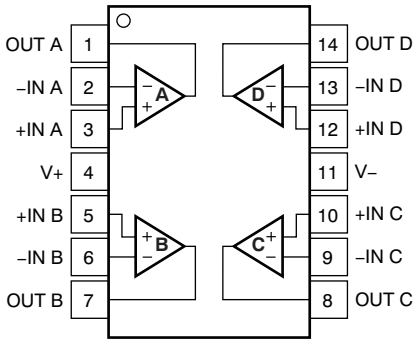
OPA2209
MSOP-8, SO-8
(TOP VIEW)



OPA209
SOT23-5
(TOP VIEW)



OPA4209
TSSOP-14
(TOP VIEW)



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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±18V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

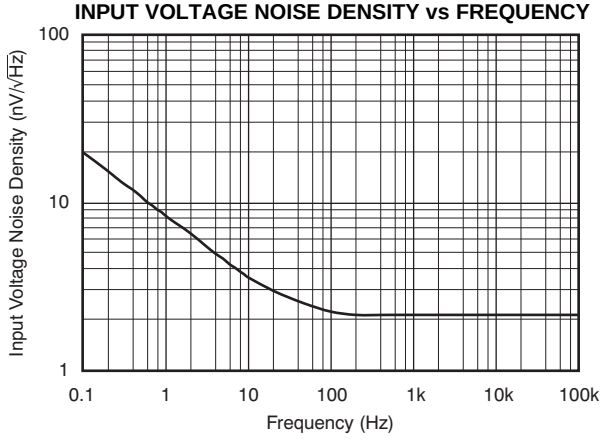

Figure 1.

INPUT CURRENT NOISE DENSITY vs FREQUENCY

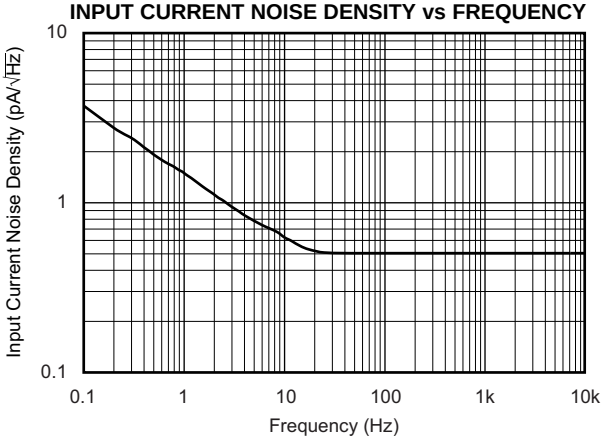

Figure 2.

TOTAL HARMONIC DISTORTION + NOISE RATIO vs FREQUENCY

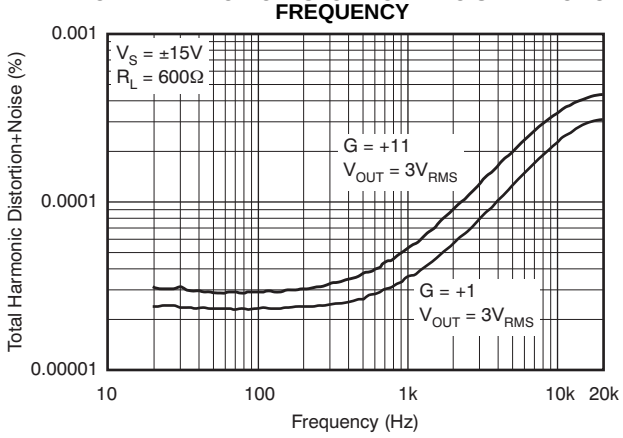

Figure 3.

TOTAL HARMONIC DISTORTION + NOISE RATIO vs AMPLITUDE

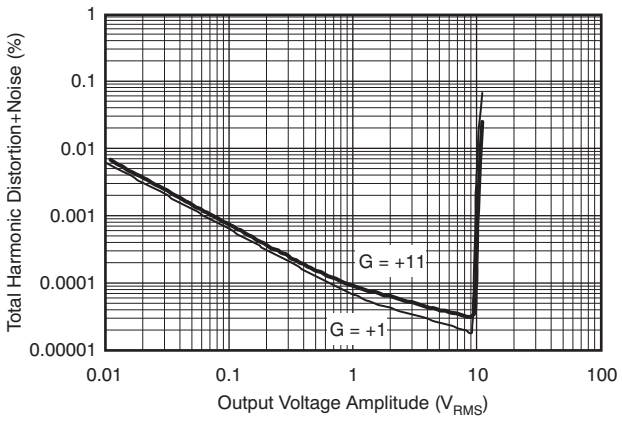

Figure 4.

0.1Hz TO 10Hz NOISE

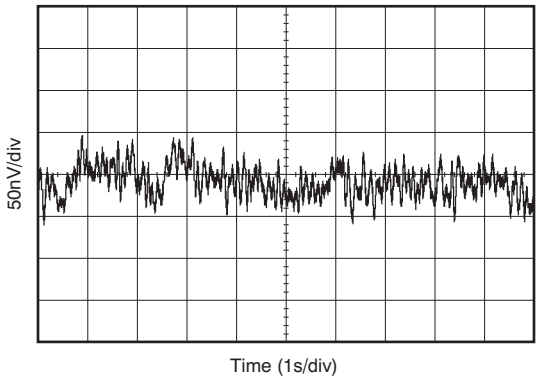

Figure 5.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (REFERRED TO INPUT)

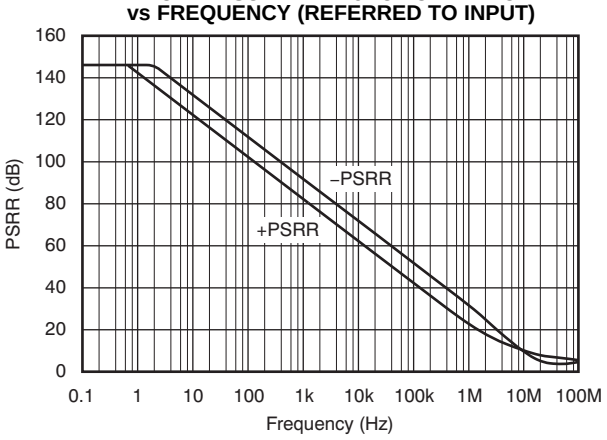

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

COMMON-MODE REJECTION RATIO vs FREQUENCY

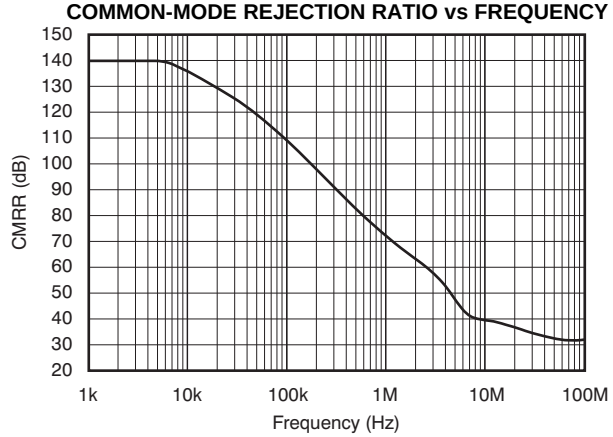

Figure 7.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

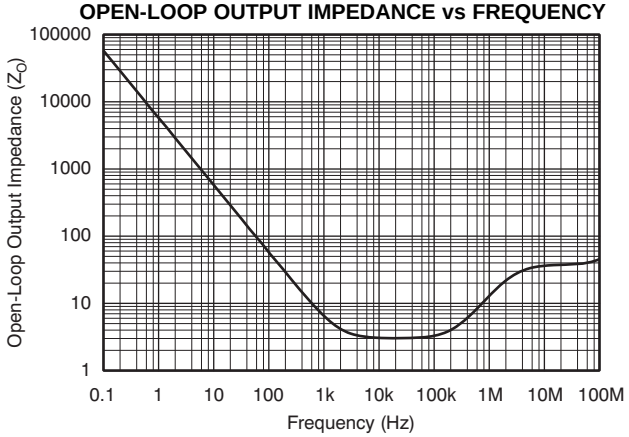

Figure 8.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

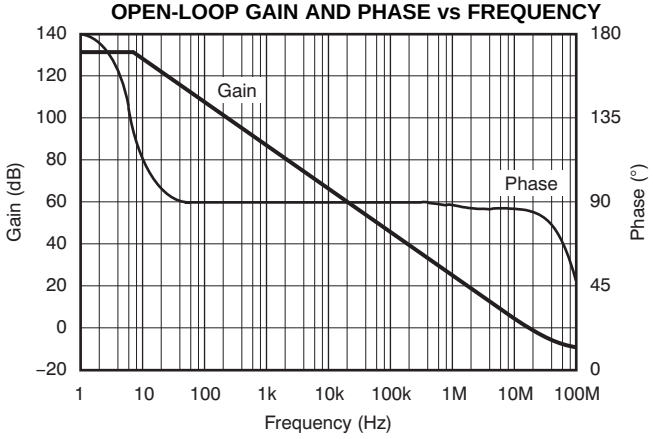

Figure 9.

OPEN-LOOP GAIN vs TEMPERATURE

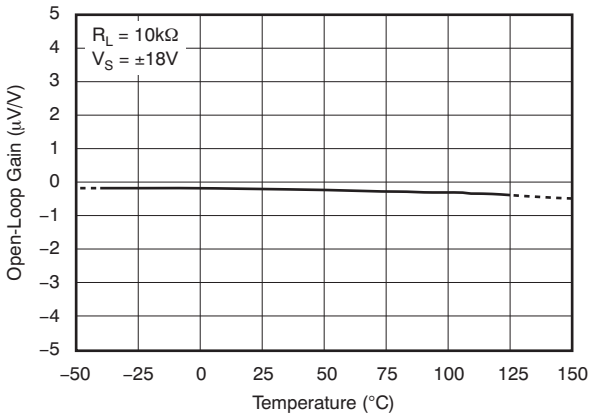

Figure 10.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

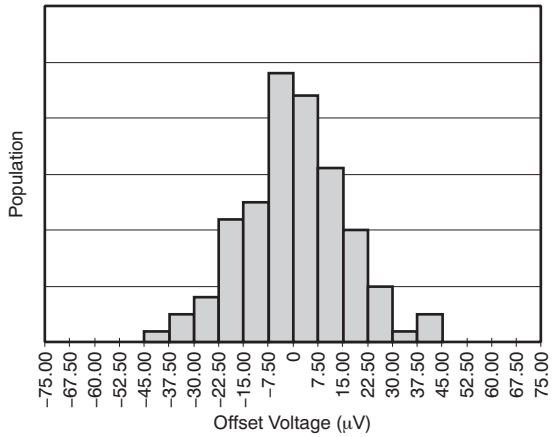

Figure 11.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

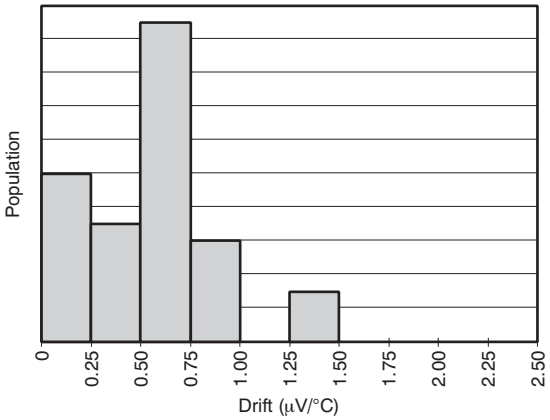

Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

INPUT BIAS AND INPUT OFFSET CURRENTS vs TEMPERATURE

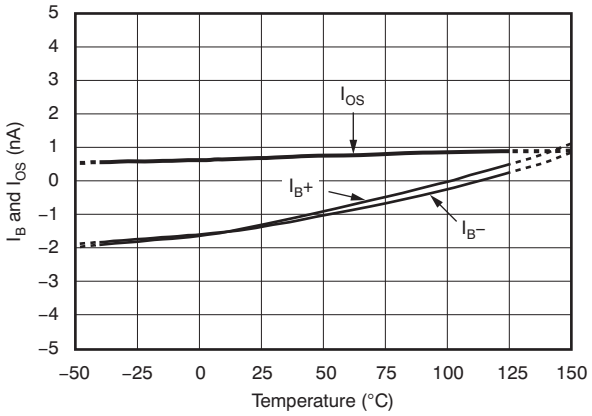

Figure 13.

INPUT OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

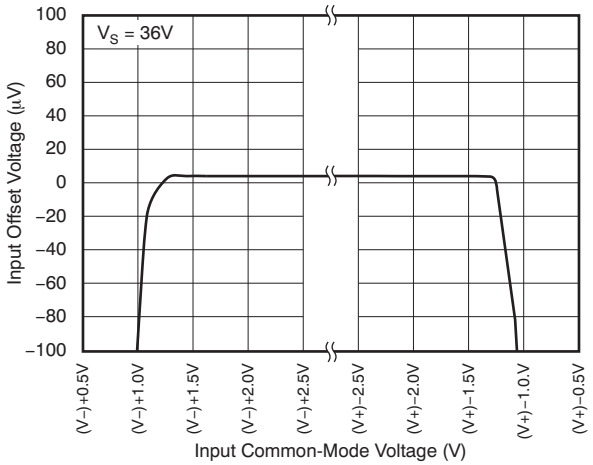

Figure 14.

INPUT OFFSET VOLTAGE vs TIME

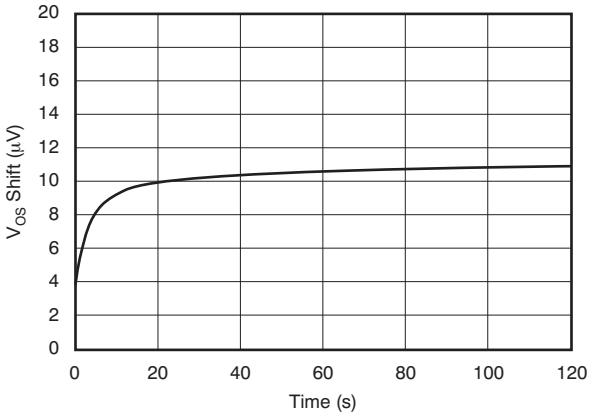

Figure 15.

INPUT OFFSET CURRENT vs SUPPLY VOLTAGE

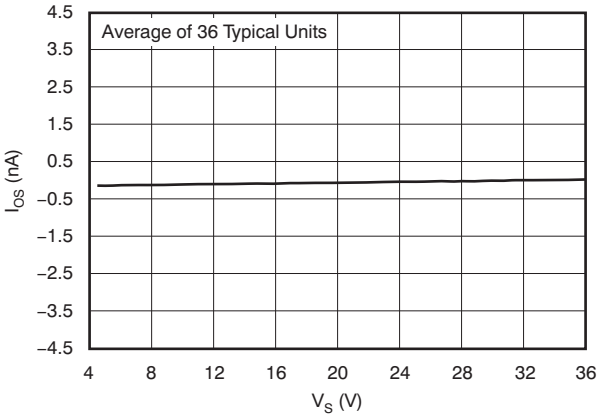

Figure 16.

INPUT BIAS AND INPUT OFFSET CURRENTS vs COMMON-MODE VOLTAGE

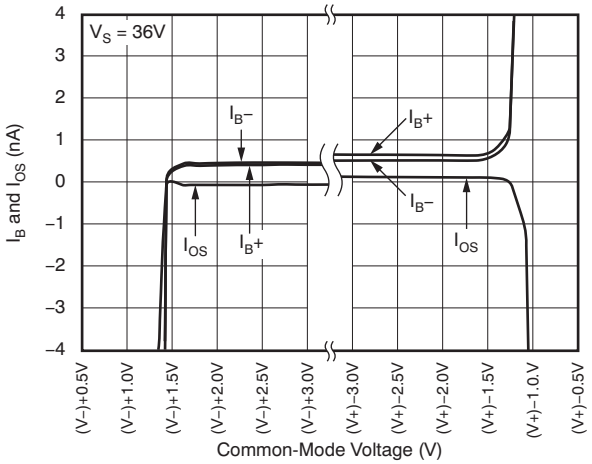

Figure 17.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

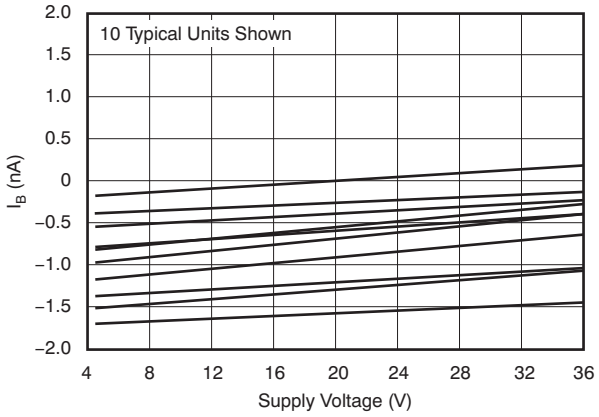

Figure 18.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

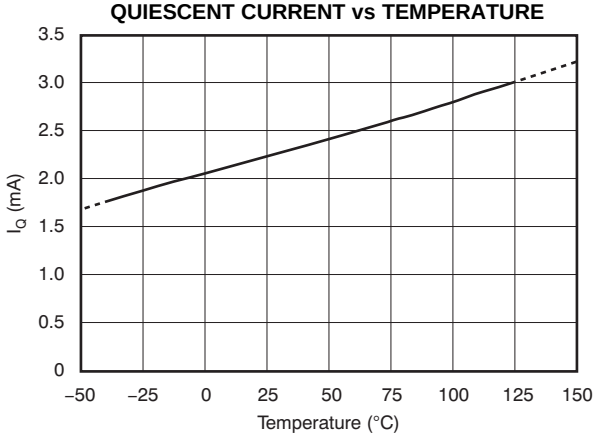

Figure 19.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

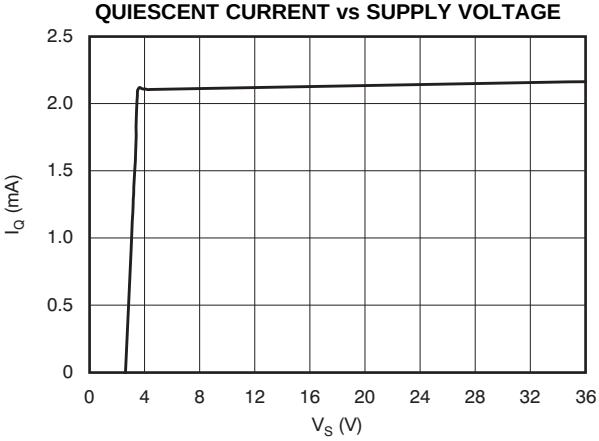

Figure 20.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

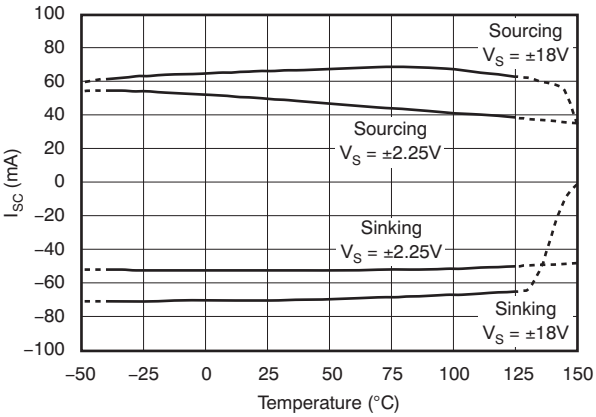

Figure 21.

OUTPUT VOLTAGE vs OUTPUT CURRENT

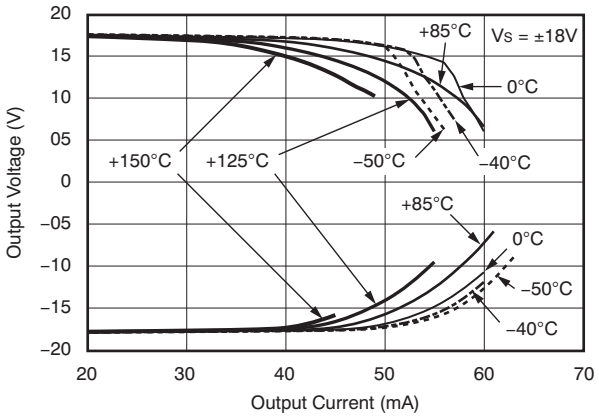

Figure 22.

SMALL-SIGNAL STEP RESPONSE

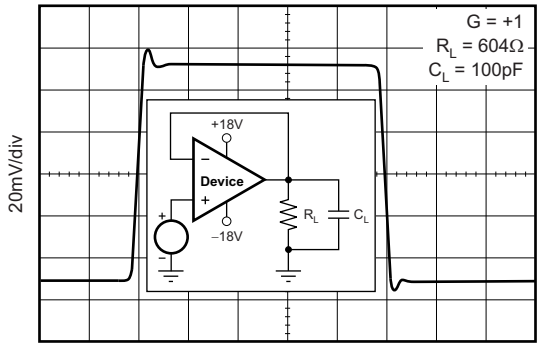

Figure 23.

SMALL-SIGNAL STEP RESPONSE

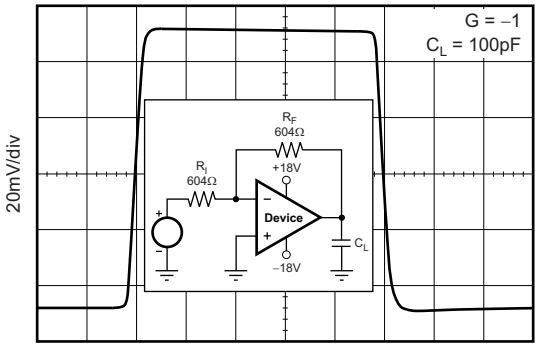

Figure 24.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

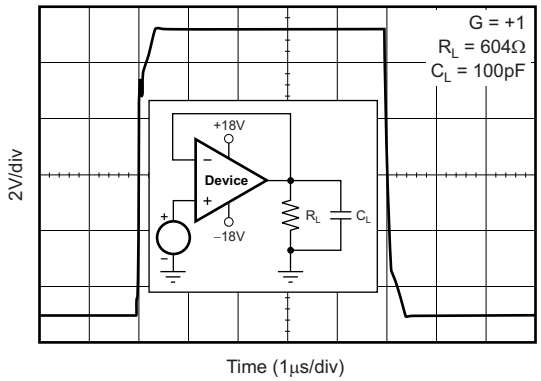

Figure 25.

LARGE-SIGNAL STEP RESPONSE

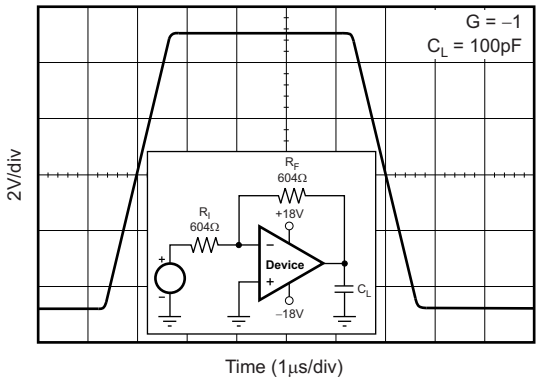

Figure 26.

NO PHASE REVERSAL

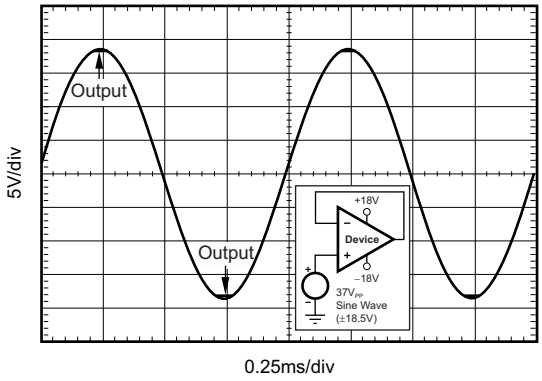

Figure 27.

NEGATIVE OVERLOAD RECOVERY

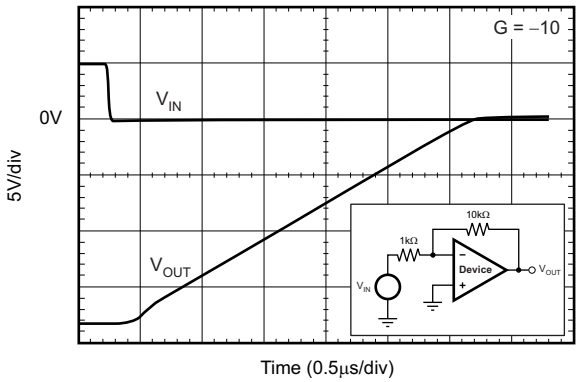

Figure 28.

POSITIVE OVERVOLTAGE RECOVERY

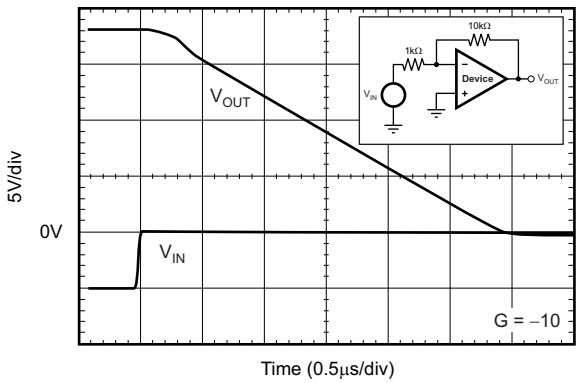

Figure 29.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

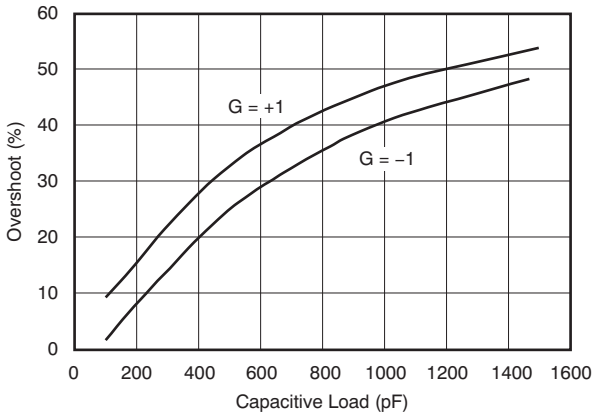

Figure 30.

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APPLICATION INFORMATION

DESCRIPTION

The OPA209 series of precision operational amplifiers are unity-gain stable, and free from unexpected output and phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1µF capacitors are adequate. Figure 31 shows a simplified schematic of the OPA209. This die uses a SiGe bipolar process and contains 180 transistors.

OPERATING VOLTAGE

The OPA209 series of op amps can be used with single or dual supplies within an operating range of V_S = +4.5V (±2.25V) up to +36V (±18V). Supply voltages higher than 40V total can permanently damage the device; see the Absolute Maximum Ratings table.

In addition, key parameters are assured over the specified temperature range, T_A = –40°C to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics section of this data sheet.

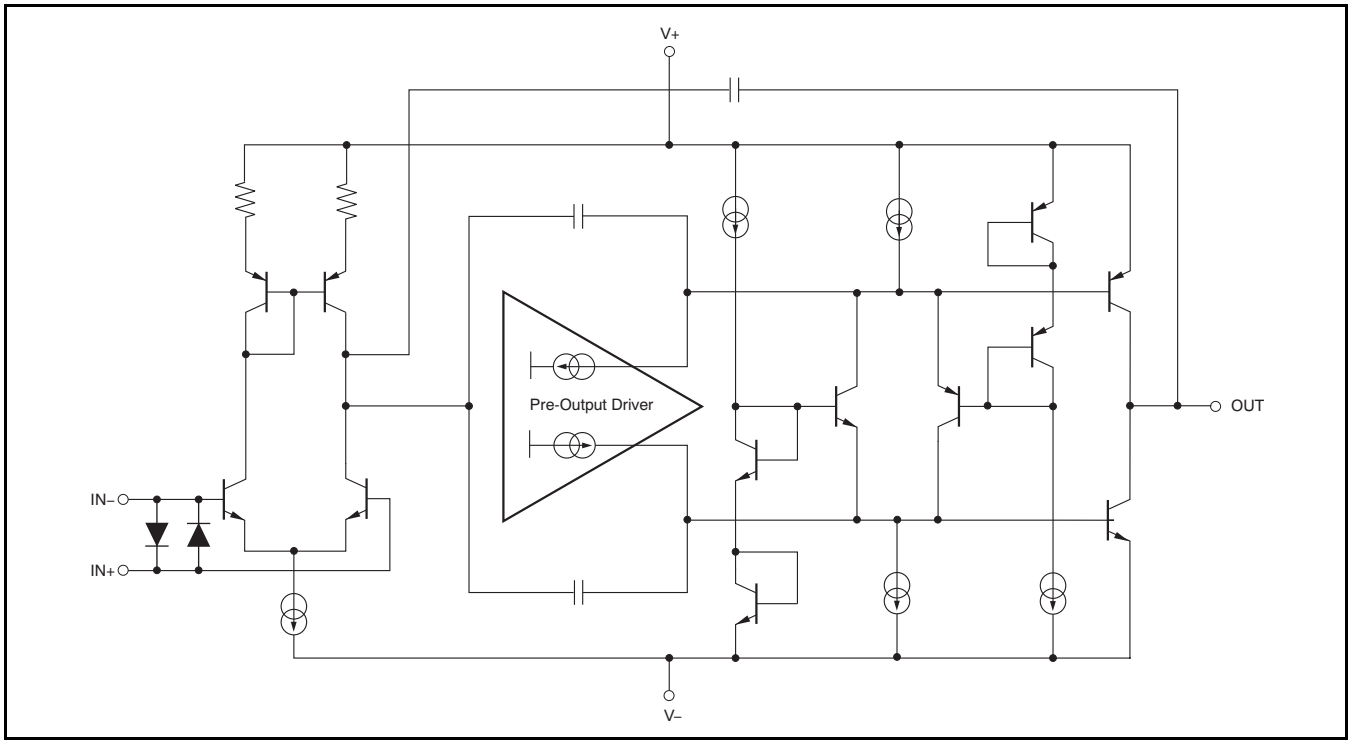

Figure 31. OPA209 Simplified Schematic

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INPUT PROTECTION

The input terminals of the OPA209 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 32. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 25 and Figure 26 of the Typical Characteristics. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA209. See the *Noise Performance* section for further information on noise performance. Figure 32 shows an example configuration that implements a current-limiting feedback resistor.

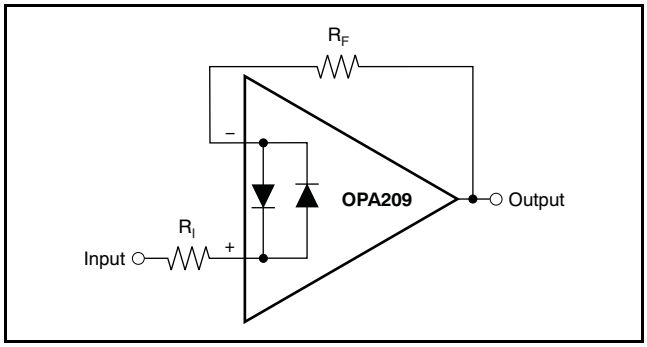

Figure 32. Pulsed Operation

NOISE PERFORMANCE

Figure 33 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with the total circuit noise calculated. The OPA209 has very low voltage noise, making it ideal for low source impedances (less than 2kΩ). As a comparable precision FET-input op amp (very low current noise), the OPA827 has somewhat higher voltage noise, but lower current noise. It provides excellent noise performance at moderate to high source impedance (10kΩ and up). For source impedance lower than 300Ω, the OPA211 may provide lower noise.

The equation in Figure 33 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise,
- i_n = current noise,
- R_S = source impedance,
- k = Boltzmann's constant = 1.38×10^{-23} J/K,
- and T = temperature in kelvins.

For more details on calculating noise, see the *Basic Noise Calculations* section.

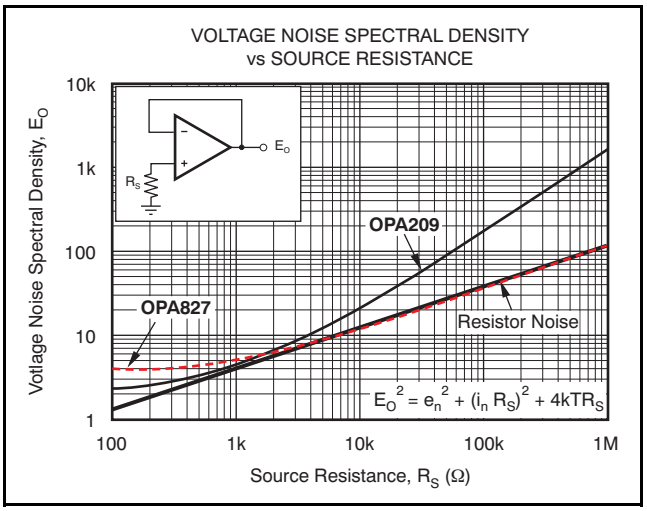

Figure 33. Noise Performance of the OPA209 and OPA827 in Unity-Gain Buffer Configuration

BASIC NOISE CALCULATIONS

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combinations of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is illustrated in Figure 33. The source impedance is usually fixed; consequently, select the appropriate op amp and the feedback resistors to minimize the respective contributions to the total noise.

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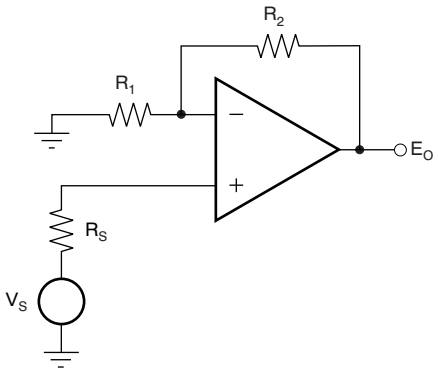
Figure 34 illustrates both noninverting (Figure 34a) and inverting (Figure 34b) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low-impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

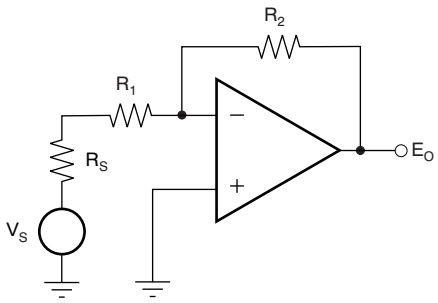
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

NOTE: For the OPA209 series op amps at 1kHz, $e_n = 2.2nV/\sqrt{Hz}$ and $I_n = 530fA/\sqrt{Hz}$.

Figure 34. Noise Calculation in Gain Configurations

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ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See Figure 35 for an illustration of the ESD circuits contained in the OPA209 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA209 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one Figure 35 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 35 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0V.

Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

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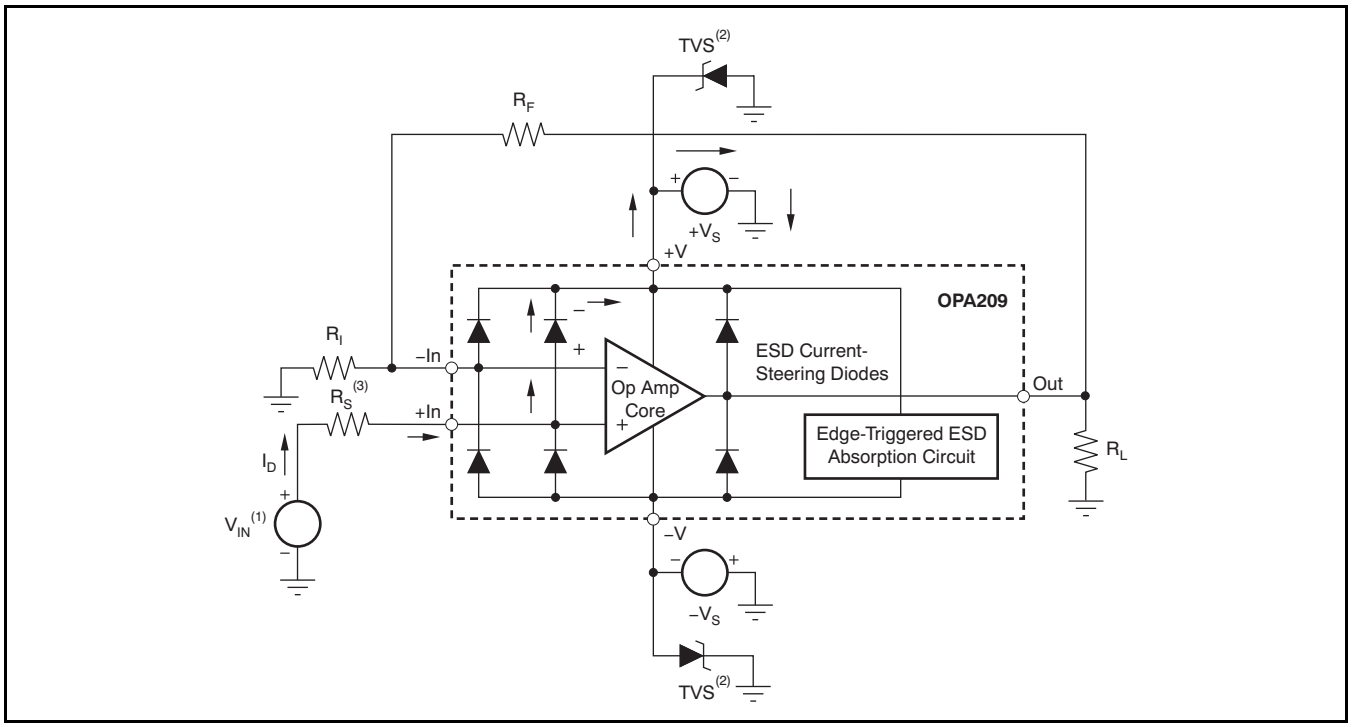
If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 35. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500mV$.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value approximately 1kΩ.

Figure 35. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2010) to Revision C	Page
• Deleted device graphic	1
• Changed y-axis units label in Figure 2	6

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA209AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 209A	Samples
OPA209AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOBQ	Samples
OPA209AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOBQ	Samples
OPA209AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OOAQ	Samples
OPA209AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OOAQ	Samples
OPA209AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 209A	Samples
OPA2209AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2209	Samples
OPA2209AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOJI	Samples
OPA2209AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOJI	Samples
OPA2209AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2209	Samples
OPA4209AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(OP4209A ~ OPA) 4209	Samples
OPA4209AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(OP4209A ~ OPA) 4209	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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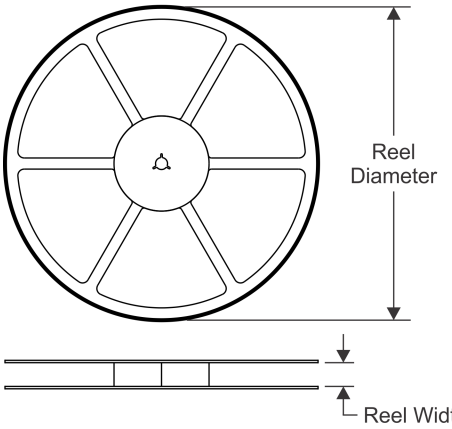
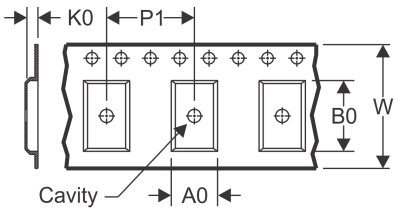
TAPE AND REEL INFORMATION

REEL DIMENSIONS

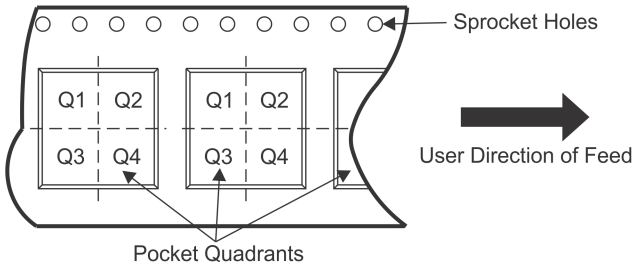


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

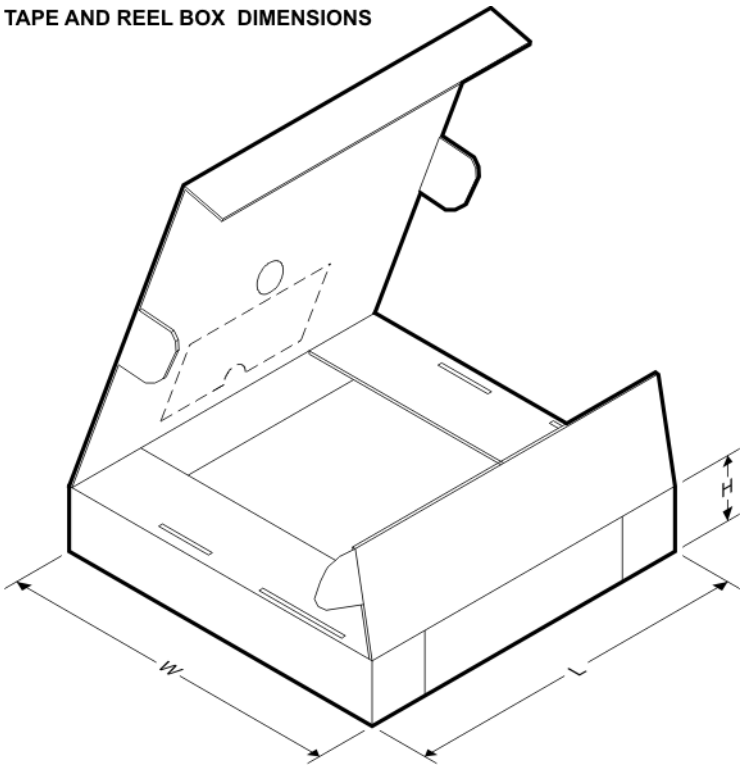
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA209AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA209AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA209AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA209AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA209AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2209AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2209AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2209AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4209AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

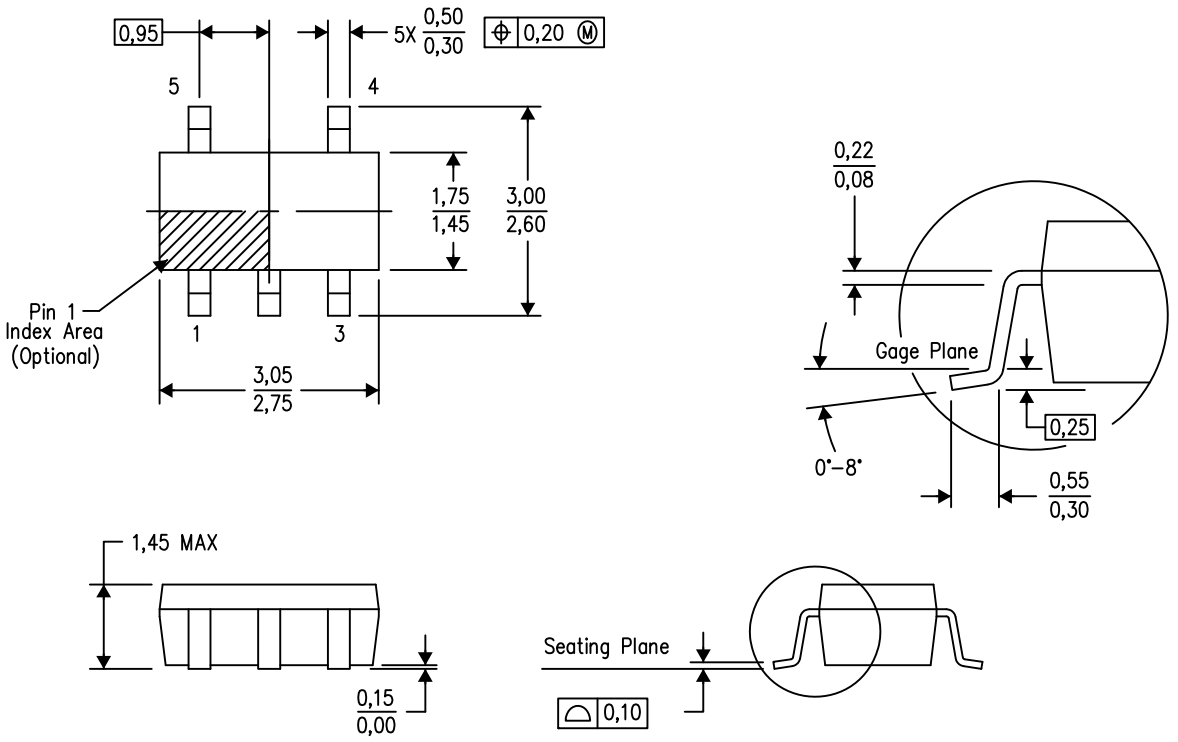
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA209AIDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA209AIDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA209AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA209AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA209AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2209AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2209AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2209AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA4209AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

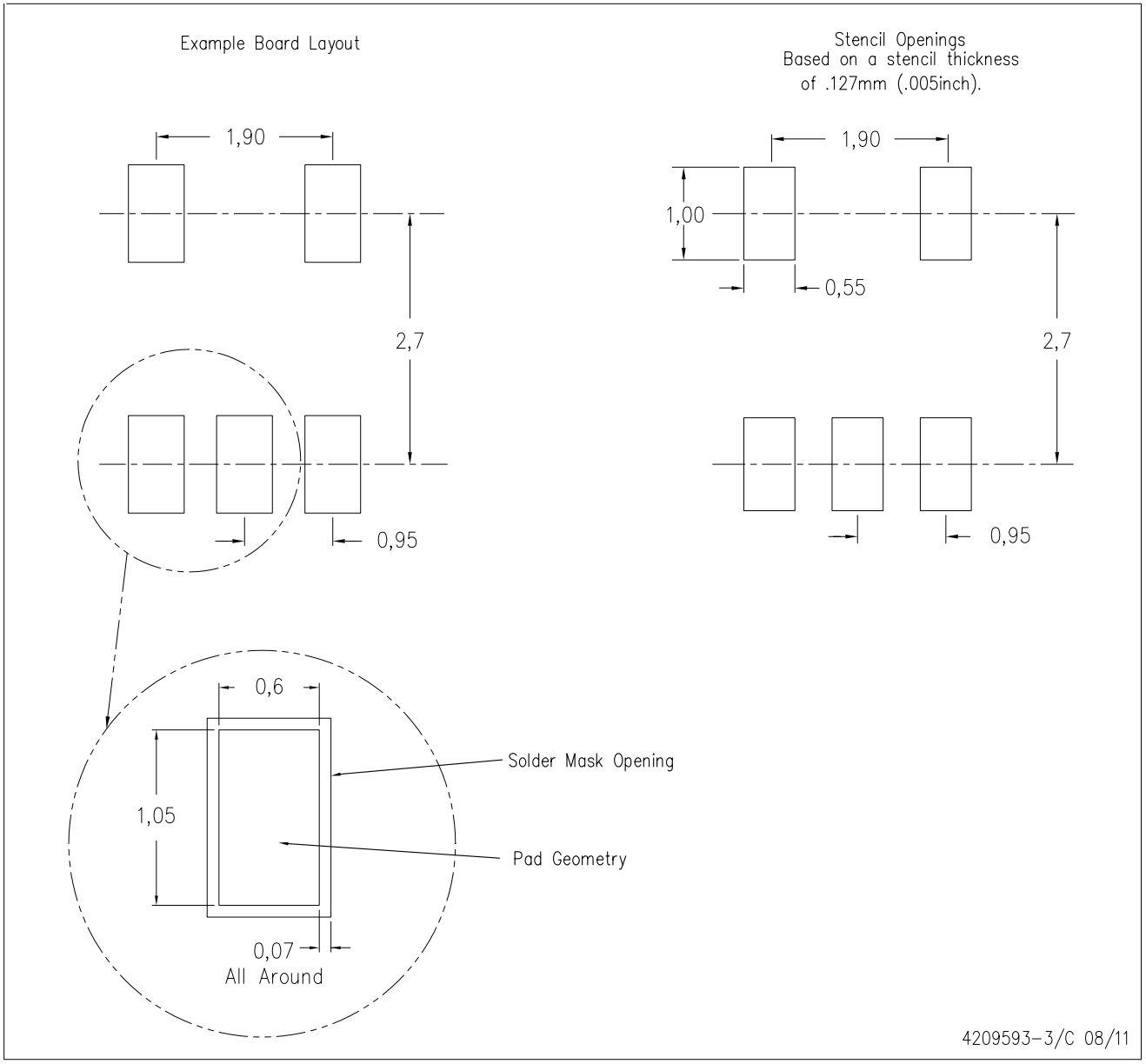
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

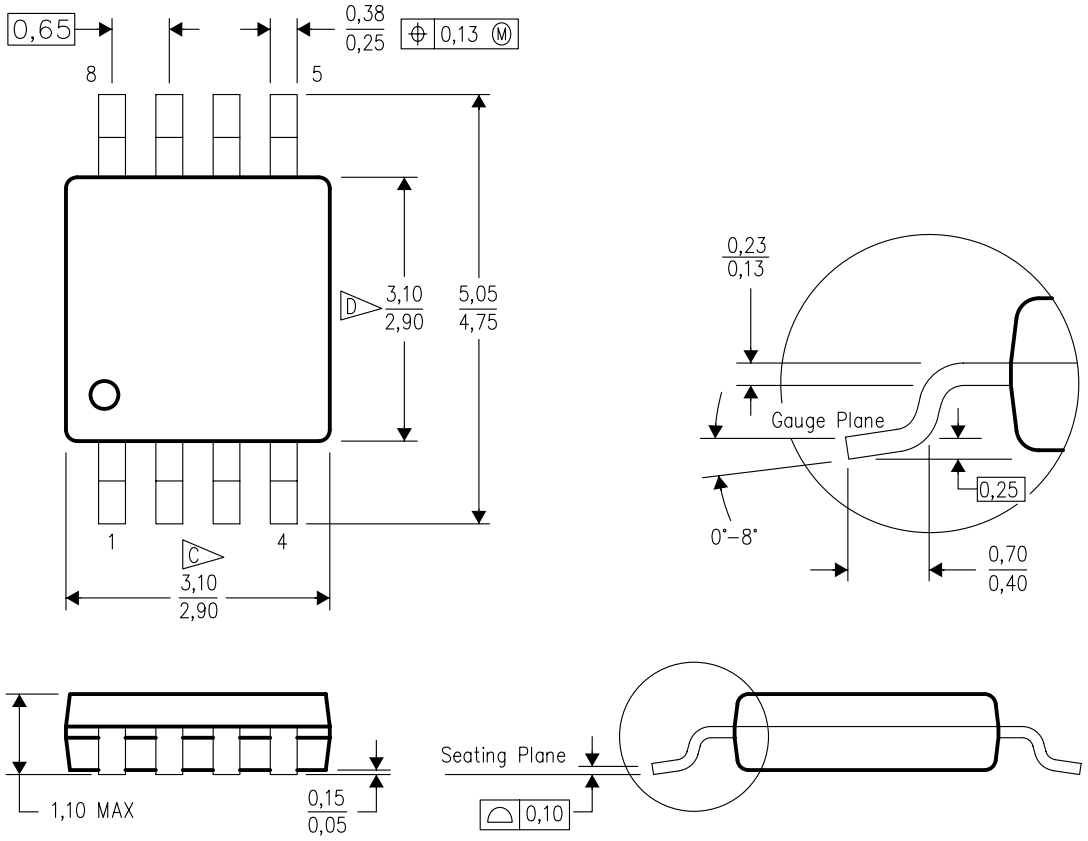
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

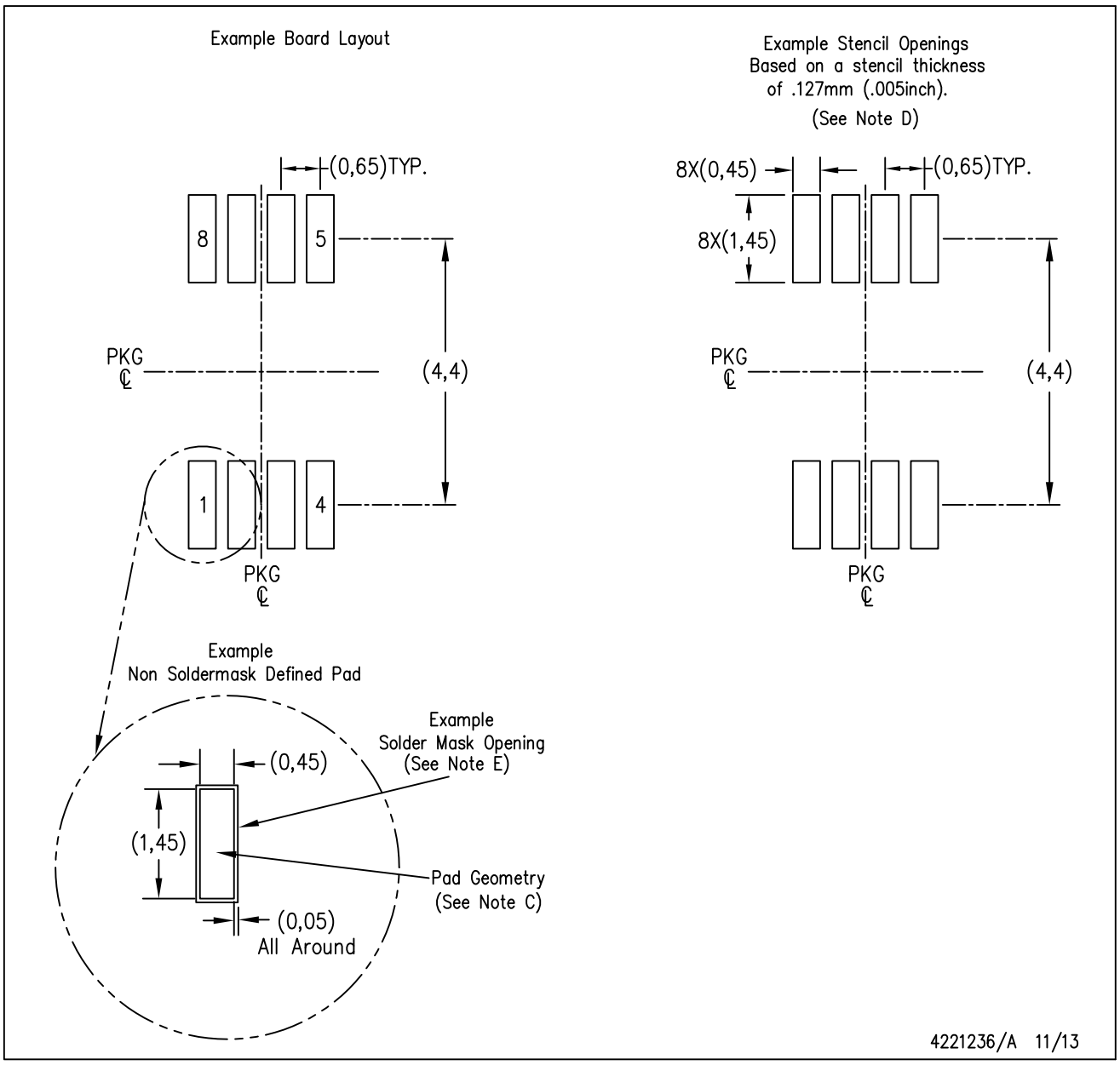
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

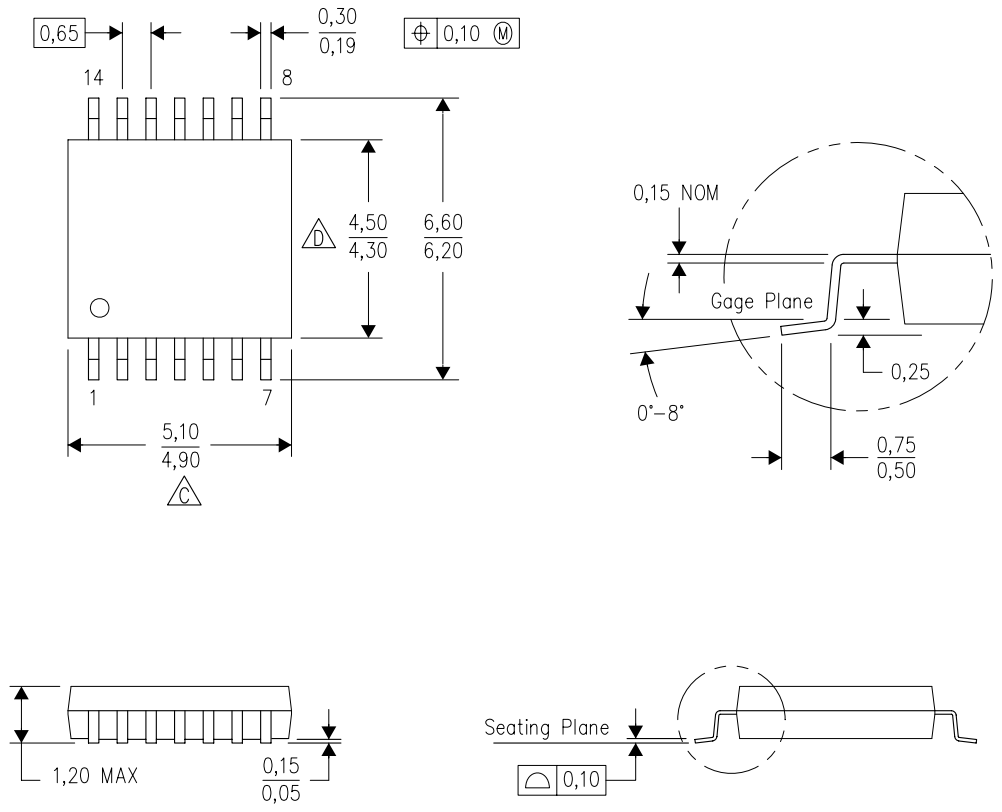
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

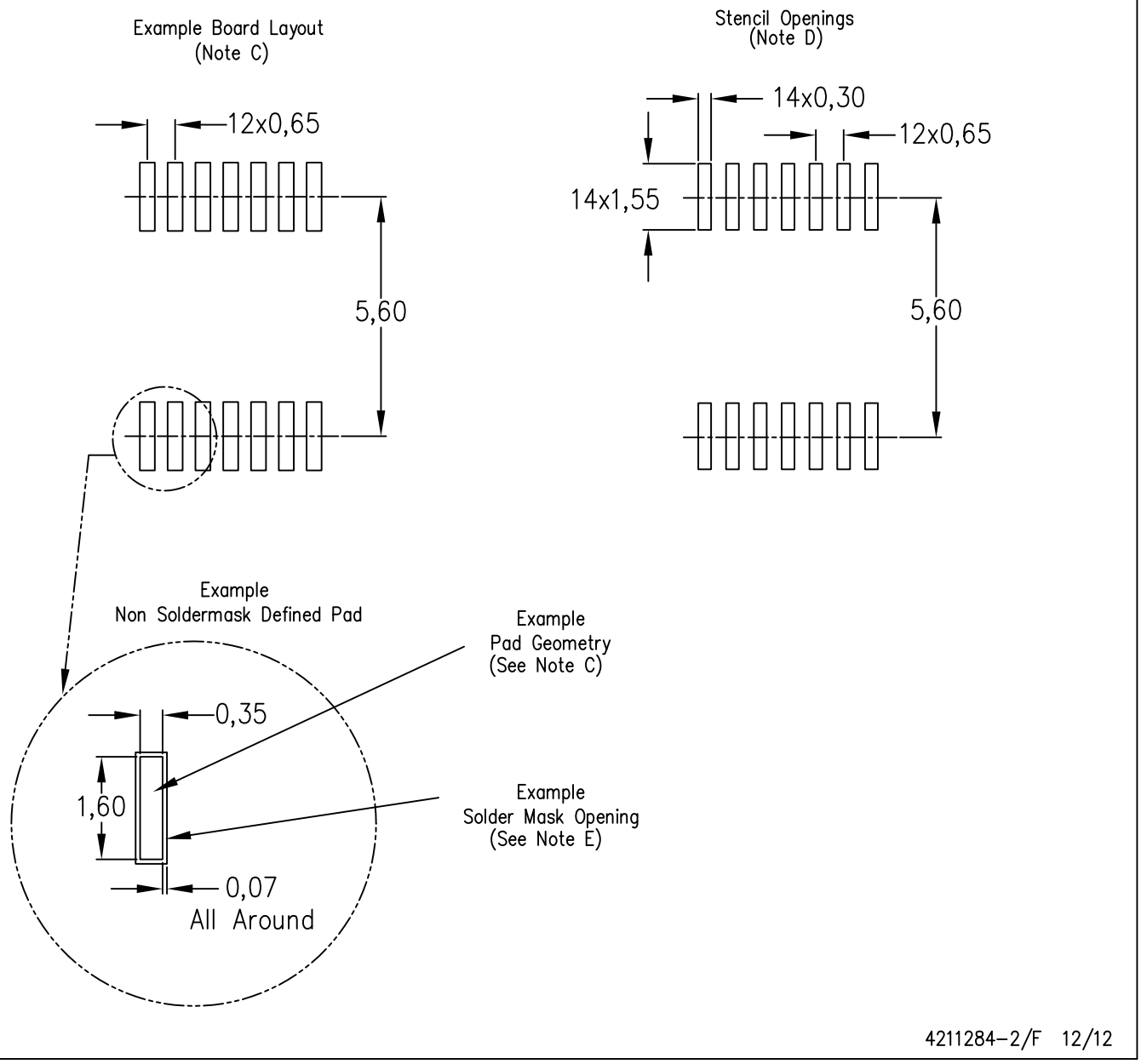
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

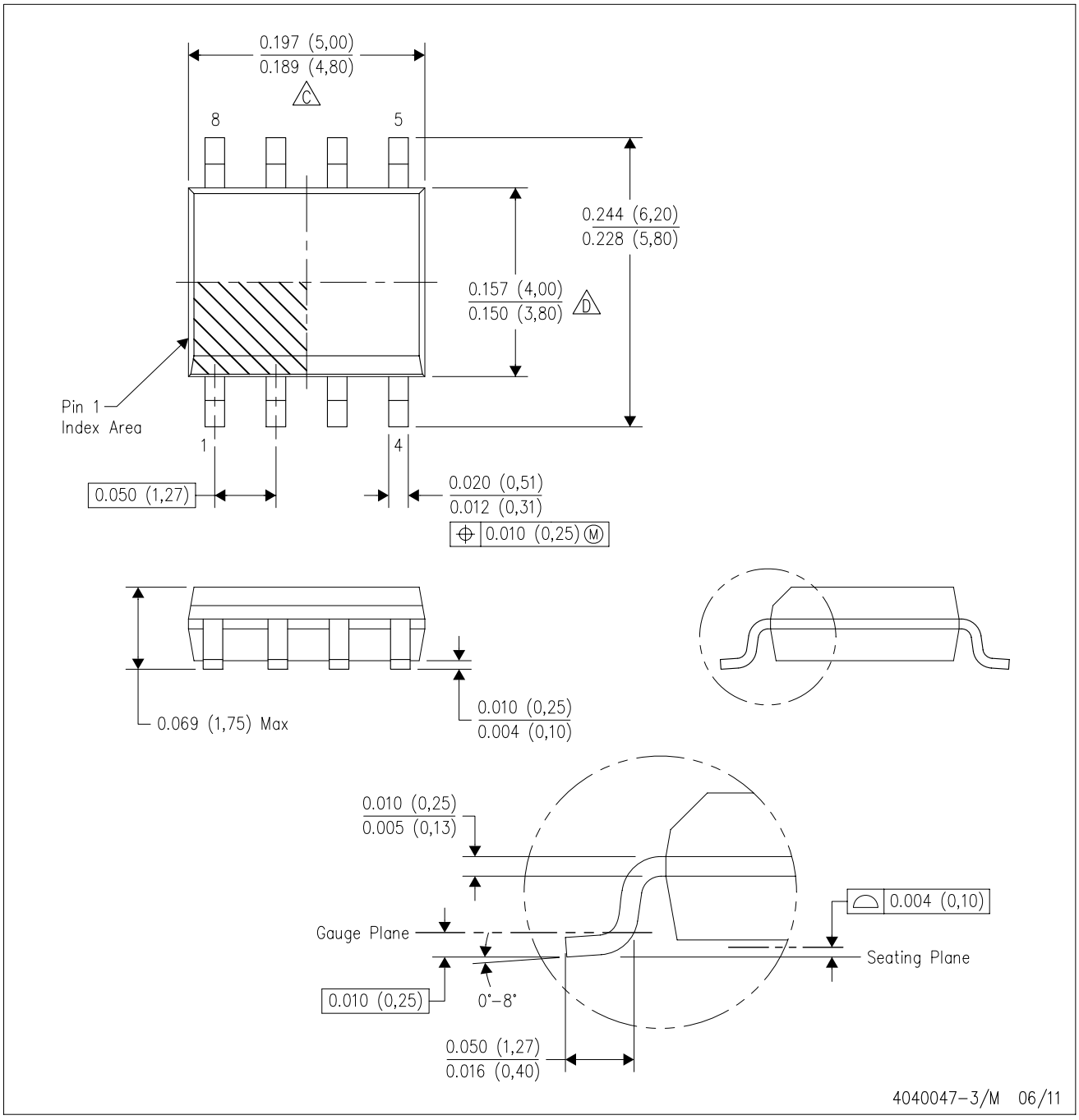
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



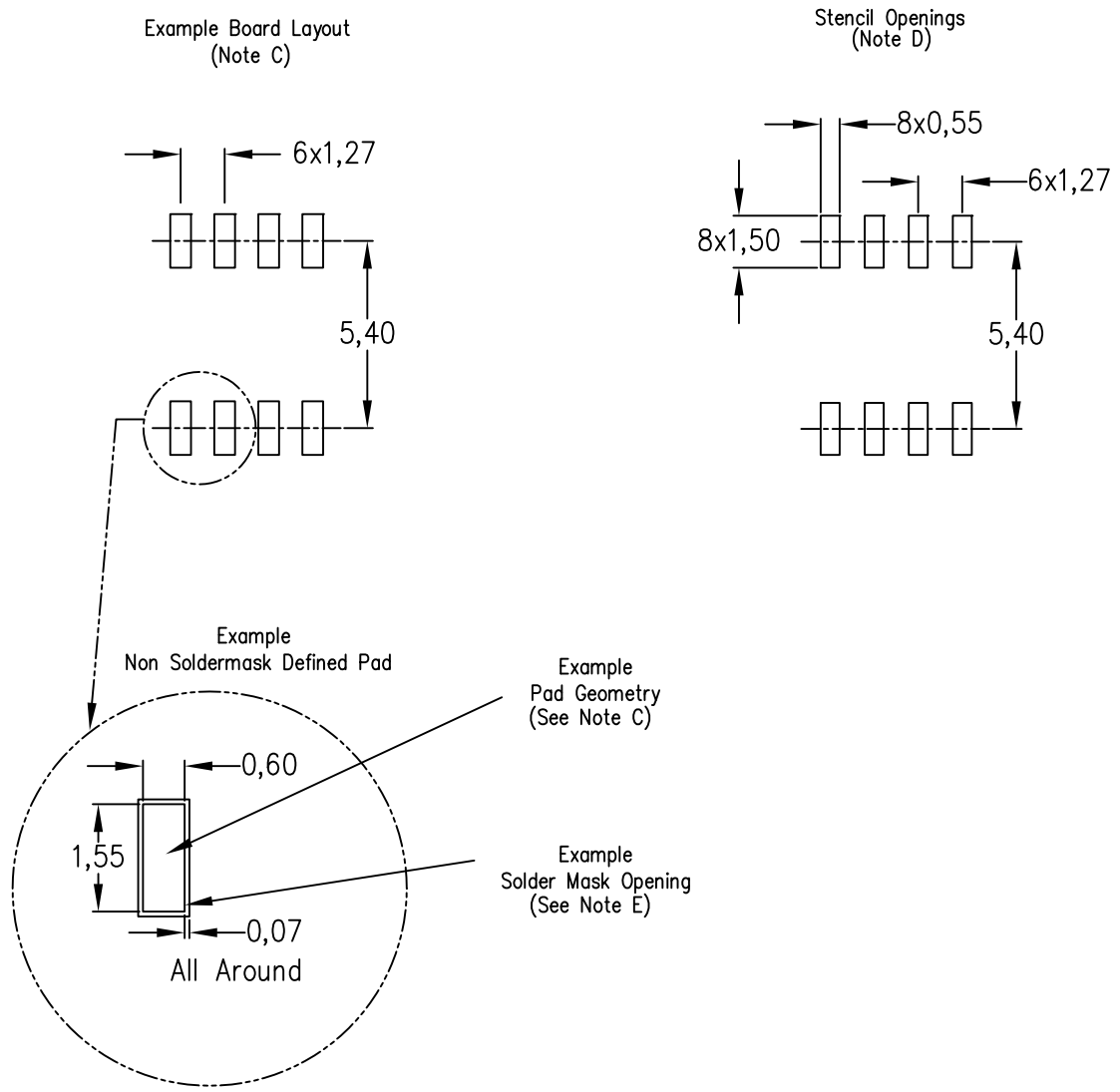
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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