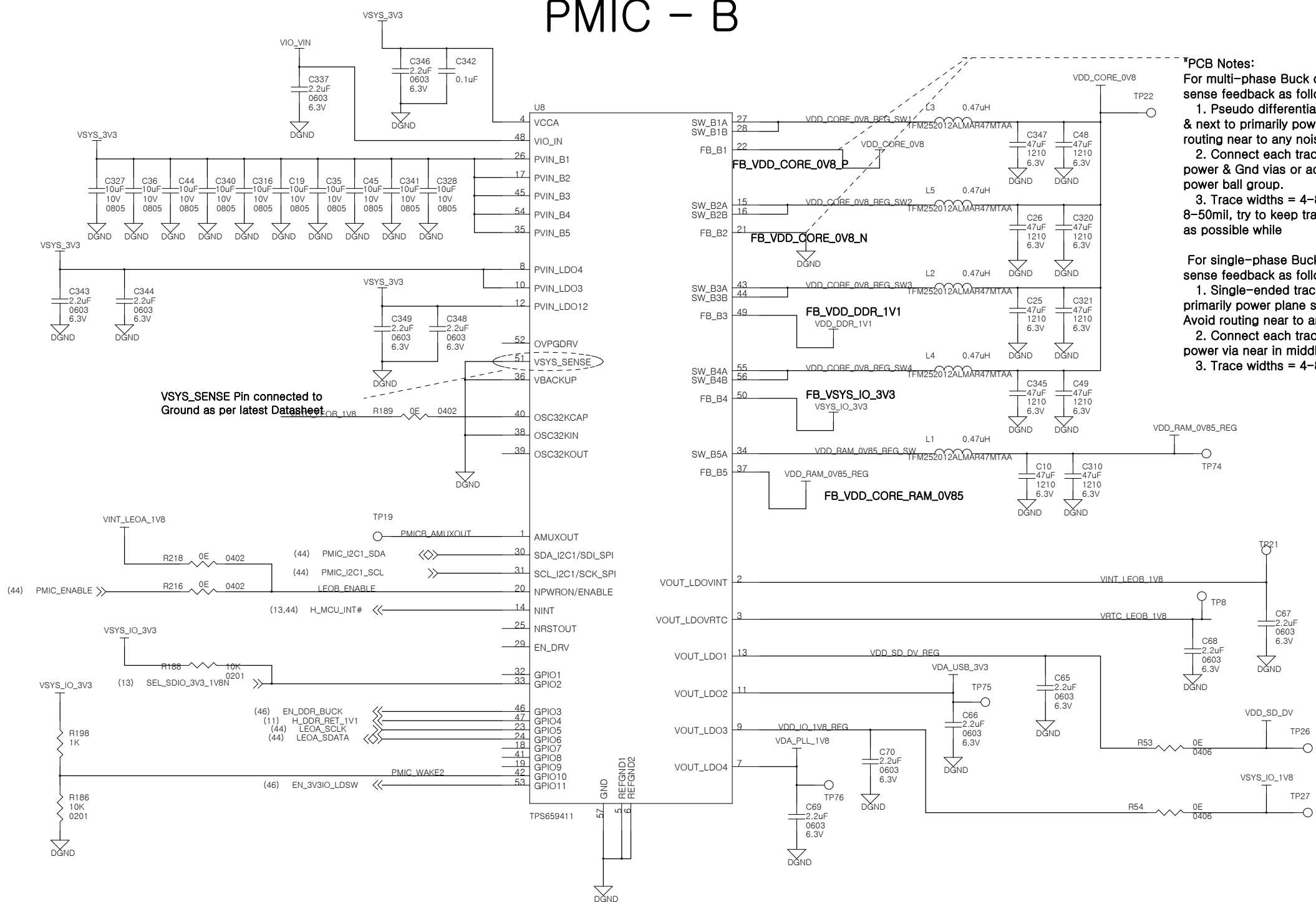


(3-Phase Buck supplying VDD_CPU)

Title PMIC A			
Size	<Core Design>		Rev
C			A
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PMIC – B

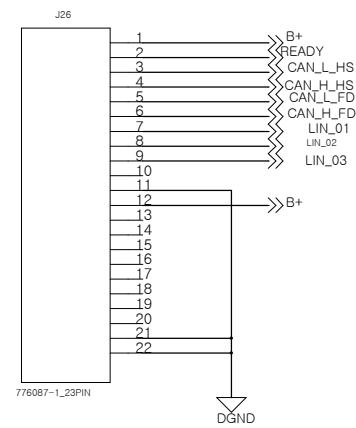


PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4–8mil & separation distance = 8–50mil, try to keep traces near each other as best as possible while

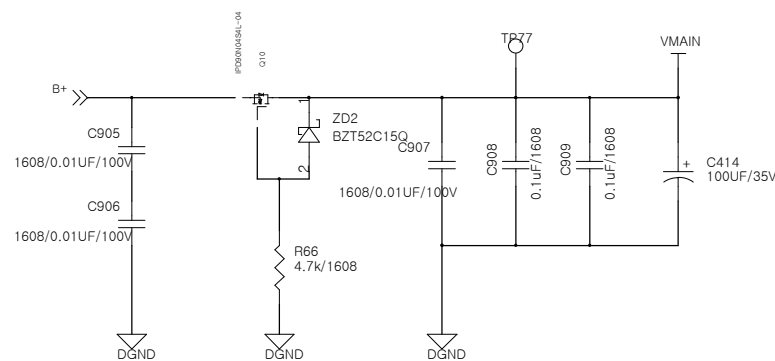
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4–8mil"

PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

MAIN CONNECTOR (Ext)

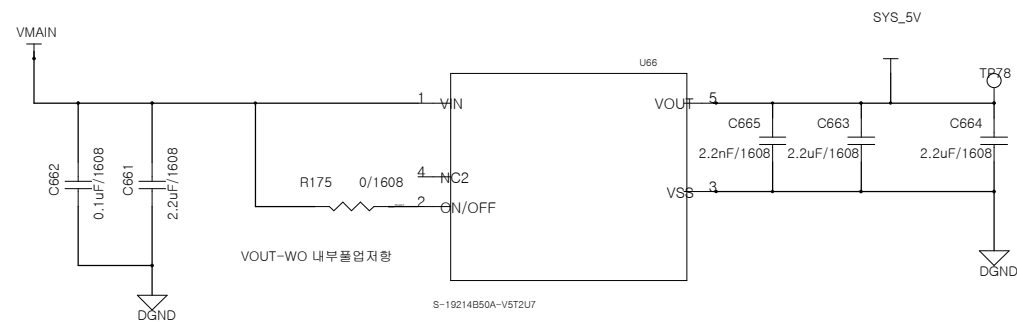


Protection Circuit

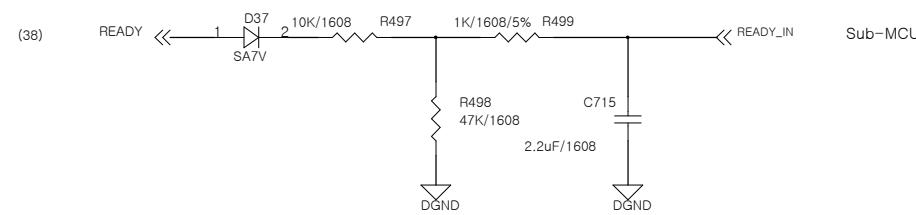


LDO (Main -> VDD_5V)

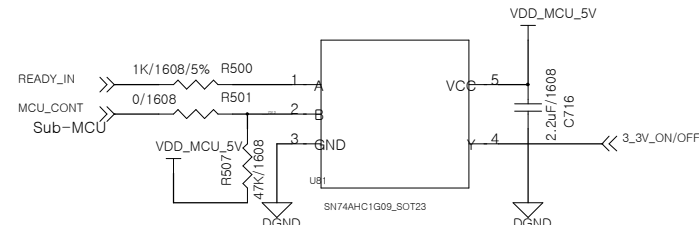
Operating Voltage (9V~16V)
12V -> 5V 1,000mA



Ready Signal



3.3V Regulator Control



3.3V Regulator Control Truth Table(And Gate)

Ready Low	Ready High	
0	0 Pull-Up	Sub-MCU Low
0	1	Sub-MCU Control High