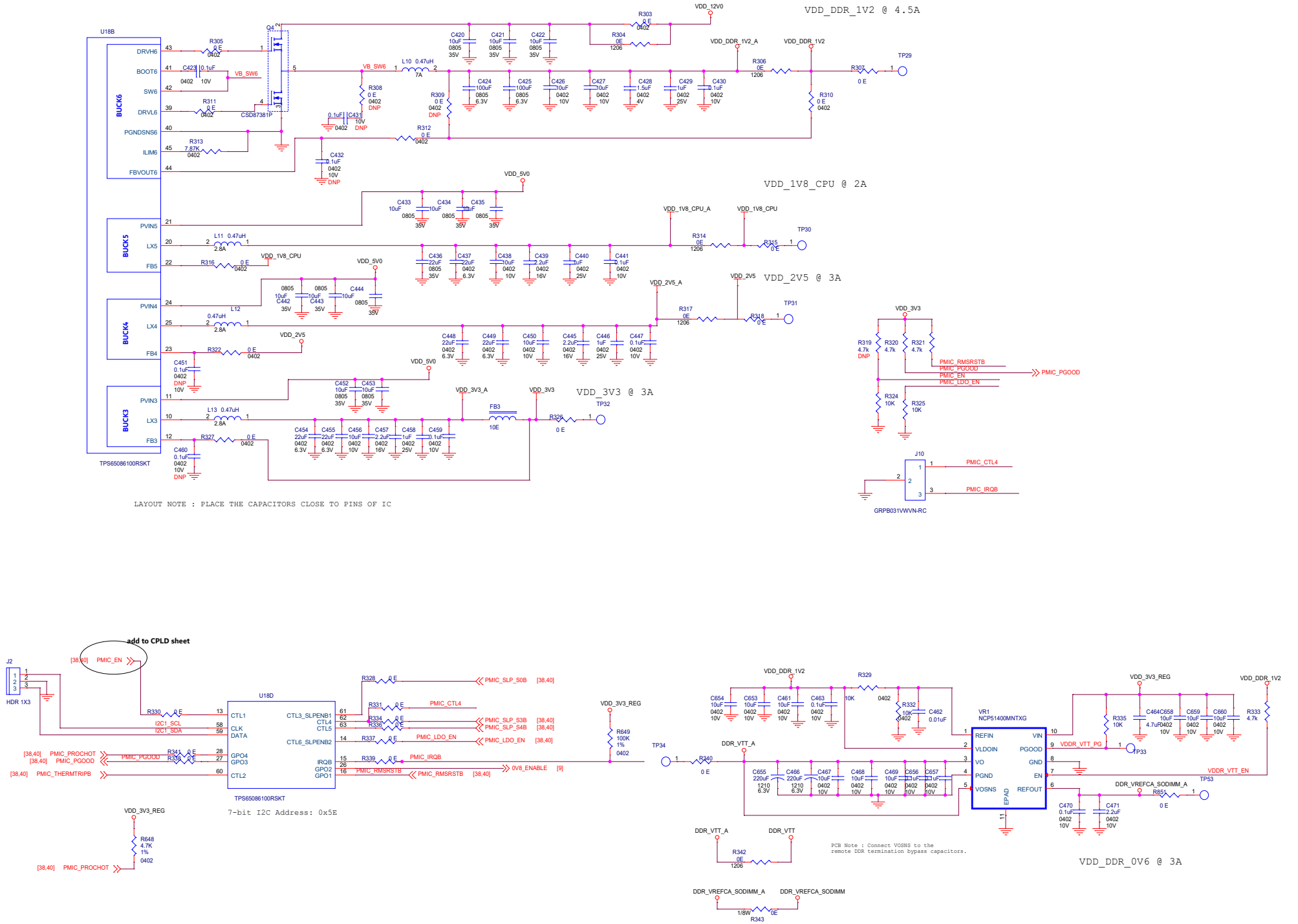
VDD_DDR_1V2 @ 4.5A
VDD_1V8_CPU @ 2A
VDD_2V5 @ 3A
VDD_3V3 @ 3A
VDD_DDR_0V6 @ 3A
U18B
TPS65086100RSKT
BUCK6
BUCK5
BUCK4
BUCK3
LAYOUT NOTE : PLACE THE CAPACITORS CLOSE TO PINS OF IC
J10
GRPB031VWVN-RC
PMIC_PGOOD
PMIC_CTL4
PMIC_IRQB
add to CPLD sheet
J2
HDR 1X3
U18D
TPS65086100RSKT
7-bit I2C Address: 0x5E
VR1
NCP51400MNTXG
PCB Note : Connect VOSNS to the remote DDR termination bypass capacitors.
Title
Size C
Document Number
Rev 0.1
Date: Thursday, September 16, 2021
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