In all the scopes rails are as following:

Blue – (2) - VLDO3 (+3.3V); (the rail supplying all the 3.3V for the CPU)

Fuchsia – (3) - Vin PMIC (VIN_DCDCx, VINLDO) (+5.2V);

Yelow – (1) - Vout DCDC3 (L3) (+1.1V) (the rail supplying the CPU Vcore);

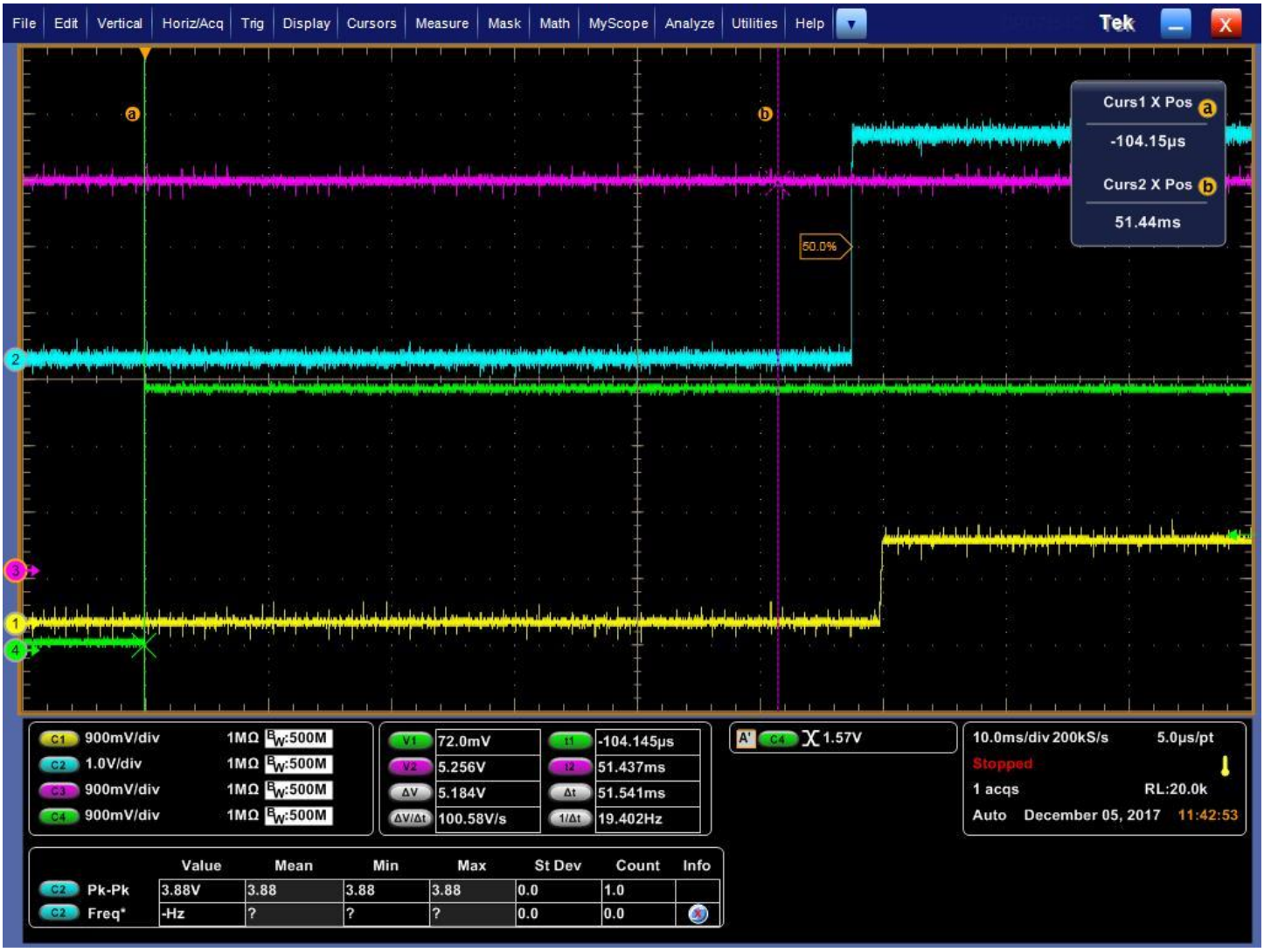
Green – (4) - PWR_EN (pin 9 on the PMIC) this is driven by a voltage supervisor (TPS3808G01) monitoring the system 12V input power…

Power Off faulty sequence. The +1.1V (core rail) can be seen shutting up to 3.5V for about 840uS !!!!!!. This happens most likely due to wrong internal PMIC design or badly PMIC misbehaving for Vpmic (VINDCDCx…) at or approaching UVLO (3.3V). Clearly seen above…..

Please see below the details of the +1.1V (CPU core voltage) reaching and siting at +3.4V !!!!! for 840uS !!!!! (this is where we believe the CPU connected to this PMIC will have an extremely hard time ???!!!).

The same behavior can be seen for the DCDC1 (L1) the rail providing +1.8V to the CPU and DDR2 memory….


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
50.0%
Curs1 X Pos a
47.27ms
Curs2 X Pos b
48.11ms
C1 900mV/div 1MΩ BW:500M
C2 1.0V/div 1MΩ BW:500M
C3 900mV/div 1MΩ BW:500M
C4 900mV/div 1MΩ BW:500M
Z1C1 900mV 667µs 44.2ms 50.9ms
Z1C2 1.0V 667µs 44.2ms 50.9ms
Z1C3 900mV 667µs 44.2ms 50.9ms
Z1C4 900mV 667µs 44.2ms 50.9ms
A' C4 1.57V
10.0ms/div 200kS/s 5.0µs/pt
Preview
0 acqs RL:20.0k
Auto December 05, 2017 11:39:57
Value Mean Min Max St Dev Count Info
C2 Pk-Pk 3.76V 3.76 3.76 3.76 0.0 1.0
C2 Freq* -Hz ? ? ? 0.0 0.0
V1 3.6V
V2 3.06V
ΔV -540mV
ΔV/Δt -642.238V/s
t1 47.266ms
t2 48.107ms
Δt 840.81µs
1/Δt 1.189kHz



The Power On sequence is always correct initiated after the PWR_EN deglitch time (50mS typ) (+/-20% from what I can gather…); GREEN trace (4) going HIGH….

Power OFF correctly initiated after PWR_EN going LOW.

Notice that in this case the Vin PMIC (VINDCDCx) was at around +3.6V at the time the power-off sequence has been initiated after a shorter that 50mS PWR_EN deglitch time…. (the Vin PMIC never reached the UVLO (+3.3V) for the whole duration of the power-off sequence)

Note: 100uF tantalum cap have been added to keep the Vin PMIC longer….

From this moment on I kept the Vin PMIC (VINDCDCx) always ON and the PWR_EN pin was used to verify the 50mS deglitch time (after noticing that the value in the datasheet is a TYP value AND more concerning this value of 50mS was “not tested in production” according with the same datasheet…..!!!!). To my unpleasant surprise, the deglitch time varies widely from around 35mS to more than 890mS !!!!!!! which renders unrealistic the use of caps to keep the Vin PMIC (VINDCDCx) reaching the UVLO before the power sequence finishes (in the case of power plug being unexpectedly disconnected from the system).

Please see below scopes that show power sequence being initiated at very different times after the PWR_EN pin was PULLED LOW.

Power OFF sequence initiated roughly 393mS after PWR_EN = LOW; Please notice the Vin PMIC (VINDCDCx) is kept at 5.2V

Power OFF sequence initiated roughly 660mS after PWR_EN = LOW; Please notice the Vin PMIC (VINDCDCx) is kept at 5.2V

Power OFF sequence WAS initiated after 900mS after PWR_EN = LOW; Please notice the Vin PMIC (VINDCDCx) is kept at 5.2V. Also, at this time the scope was set with 100ms/div and unfortunately the rails going down was not captured but I can tell for sure they eventually went down…!!!!!