TPS6594 all registers are 0:

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| **User Registers - Page 0** | 　 | 　 | 　 | 　 | 　 | 　 |
| DEV\_REV | 　 | 0x01 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NVM\_CODE\_1 | 　 | 0x02 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NVM\_CODE\_2 | 　 | 0x03 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK1\_CTRL | 　 | 0x04 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK1\_CONF | 　 | 0x05 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK2\_CTRL | 　 | 0x06 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK2\_CONF | 　 | 0x07 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK3\_CTRL | 　 | 0x08 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK3\_CONF | 　 | 0x09 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_CTRL | 　 | 0x0A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_CONF | 　 | 0x0B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK1\_VOUT\_1 | 　 | 0x0E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK1\_VOUT\_2 | 　 | 0x0F |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK2\_VOUT\_1 | 　 | 0x10 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK2\_VOUT\_2 | 　 | 0x11 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK3\_VOUT\_1 | 　 | 0x12 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK3\_VOUT\_2 | 　 | 0x13 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_VOUT\_1 | 　 | 0x14 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_VOUT\_2 | 　 | 0x15 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK1\_PG\_WINDOW | 　 | 0x18 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK2\_PG\_WINDOW | 　 | 0x19 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK3\_PG\_WINDOW | 　 | 0x1A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_PG\_WINDOW | 　 | 0x1B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| LDOINT\_CTRL | 　 | 0x21 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VCCA\_VMON\_CTRL | 　 | 0x2B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VCCA\_PG\_WINDOW | 　 | 0x2C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VMON1\_PG\_WINDOW | 　 | 0x2D |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VMON1\_PG\_LEVEL | 　 | 0x2E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VMON2\_PG\_WINDOW | 　 | 0x2F |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VMON2\_PG\_LEVEL | 　 | 0x30 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO1\_CONF | 　 | 0x31 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO2\_CONF | 　 | 0x32 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO3\_CONF | 　 | 0x33 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO4\_CONF | 　 | 0x34 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO5\_CONF | 　 | 0x35 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO6\_CONF | 　 | 0x36 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO7\_CONF | 　 | 0x37 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO8\_CONF | 　 | 0x38 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO9\_CONF | 　 | 0x39 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO10\_CONF | 　 | 0x3A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ENABLE\_CONF | 　 | 0x3C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO\_OUT\_1 | 　 | 0x3D |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO\_OUT\_2 | 　 | 0x3E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO\_IN\_1 | 　 | 0x3F |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO\_IN\_2 | 　 | 0x40 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RAIL\_SEL\_1 | 　 | 0x41 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RAIL\_SEL\_3 | 　 | 0x43 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_TRIG\_SEL\_1 | 　 | 0x44 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_TRIG\_SEL\_2 | 　 | 0x45 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_TRIG\_MASK\_1 | 　 | 0x46 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_TRIG\_MASK\_2 | 　 | 0x47 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_TRIG\_MASK\_3 | 　 | 0x48 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_BUCK1\_2 | 　 | 0x49 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_BUCK3\_4 | 　 | 0x4A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_VMON | 　 | 0x4E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_GPIO1\_8\_FALL | 　 | 0x4F |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_GPIO1\_8\_RISE | 　 | 0x50 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_GPIO9\_10 | 　 | 0x51 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_STARTUP | 　 | 0x52 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_MISC | 　 | 0x53 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_MODERATE\_ERR | 　 | 0x54 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_FSM\_ERR | 　 | 0x56 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_COMM\_ERR | 　 | 0x57 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_READBACK\_ERR | 　 | 0x58 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_ESM | 　 | 0x59 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_TOP | 　 | 0x5A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_BUCK | 　 | 0x5B | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_BUCK1\_2 | 　 | 0x5C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_BUCK3\_4 | 　 | 0x5D |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_VMON | 　 | 0x62 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_GPIO | 　 | 0x63 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_GPIO1\_8 | 　 | 0x64 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_STARTUP | 　 | 0x65 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_MISC | 　 | 0x66 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_MODERATE\_ERR | 　 | 0x67 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_SEVERE\_ERR | 　 | 0x68 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_FSM\_ERR | 　 | 0x69 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_COMM\_ERR | 　 | 0x6A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_READBACK\_ERR | 　 | 0x6B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_ESM | 　 | 0x6C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_BUCK1\_2 | 　 | 0x6D | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_BUCK3\_4 | 　 | 0x6E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_VMON | 　 | 0x72 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_STARTUP | 　 | 0x73 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_MISC | 　 | 0x74 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_MODERATE\_ERR | 　 | 0x75 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_SEVERE\_ERR | 　 | 0x76 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_READBACK\_ERR | 　 | 0x77 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PGOOD\_SEL\_1 | 　 | 0x78 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PGOOD\_SEL\_4 | 　 | 0x7B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PLL\_CTRL | 　 | 0x7C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CONFIG\_1 | 　 | 0x7D |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ENABLE\_DRV\_REG | 　 | 0x80 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MISC\_CTRL | 　 | 0x81 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ENABLE\_DRV\_STAT | 　 | 0x82 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RECOV\_CNT\_REG\_1 | 　 | 0x83 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RECOV\_CNT\_REG\_2 | 　 | 0x84 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_I2C\_TRIGGERS | 　 | 0x85 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_NSLEEP\_TRIGGERS | 　 | 0x86 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK\_RESET\_REG | 　 | 0x87 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPREAD\_SPECTRUM\_1 | 　 | 0x88 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FREQ\_SEL | 　 | 0x8A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_STEP\_SIZE | 　 | 0x8B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| USER\_SPARE\_REGS | 　 | 0x8E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_START\_REG | 　 | 0x8F |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_DELAY1\_REG | 　 | 0x90 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_DELAY2\_REG | 　 | 0x91 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_MODE\_CFG | 　 | 0x92 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_HMAX\_REG | 　 | 0x93 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_HMIN\_REG | 　 | 0x94 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_LMAX\_REG | 　 | 0x95 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_LMIN\_REG | 　 | 0x96 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_ERR\_CNT\_REG | 　 | 0x97 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| REGISTER\_LOCK | 　 | 0xA1 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| USER\_EE\_CTRL\_1 | 　 | 0xA2 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| USER\_EE\_CTRL\_2 | 　 | 0xA3 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SRAM\_ADDR\_CTRL | 　 | 0xA4 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RECOV\_CNT\_PFSM\_INCR | 　 | 0xA5 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MANUFACTURING\_VER | 　 | 0xA6 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CUSTOMER\_NVM\_ID\_REG | 　 | 0xA7 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VMON\_CONF | 　 | 0xA8 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_SPI\_STATUS | 　 | 0xA9 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SOFT\_REBOOT\_REG | 　 | 0xAB |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STARTUP\_CTRL | 　 | 0xC3 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCRATCH\_PAD\_REG\_1 | 　 | 0xC9 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCRATCH\_PAD\_REG\_2 | 　 | 0xCA |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCRATCH\_PAD\_REG\_3 | 　 | 0xCB |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCRATCH\_PAD\_REG\_4 | 　 | 0xCC |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PFSM\_DELAY\_REG\_1 | 　 | 0xCD |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PFSM\_DELAY\_REG\_2 | 　 | 0xCE |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PFSM\_DELAY\_REG\_3 | 　 | 0xCF |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PFSM\_DELAY\_REG\_4 | 　 | 0xD0 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CRC Registers - Page 0** | 　 | 　 | 　 | 　 | 　 | 　 |
| CRC\_CALC\_CONTROL | 　 | 0xEF |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_1 | 　 | 0xF0 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_2 | 　 | 0xF1 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_3 | 　 | 0xF2 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_4 | 　 | 0xF3 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_5 | 　 | 0xF4 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_6 | 　 | 0xF5 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_7 | 　 | 0xF6 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_8 | 　 | 0xF7 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_9 | 　 | 0xF8 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_10 | 　 | 0xF9 | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_15 | 　 | 0xFE | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_16 | 　 | 0xFF | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **WatchDog Registers - Page 4** | 　 | 　 | 　 | 　 | 　 | 　 |
| WD\_ANSWER\_REG | 　 | 0x01 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| WD\_QUESTION\_ANSW\_CNT | 　 | 0x02 |

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 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| WD\_WIN1\_CFG | 　 | 0x03 |

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 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| WD\_WIN2\_CFG | 　 | 0x04 |

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 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| WD\_LONGWIN\_CFG | 　 | 0x05 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| WD\_MODE\_REG | 　 | 0x06 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| WD\_QA\_CFG | 　 | 0x07 |

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 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| WD\_ERR\_STATUS | 　 | 0x08 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| WD\_THR\_CFG | 　 | 0x09 |

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 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| WD\_FAIL\_CNT\_REG | 　 | 0x0A |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

LP8764 registers :

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| **User Registers - Page 0** | 　 | 　 | 　 | 　 | 　 | 　 |
| DEV\_REV | 　 | 0x01 |

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 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| NVM\_CODE\_1 | 　 | 0x02 |

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 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| NVM\_CODE\_2 | 　 | 0x03 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK1\_CTRL | 　 | 0x04 |

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 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| BUCK1\_CONF | 　 | 0x05 |

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 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| BUCK2\_CTRL | 　 | 0x06 |

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 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| BUCK2\_CONF | 　 | 0x07 |

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 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| BUCK3\_CTRL | 　 | 0x08 |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| BUCK3\_CONF | 　 | 0x09 |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| BUCK4\_CTRL | 　 | 0x0A |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_CONF | 　 | 0x0B |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| BUCK1\_VOUT\_1 | 　 | 0x0E |

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 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| BUCK1\_VOUT\_2 | 　 | 0x0F |

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 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| BUCK2\_VOUT\_1 | 　 | 0x10 |

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 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| BUCK2\_VOUT\_2 | 　 | 0x11 |

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 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| BUCK3\_VOUT\_1 | 　 | 0x12 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK3\_VOUT\_2 | 　 | 0x13 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_VOUT\_1 | 　 | 0x14 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_VOUT\_2 | 　 | 0x15 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK1\_PG\_WINDOW | 　 | 0x18 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| BUCK2\_PG\_WINDOW | 　 | 0x19 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| BUCK3\_PG\_WINDOW | 　 | 0x1A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK4\_PG\_WINDOW | 　 | 0x1B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| LDOINT\_CTRL | 　 | 0x21 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VCCA\_VMON\_CTRL | 　 | 0x2B |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| VCCA\_PG\_WINDOW | 　 | 0x2C |

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 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| VMON1\_PG\_WINDOW | 　 | 0x2D |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 　 | 　 | 　 | 　 | 　 | 　 | 　 | 　 | 　 | 　 | 　 | 　 |
| VMON1\_PG\_LEVEL | 　 | 0x2E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VMON2\_PG\_WINDOW | 　 | 0x2F |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VMON2\_PG\_LEVEL | 　 | 0x30 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO1\_CONF | 　 | 0x31 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| GPIO2\_CONF | 　 | 0x32 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| GPIO3\_CONF | 　 | 0x33 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| GPIO4\_CONF | 　 | 0x34 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| GPIO5\_CONF | 　 | 0x35 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| GPIO6\_CONF | 　 | 0x36 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| GPIO7\_CONF | 　 | 0x37 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| GPIO8\_CONF | 　 | 0x38 |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| GPIO9\_CONF | 　 | 0x39 |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| GPIO10\_CONF | 　 | 0x3A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ENABLE\_CONF | 　 | 0x3C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO\_OUT\_1 | 　 | 0x3D |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO\_OUT\_2 | 　 | 0x3E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO\_IN\_1 | 　 | 0x3F |

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 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| GPIO\_IN\_2 | 　 | 0x40 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RAIL\_SEL\_1 | 　 | 0x41 |

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 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| RAIL\_SEL\_3 | 　 | 0x43 |

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 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| FSM\_TRIG\_SEL\_1 | 　 | 0x44 |

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 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| FSM\_TRIG\_SEL\_2 | 　 | 0x45 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| FSM\_TRIG\_MASK\_1 | 　 | 0x46 |

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 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| FSM\_TRIG\_MASK\_2 | 　 | 0x47 |

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 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| FSM\_TRIG\_MASK\_3 | 　 | 0x48 |

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 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| MASK\_BUCK1\_2 | 　 | 0x49 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_BUCK3\_4 | 　 | 0x4A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_VMON | 　 | 0x4E |

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 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| MASK\_GPIO1\_8\_FALL | 　 | 0x4F |

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 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 　 |
| MASK\_GPIO1\_8\_RISE | 　 | 0x50 |

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 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| MASK\_GPIO9\_10 | 　 | 0x51 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| MASK\_STARTUP | 　 | 0x52 |

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 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| MASK\_MISC | 　 | 0x53 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| MASK\_MODERATE\_ERR | 　 | 0x54 |

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 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_FSM\_ERR | 　 | 0x56 |

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 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MASK\_COMM\_ERR | 　 | 0x57 |

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 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| MASK\_READBACK\_ERR | 　 | 0x58 |

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 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| MASK\_ESM | 　 | 0x59 |

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 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| INT\_TOP | 　 | 0x5A |

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 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| INT\_BUCK | 　 | 0x5B | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_BUCK1\_2 | 　 | 0x5C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_BUCK3\_4 | 　 | 0x5D |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_VMON | 　 | 0x62 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| INT\_GPIO | 　 | 0x63 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_GPIO1\_8 | 　 | 0x64 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_STARTUP | 　 | 0x65 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_MISC | 　 | 0x66 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| INT\_MODERATE\_ERR | 　 | 0x67 |

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 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| INT\_SEVERE\_ERR | 　 | 0x68 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_FSM\_ERR | 　 | 0x69 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| INT\_COMM\_ERR | 　 | 0x6A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_READBACK\_ERR | 　 | 0x6B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_ESM | 　 | 0x6C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_BUCK1\_2 | 　 | 0x6D | 　 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_BUCK3\_4 | 　 | 0x6E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_VMON | 　 | 0x72 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_STARTUP | 　 | 0x73 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_MISC | 　 | 0x74 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_MODERATE\_ERR | 　 | 0x75 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_SEVERE\_ERR | 　 | 0x76 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STAT\_READBACK\_ERR | 　 | 0x77 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PGOOD\_SEL\_1 | 　 | 0x78 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PGOOD\_SEL\_4 | 　 | 0x7B |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PLL\_CTRL | 　 | 0x7C |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CONFIG\_1 | 　 | 0x7D |

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 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| ENABLE\_DRV\_REG | 　 | 0x80 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MISC\_CTRL | 　 | 0x81 |

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 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| ENABLE\_DRV\_STAT | 　 | 0x82 |

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 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| RECOV\_CNT\_REG\_1 | 　 | 0x83 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| RECOV\_CNT\_REG\_2 | 　 | 0x84 |

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 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| FSM\_I2C\_TRIGGERS | 　 | 0x85 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_NSLEEP\_TRIGGERS | 　 | 0x86 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BUCK\_RESET\_REG | 　 | 0x87 |

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 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| SPREAD\_SPECTRUM\_1 | 　 | 0x88 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FREQ\_SEL | 　 | 0x8A |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FSM\_STEP\_SIZE | 　 | 0x8B |

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 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| USER\_SPARE\_REGS | 　 | 0x8E |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_START\_REG | 　 | 0x8F |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_DELAY1\_REG | 　 | 0x90 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_DELAY2\_REG | 　 | 0x91 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_MODE\_CFG | 　 | 0x92 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_HMAX\_REG | 　 | 0x93 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_HMIN\_REG | 　 | 0x94 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_LMAX\_REG | 　 | 0x95 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_LMIN\_REG | 　 | 0x96 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ESM\_MCU\_ERR\_CNT\_REG | 　 | 0x97 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| REGISTER\_LOCK | 　 | 0xA1 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| USER\_EE\_CTRL\_1 | 　 | 0xA2 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| USER\_EE\_CTRL\_2 | 　 | 0xA3 |

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 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SRAM\_ADDR\_CTRL | 　 | 0xA4 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RECOV\_CNT\_PFSM\_INCR | 　 | 0xA5 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MANUFACTURING\_VER | 　 | 0xA6 |

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 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| CUSTOMER\_NVM\_ID\_REG | 　 | 0xA7 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VMON\_CONF | 　 | 0xA8 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| INT\_SPI\_STATUS | 　 | 0xA9 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SOFT\_REBOOT\_REG | 　 | 0xAB |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| STARTUP\_CTRL | 　 | 0xC3 |

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 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| SCRATCH\_PAD\_REG\_1 | 　 | 0xC9 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCRATCH\_PAD\_REG\_2 | 　 | 0xCA |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCRATCH\_PAD\_REG\_3 | 　 | 0xCB |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCRATCH\_PAD\_REG\_4 | 　 | 0xCC |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PFSM\_DELAY\_REG\_1 | 　 | 0xCD |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PFSM\_DELAY\_REG\_2 | 　 | 0xCE |

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 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| PFSM\_DELAY\_REG\_3 | 　 | 0xCF |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PFSM\_DELAY\_REG\_4 | 　 | 0xD0 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CRC Registers - Page 0** | 　 | 　 | 　 | 　 | 　 | 　 |
| CRC\_CALC\_CONTROL | 　 | 0xEF |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC\_1 | 　 | 0xF0 |

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 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| CRC\_2 | 　 | 0xF1 | 　 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| CRC\_3 | 　 | 0xF2 | 　 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| CRC\_4 | 　 | 0xF3 | 　 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| CRC\_5 | 　 | 0xF4 | 　 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| CRC\_6 | 　 | 0xF5 | 　 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| CRC\_7 | 　 | 0xF6 | 　 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| CRC\_8 | 　 | 0xF7 | 　 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| CRC\_9 | 　 | 0xF8 | 　 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| CRC\_10 | 　 | 0xF9 | 　 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| CRC\_15 | 　 | 0xFE | 　 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| CRC\_16 | 　 | 0xFF | 　 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| **WatchDog Registers - Page 4** | 　 | 　 | 　 | 　 | 　 | 　 |
| WD\_ANSWER\_REG | 　 | 0x01 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| WD\_QUESTION\_ANSW\_CNT | 　 | 0x02 |

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 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| WD\_WIN1\_CFG | 　 | 0x03 |

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 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| WD\_WIN2\_CFG | 　 | 0x04 |

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 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| WD\_LONGWIN\_CFG | 　 | 0x05 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| WD\_MODE\_REG | 　 | 0x06 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| WD\_QA\_CFG | 　 | 0x07 |

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 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| WD\_ERR\_STATUS | 　 | 0x08 |

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 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| WD\_THR\_CFG | 　 | 0x09 |

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 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| WD\_FAIL\_CNT\_REG | 　 | 0x0A |

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 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |