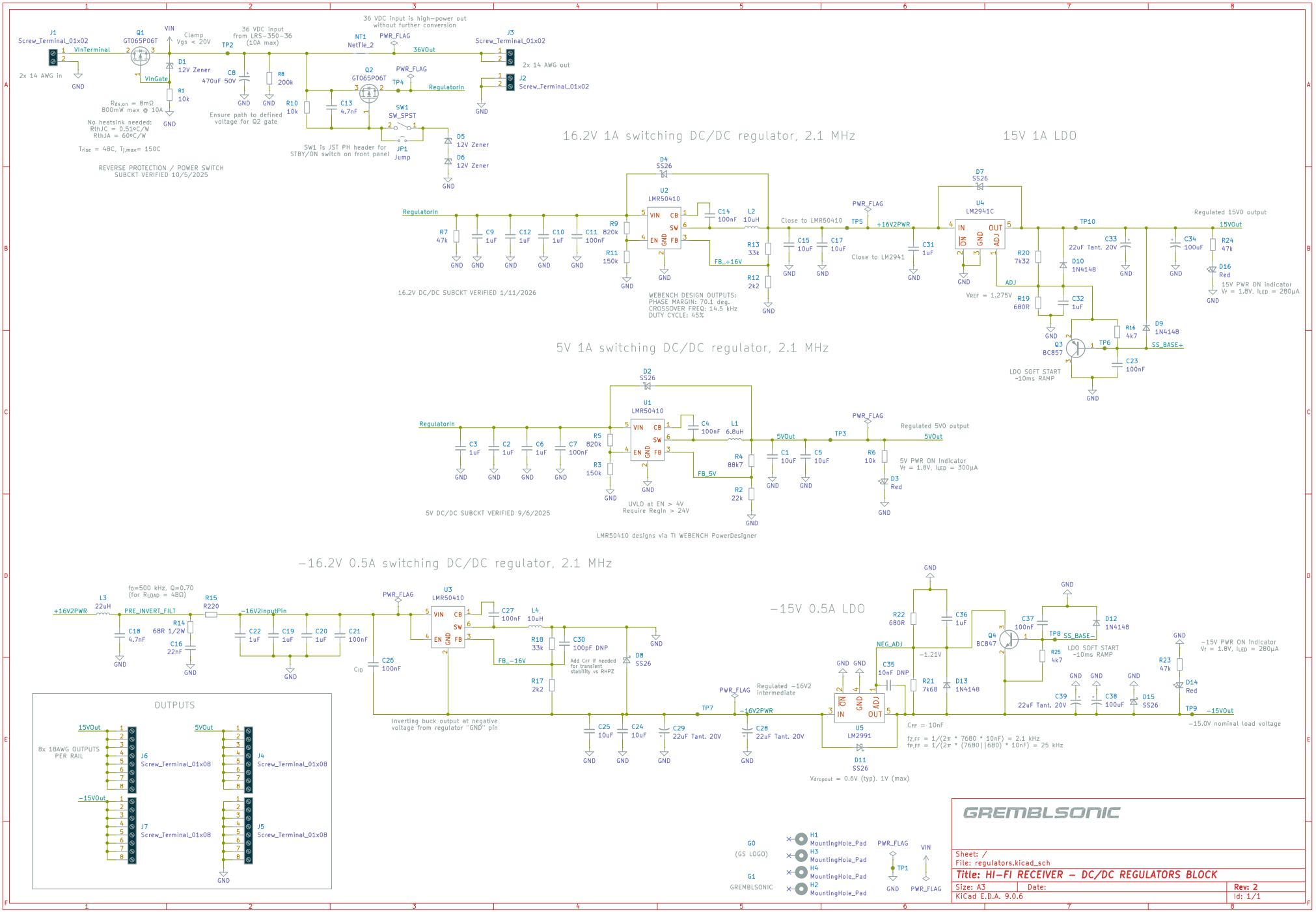
J1
Screw_Terminal_01x02
2x 14 AWG in
VInTerminal
GND
Q1
GT065P06T
VIN
Clamp
Vgs < 20V
D1
12V Zener
VInGate
R1
10k
Rds,on = 8mΩ
800mW max @ 10A
No heatsink needed:
RthJC = 0.51°C/W
RthJA = 60°C/W
Trise = 48C, Tj,max= 150C
REVERSE PROTECTION / POWER SWITCH
SUBCKT VERIFIED 10/5/2025
TP2
36 VDC Input
from LRS-350-36
(10A max)
C8
470uF 50V
R8
200k
R10
10k
Ensure path to defined
voltage for Q2 gate
C13
4.7nF
Q2
GT065P06T
TP4
PWR_FLAG
RegulatorIn
SW1
SW_SPST
JP1
Jump
SW1 is JST PH header for
STBY/ON switch on front panel
D5
12V Zener
D6
12V Zener
NT1
NetTie_2
36 VDC input is high-power out
without further conversion
36VOut
J3
Screw_Terminal_01x02
2x 14 AWG out
J2
Screw_Terminal_01x02
16.2V 1A switching DC/DC regulator, 2.1 MHz
D4
SS26
U2
LMR50410
VIN
CB
SW
EN
GND
FB
R7
47k
C9
1uF
C12
1uF
C10
1uF
C11
100nF
R9
820k
R11
150k
C14
100nF
L2
10uH
R13
33k
R12
2k2
FB_+16V
16.2V DC/DC SUBCKT VERIFIED 1/11/2026
WEBENCH DESIGN OUTPUTS:
PHASE MARGIN: 70.1 deg.
CROSSOVER FREQ: 14.5 kHz
DUTY CYCLE: 45%
Close to LMR50410
C15
10uF
C17
10uF
TP5
+16V2PWR
Close to LM2941
C31
1uF
15V 1A LDO
D7
SS26
U4
LM2941C
IN
ON
GND
OUT
ADJ
R20
7k32
R19
680R
C32
1uF
VREF = 1.275V
TP10
22uF Tant. 20V
D10
1N4148
C33
C34
100uF
Regulated 15V0 output
15VOut
R24
47k
D16
Red
15V PWR ON Indicator
VF = 1.8V, ILED = 280µA
R16
4k7
D9
1N4148
SS_BASE+
Q3
BC857
TP6
C23
100nF
LDO SOFT START
~10ms RAMP
5V 1A switching DC/DC regulator, 2.1 MHz
D2
SS26
U1
LMR50410
C3
1uF
C2
1uF
C6
1uF
C7
100nF
R5
820k
R3
150k
C4
100nF
L1
6.8uH
R4
88k7
R2
22k
FB_5V
UVLO at EN > 4V
Require RegIn > 24V
5V DC/DC SUBCKT VERIFIED 9/6/2025
LMR50410 designs via TI WEBENCH PowerDesigner
5VOut
C1
10uF
C5
10uF
TP3
R6
10k
D3
Red
5V PWR ON Indicator
VF = 1.8V, ILED = 300µA
−16.2V 0.5A switching DC/DC regulator, 2.1 MHz
fc=500 kHz, Q=0.70
(for RLOAD = 48Ω)
L3
22uH
+16V2PWR
PRE_INVERT_FILT
R15
R220
−16V2InputPin
C18
4.7nF
R14
68R 1/2W
C16
22nF
C22
1uF
C19
1uF
C20
1uF
C21
100nF
C26
100nF
U3
LMR50410
C27
100nF
L4
10uH
R18
33k
C30
100pF DNP
Add Crr if needed
for transient
stability vs RHPZ
D8
SS26
R17
2k2
FB_−16V
Inverting buck output at negative
voltage from regulator "GND" pin
C25
10uF
C24
10uF
C29
22uF Tant. 20V
C28
22uF Tant. 20V
TP7
Regulated −16V2
intermediate
−16V2PWR
−15V 0.5A LDO
R22
680R
C36
1uF
NEG_ADJ
−1.21V
C35
10nF DNP
R21
7k68
D13
1N4148
U5
LM2991
D11
SS26
Vdropout = 0.6V (typ), 1V (max)
Crr = 10nF
fZ,FF = 1/(2π * 7680 * 10nF) = 2.1 kHz
fP,FF = 1/(2π * (7680||680) * 10nF) = 25 kHz
Q4
BC847
C37
100nF
TP8
SS_BASE−
R25
4k7
D12
1N4148
LDO SOFT START
~10ms RAMP
C39
22uF Tant. 20V
C38
100uF
D15
SS26
R23
47k
D14
Red
−15V PWR ON Indicator
VF = 1.8V, ILED = 280µA
TP9
−15VOut
−15.0V nominal load voltage
OUTPUTS
8x 18AWG OUTPUTS
PER RAIL
15VOut
5VOut
−15VOut
J6
Screw_Terminal_01x08
J4
Screw_Terminal_01x08
J7
Screw_Terminal_01x08
J5
Screw_Terminal_01x08
G0
(GS LOGO)
G1
GREMBLSONIC
H1
MountingHole_Pad
H3
MountingHole_Pad
H4
MountingHole_Pad
H2
MountingHole_Pad
TP1
GREMBLSONIC
Sheet: /
File: regulators.kicad_sch
Title: HI-FI RECEIVER – DC/DC REGULATORS BLOCK
Size: A3
Date:
Rev: 2
KiCad E.D.A. 9.0.6
Id: 1/1