

Design Summary for MicroSiP™-enabled TPS8267xSiP



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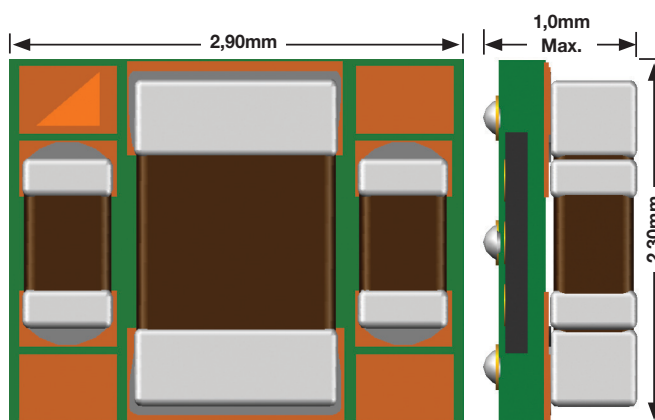
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MicroSiP™ package

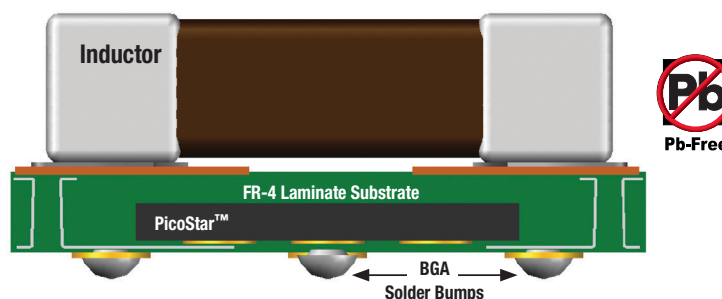
Introduction

As the marketplace continues to demand size reductions in portable electronic products, the need for smaller packaging and smaller subsystem packaging becomes paramount. In addition, size reductions can no longer focus only on package surface area, meaning length and width, but also must decrease the package thickness and weight. To address these rapidly evolving customer requirements, TI has introduced MicroSiP™, the latest innovation in System-in-Package (SiP) technology integrating IC and passive components in a single device featuring an embedded PicoStar™. The small MicroSiP footprint provides a stand-alone power supply platform driving an unprecedented power to package density of 90mA/mm². MicroSiP (package designator SIP) is offered today in a 8-pin format for the TPS8267x.

Packaging Attributes

Attribute	8-ball
Ball Pitch	0,8/1,0mm**
Ball Diameter	0,30mm
Package Length	~2,30mm
Package Width	~2,90mm
Package Height	1,0mm max
Bump Matrix	3x3
Bump Metallurgy	SAC305
Moisture Level	Level 2 at 260°C

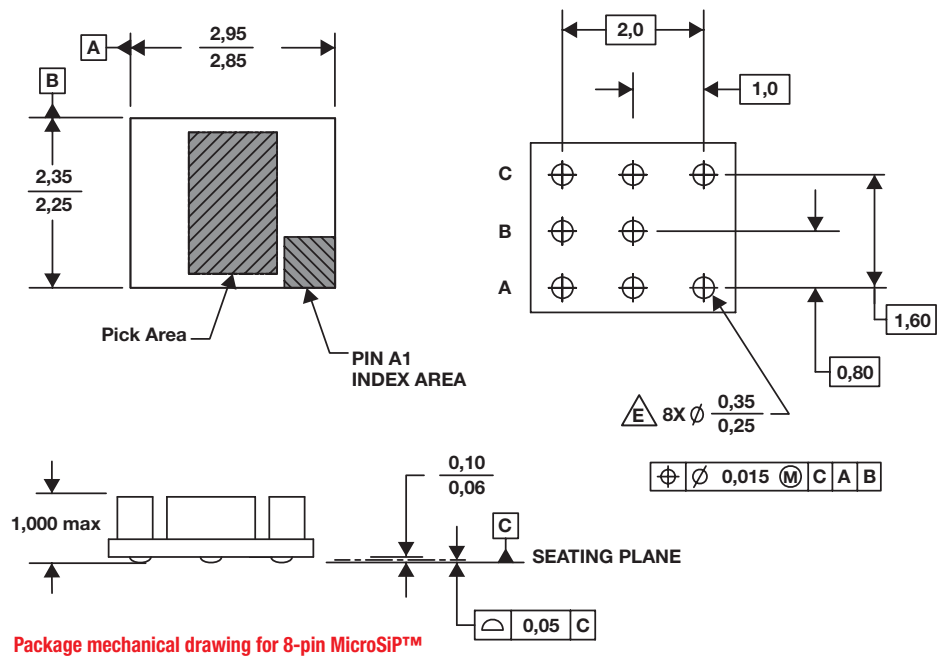
** Bump pitch is 1,0mm in x direction, 0,8mm in y direction.



MicroSiP™ cross-sectional view

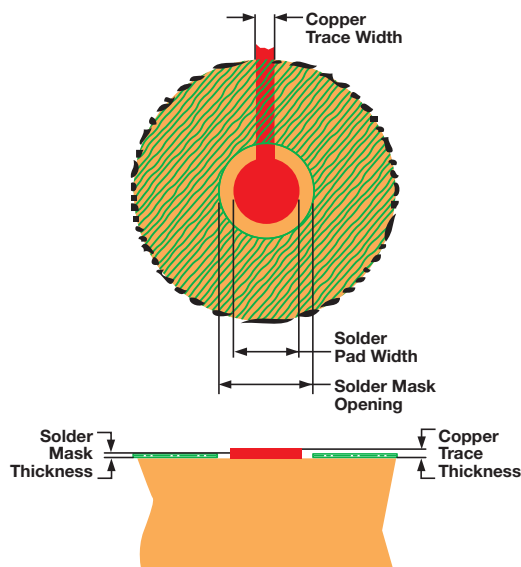
8-pin MicroSiP™ Package Drawing

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994
- This drawing is subject to change without notice
- MicroSiP package configuration - Micro system in package
- Reference product data sheet for array population. 3x3 matrix pattern is shown for illustration purposes only
- This package contains Pb-free balls



Board Layout

When designing the pad size for the MicroSiP™ solder bumps, it is recommended that the layout use a non-solder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Table below shows the appropriate diameters for the 8-pin MicroSiP™ layout.



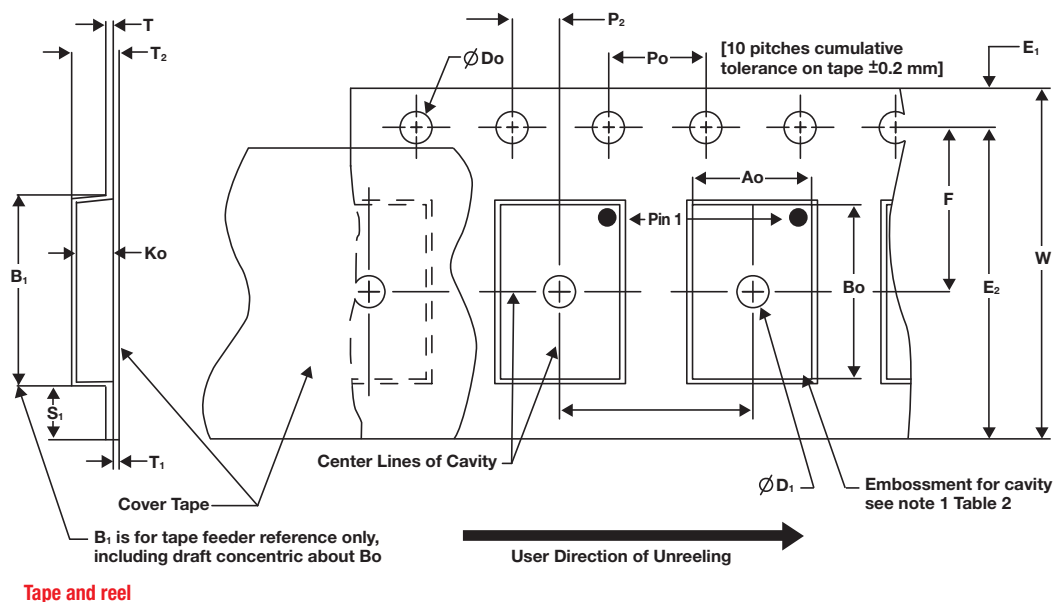
Land pattern image

Land Pattern Dimensions

Solder Pad Definitions	Copper Pad	Solder Mask (5) Opening	Copper Thickness	Stencil (6) Opening	Stencil Thickness
Non-solder mask undefined (NSMD)	0.30mm	.360mm	1 oz. max (0.032 mm)	.34mm diameter	0.1mm thick

- Circuit traces from NSMD defined PWB lands should be 75µm to 100µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability
- Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating range of the intended application
- Recommend solder paste is Type 3 or Type 4
- For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5µm to avoid a reduction in thermal fatigue performance
- Solder mask thickness should be less than 20µm on top of the copper circuit pattern
- Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils give inferior solder paste volume control

Packaging Information



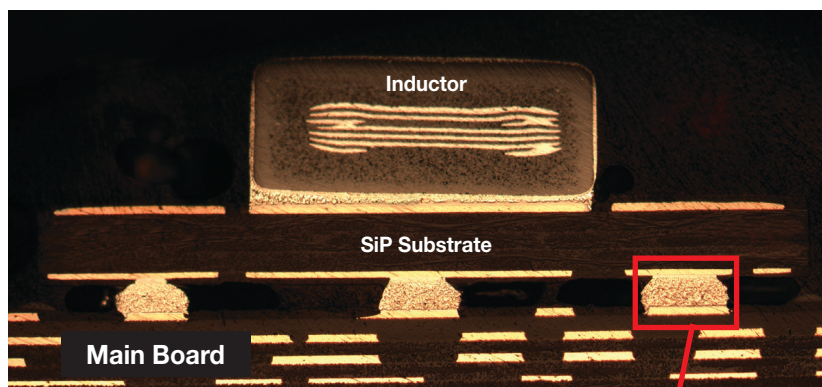
Package	Carrier-Tape Width (W)	Pocket Pitch (P)	Pocket Width (Ao)	Pocket Length (Bo)	Pocket Depth (Ko)	Reel Diameter
MicroSiP™	8.0 ± 0.30	4.0 ± 0.10	2.45 ± 0.05	3.05 ± 0.05	1.1 ± 0.05	178

Do	D1 Min	E1	Po	P2	R Ref.	S1 Min.	T Max.	T ₁₀ Max.
1.5+0.1 -0.0	1.5	1.75 ± 0.1	4.0 ± 0.	2.0 ± .05	30	0.6	0.6	0.25

Orient component as shown with Pin 1 closest to the tape sprocket holes on tape leading edge. All dimensions in millimeters.

MicroSiP™ Surface Mount

Surface mounting of MicroSiP packages is broadly similar to BGA package assembly. TI recommends the use of Pb-free solder paste applied via a 0.1mm thick stencil (critical stencil dimensions shown in board layout subsection). The paste acts: to aid wetting of the SiP bump to the board land, to hold the SiP in place during reflow, and to contribute metal volume of the resultant solder joint. Standard JEDEC reflow profiles for near-eutectic SnAgCu solder alloys are suggested (max 260°C). Board-SiP solder joint height is 120µm.

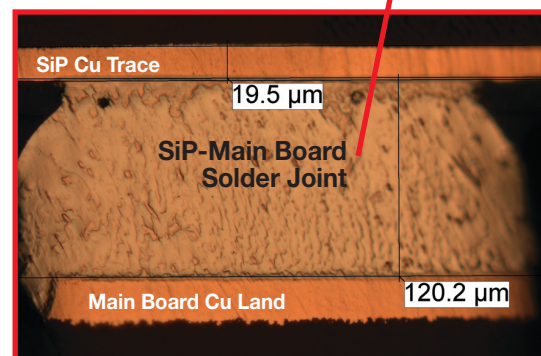


Cross-section of MicroSiP™ mounted to main board

Board-Level Reliability Data

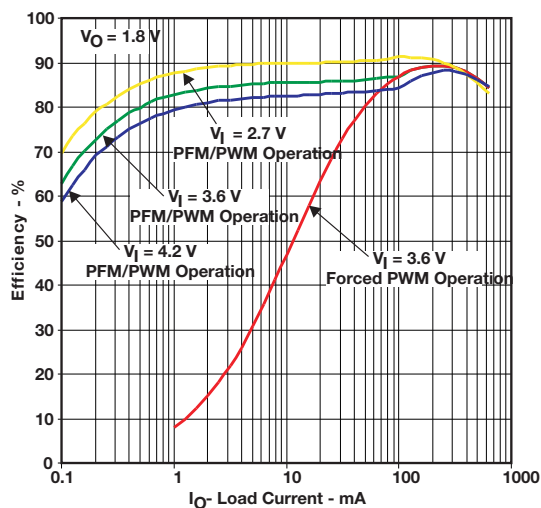
8-pin MicroSiP™		
	Test Parameters	Results ($t_{first fail}$)
Drop	1500G/1.0ms pulse	> 100 drops
Temp Cycle	-40/125°C, 2 cycles/hr	> 1000 cycles

No underfill or adhesive was either used or required for these packages. Preconditioning: 3 pass reflow + 24hr/125°C bake 0.7mm thick FR4 epoxy main board.



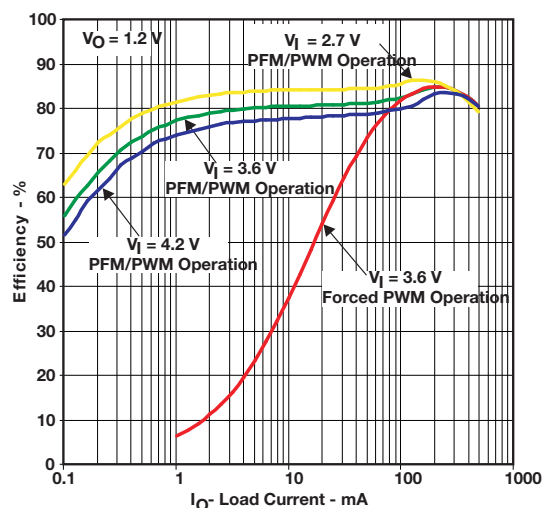
Electrical Characterization

A - Efficiency vs Load Current

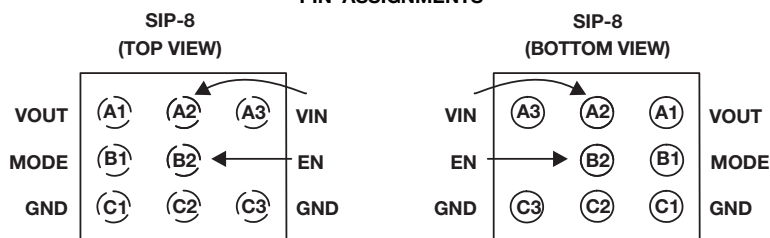


Plot of efficiency as a function of current for
A) $V_O=1.8V$ and B) $V_O=1.2V$

B - Efficiency vs Load Current

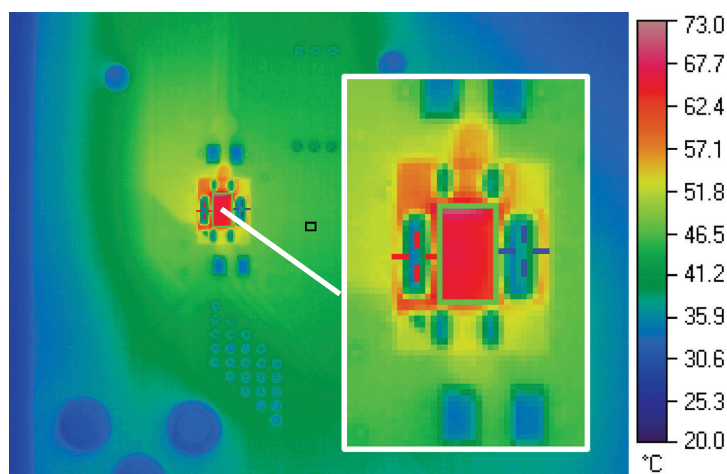


PIN ASSIGNMENTS

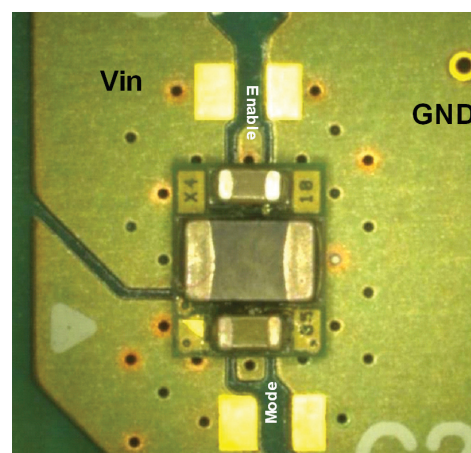


Pin Description

Thermal Evaluation



Thermal Image of MicroSiP™ when IC is dissipating 0.45W. Ambient temperature is 22°C, max junction temperature is 72°C. For thermal modeling, a value of $\Theta_{JA}=125^{\circ}\text{C/W}$ provides an excellent initial estimate of thermal performance.



Close-up of MicroSiP™ mounted to the TI EVM

Package Label

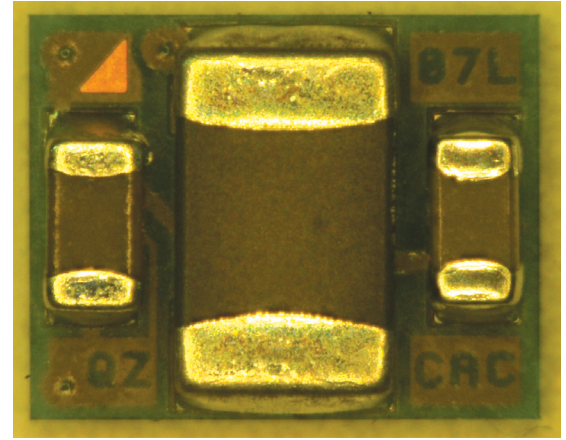
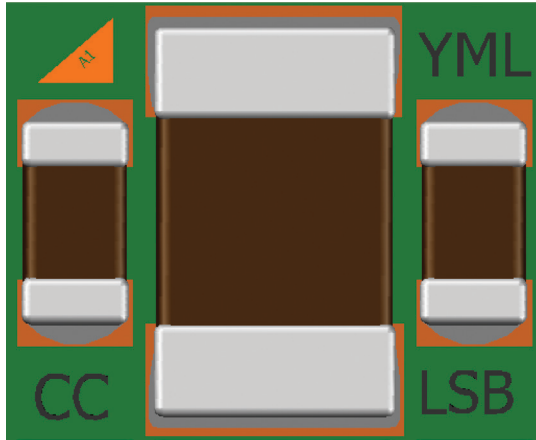
Typical view of the SiP marking in the top of the package. Marking includes both lot trace coding and pin 1 indicator.

Code:

CC - Device Code

YML - Date Code

LSB - Lot/Site/Board
Trace Code



MicroSiP labeling is shown in the top view image. Marking includes both lot trace coding and pin 1 indicator

FAQ

Q: *What is a MicroSiP™?*

A: MicroSiP™ is a miniaturized System-in-Package (SiP) that integrates Silicon integrated circuits (IC's) with passive components in a BGA-format. Typically, the passives are arranged on the top, BGA balls are arrayed on the bottom and the integrated circuit PicoStar™ package is embedded in the laminate substrate. The MicroSiP can be either square or rectangular.

Q: *How is a MicroSiP™ different from a wafer-chip-scale-package (WCSP)?*

A: The MicroSiP package includes IC and passives while the WCSP is only an IC. For example, the TPS8267x packaged in MicroSiP integrates a DC-DC converter with inductor and input-output caps to provide a stand-alone power supply.

Q: *What is a PicoStar™?*

A: PicoStar™ is a die-sized package designed to be embedded in HDI laminate substrates.

Q: *Is this a lead-free (Pb-free) package?*

A: Yes, MicroSiP packages comply with lead-free environmental policies. The BGA bumps and the passive joints both are SAC305 (3%Ag, 0.5%Cu, balance Sn).

Q: *What land pad size should I design on my board for these packages?*

A: TI recommends that the board land closely match the land size on the SiP—300um diameter, non-solder mask defined. MicroSiP mounted to a 0.7mm thick PCB with OSP pads easily withstands 1000 cycles from -40 to 125°C (15 minute dwells).

Q: *Are there any special MicroSiP™ placement requirements?*

A: Movement of the MicroSiP from T&R to placement on the PCB can be treated as a similar sized BGA. The MicroSiP should be picked from the inductor top surface employing a ~1mm diameter nozzle/rubber tip (contact area between 0.5-1.0mm²).

Q: *Can I mount MicroSiP™ to the bottom of the PCB board?*

A: Yes you can. Ideally, the first and second reflow profiles are identical. The reflow profile should follow JEDEC standards for SMT of near-eutectic SnAgCu solder.

Q: *Can the MicroSiP™ withstand multiple reflows?*

A: Yes. Board level reliability testing was performed after 3 pass reflow (1 pass for assembly, then 2 additional passes). In general, assembly of the MicroSiP package can be treated exactly like a BGA.

Q: *What alignment accuracy is possible?*

A: TI recommends printing a lead-free solder paste as described in the board layout subsection before placement of the MicroSiP. Alignment accuracy depends on board pad tolerance and MicroSiP placement accuracy. MicroSiP packages self-align during reflow—final alignment accuracy is very likely better than placement accuracy.

Q: *How do board assembly yields of MicroSiP™ compare to a similar BGA?*

A: For a BGA of similar size and pitch, the assembly yield is identical to the MicroSiP package.

Rework

It is strongly recommended that the PCB with mounted SMT devices be baked prior to any rework so that absorbed moisture is removed (See J-STD-033 for more details). The rework process should be characterized such that the temperature of the MicroSiP™ package and surrounding PCB area are controlled. Either an attached thermocouple or an infrared camera works well to determine a repeatable heating profile.

Component removal process example:

- Align nozzle over part to be removed
- Maintain nozzle 1.27mm over the package
- Preheat board to 90°C, nozzle warming at 20% airflow/125°C
- Soak stage at 20% air flow/225°C/90 seconds
- Ramp stage at 25% air flow/335°C/30 seconds
- Reflow stage at 25% air flow/370°C/65 seconds
- Enable vacuum, lower nozzle, remove inductor from MicroSiP
- Discard Inductor
- Reposition nozzle, reheat at 25% air flow/370°C/20 seconds
- Enable vacuum, lower nozzle, remove MicroSiP from PCB
- Cool down stage at 40% air flow/25°C/50 seconds
- Turn off vacuum and remove part MicroSiP from nozzle
- Avoid handling damage of the removed unit
- Do not reuse/repair the removed unit

Component replacement process example:

- Apply solder paste to board using a micro-stencil
- Align MicroSiP over board land pads
- Place MicroSiP on board. Care should be taken to prevent overtravel during placement which may damage the package or vacuum tip
- Raise nozzle 1.27mm
- Preheat board to 90°C, nozzle warming at 20% air flow/125°C
- Soak stage at 20% air flow/225°C/90 seconds
- Ramp stage at 25% air flow/335°C/30 seconds
- Reflow stage at 25% air flow/370°C/65 seconds
- Cool down stage at 40% air flow/25°C/50 seconds

Air-Vac Engineering:

Air-Vac Engineering (www.air-vac-eng.com) has established heating profiles and tooling recommendations for their Hot Gas (convection) rework equipment, DRS-24NC.

Nozzle NMX188DVG

- 0.18" Exhaust opening
- VTMX020-35 Vacuum Tip

Comparable hot gas (convection heating) rework equipment from other vendors can also be used successfully.

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