## Calculation of UCD3138 Slope Compensation for PCM

Step 1. Take CLAO output which is voltage loop output every half switching cycle;
Step2: CLAO is the starting point of the slope ramp, every 32 ns , CLAO is reduced by the DAC_STEP;
Step3: The substraction is fed into FE2_DAC;
Step4: The DAC output is a analog voltage, which is compared with input current signal;
The below is blocking diagram to explain the sequence.

Diagram of Slope Compensation


For example: how to calculate the slope rate in 1us for DAC_STEP $=48000$ :
((1000ns/32ns) *48000 /1024 *0.0976mV = 142mv/us
DAC_VALUE

| $13\|12\| 11\|10\| 9\|8\| 7\|6\| 5 \mid 4$ | $3\|2\| 1 \mid 0$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DAC Value |  | Dither |



## DAC_STEP

Where 1024 is fractional part of DAC_STEP, and 0.0976 mv is DAC LSB

Use inverse equation, DAC_STEP can be calculated for a given slope compensation.
For example, calculate the DAC_STEP for SLOPE $=100 \mathrm{mV} / \mathrm{us}$
$(100(\mathrm{mv}) / 0.097(\mathrm{mv})) * 1024 /(1000 \mathrm{~ns} / 32 \mathrm{~ns})=33781$

