Application Report
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How to Design an LED Driver Using the TPS92510

Joel Brassfield *PS-Lighting Power*

ABSTRACT

This design example consists of a single string of ten LEDs driven with 1-A forward current. This design example is a supplement to the TPS92510 data sheet and provides step-by-step instructions for optimizing an LED driver design. In particular, detailed attention is given to compensating and measuring the feedback loop, implementing the thermal foldback protection, and designing the printed-circuit board layout. Graphs are provided showing the design example test data.

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The following system parameters must be known in order to start the design process.

Input Voltage Range	48 V ± 10%
Maximum Output Voltage	34 V
LED Current	1 A
LED Current Ripple	3% of I_{LED}
Start Input Voltage (rising V_{IN})	40 V
Stop Input Voltage (falling V_{IN})	38 V
Cross-Over Frequency	20 kHz

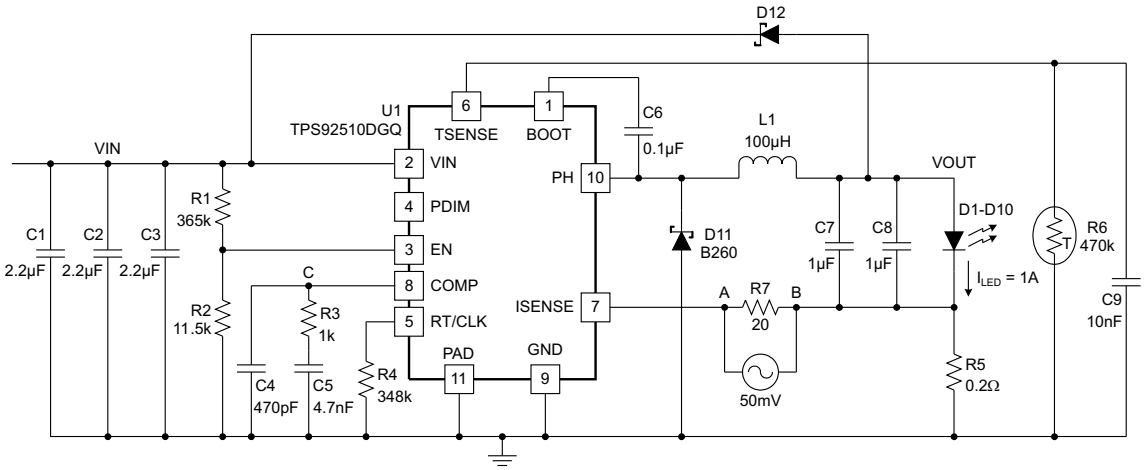


Figure 1. TPS92510 Design Example Schematic

1 LED Current Setpoint

The light-emitting diode (LED) current is programmed with resistor R5. The current-sense resistor value and power dissipation are shown in Equation 1 and Equation 2. The current-sense resistor is part of the power supply, not the load. When making efficiency measurements, the output voltage is sensed directly across the LED string, not from V_{OUT} to GND. The current-sense resistor value in this example is 0.2 Ω and dissipates 200 mW. As the inductor ripple current increases, the power dissipation of the current-sense resistor exceeds the result of Equation 1. For a more accurate calculation, multiply the current-sense resistor value by the RMS inductor current squared $(I_{L\_RMS^2})$, which is shown in the inductor section Section 5.

$$R5 = \frac{V_{REF}}{I_{LED}} \quad (1)$$

$$P_{DIS} = \frac{V_{REF}^2}{R5} \quad (2)$$

2 Output Voltage

The output voltage of the converter is approximated as shown in Equation 3.

$$V_{OUT} = V_{LED} \times n + V_{REF} \quad (3)$$

Where:

V_{LED} = the forward voltage drop of a single LED
n = number of LEDs
V_{REF} = 0.2 V, the TPS92510 reference voltage

Using Equation 3, the approximate output voltage is (3.323 V × 10) + 0.2 V = 33.43 V.

3 Enable Undervoltage Lockout

The TPS92510 can be programmed to enable at a user-defined input voltage threshold, V_{START}. In addition, the desired input voltage hysteresis ($V_{START} - V_{STOP}$) can be selected. Once these values are known, the required resistors R1 and R2 can be calculated as shown in Equation 4 and Equation 5. For this example, the input voltage can be as low as 43 V, so the V_{START} threshold must be lower than this voltage to ensure operation. The V_{STOP} threshold must be at least V_{OUT} + 2.1 V. This ensures that the UVLO hysteresis threshold controls the converter turnoff, rather than the BOOT UVLO threshold. For this example, a 40-V start threshold and a 38-V stop threshold are chosen.

$$R1 = \frac{V_{HYS} \times (V_{EN} - I1 \times R_{ESD}) - I_{HYS} \times R_{ESD} \times V_{START}}{I_{HYS} \times V_{EN}} \quad (4)$$

$$R2 = \frac{R1 \times [V_{EN} - R_{ESD} \times (I1 + I_{HYS})]}{V_{STOP} - V_{EN} + (I1 + I_{HYS}) \times (R1 + R_{ESD})} \quad (5)$$

Where:

$V_{HYS} = V_{START} - V_{STOP}$
R_{ESD} = 10kΩ

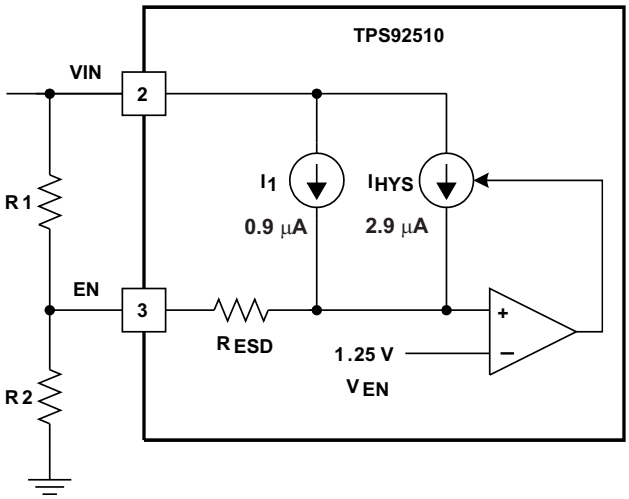


Figure 2. Adjustable UVLO

Using nearest standard values, R1 is chosen to be 681 kΩ, and R2 is chosen to be 22.1 kΩ. Once the values are chosen, calculate the worst-case start and stop thresholds, taking into account the tolerance of each variable to ensure that the UVLO feature functions as intended. For convenience, the start and stop thresholds are derived in Equation 6 and Equation 7 showing their dependent variables. The minimum and maximum values for V_{ENABLE} are given in the electrical specification table.

$$V_{START} = \frac{R1 \times V_{EN} + V_{EN} \times R2 - R1 \times I1 \times R2 - R1 \times I1 \times R_{ESD} - I1 \times R_{ESD} \times R2}{R2} \quad (6)$$

$$V_{STOP} = \frac{R1 \times V_{EN} + V_{EN} \times R2 - R1 \times I1 \times R2 - R1 \times I_{HYS} \times R2 - R1 \times I1 \times R_{ESD} - I1 \times R_{ESD} \times R2 - R1 \times I_{HYS} \times R_{ESD} - R_{ESD} \times R2 \times I_{HYS}}{R2} \quad (7)$$

4 Selecting the Switching Frequency

When choosing the switching frequency for the regulator, a trade-off is made between small solution size and higher performance. In this example, the system performance is optimized to yield a higher efficacy (lumens/watt) at the expense of a physically larger inductor. A switching frequency of 350 kHz is used. Use Equation 8 to determine the RT resistance, where F_{SW} is in units of kHz. In this example, a 348-kΩ resistor is chosen.

$$R_T = \frac{206033}{F_{SW}^{1.0888}} \quad (8)$$

5 Selecting the Buck Inductor

The value of the buck inductor impacts the peak-to-peak, ripple-current amplitude. The peak-to-peak ripple current is part of the PWM control system and must typically be greater than 150 mA for dependable operation. Choosing an inductor ripple current on the larger side is better in a wide-input application. This allows the control system to have an adequate current signal even at the lowest input voltage. Equation 9 calculates the maximum value for the buck inductance, given a minimum ripple current of 150 mA. Enter the lowest input voltage and the highest output voltage to yield the maximum inductance value.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{150\ mA \times V_{IN} \times F_{SW}} \quad (9)$$

In our example, a minimum input voltage of 43 V, a maximum output voltage of 34 V, and a switching frequency of 350 kHz yield a maximum inductance value of 135 µH. Therefore, an inductor value of 100 µH with 200-mΩ dc resistance was chosen for this design. At the typical input voltage, Equation 10 yields a peak-to-peak inductor ripple current of 290 mA.

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times L} \quad (10)$$

The inductor RMS current and saturation current ratings must be greater than those seen in the application. This ensures that the inductor does not overheat or saturate. During power-up, transient conditions, or fault conditions, the inductor current can exceed its normal operating current. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the converter current limit. This is not always possible due to application size limitations. The peak inductor current and the RMS current equations are shown in Equation 11 and Equation 12.

$$I_{L\_PEAK} = I_{LED} + \frac{I_{RIPPLE}}{2} \quad (11)$$

$$I_{L\_RMS} = \sqrt{I_{LED}^2 + \frac{I_{RIPPLE}^2}{12}} \quad (12)$$

6 Input Capacitor

The TPS92510 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 2-µF effective capacitance. Ceramic capacitance tends to decrease as the applied dc voltage increases. This depreciation must be accounted for to ensure that the minimum input capacitance is satisfied. In some applications, additional electrolytic capacitance is needed to provide bulk energy storage. The input capacitor voltage rating must be greater than the maximum input voltage and have a ripple current rating greater than the maximum input current ripple of the converter. The RMS input ripple current is calculated in Equation 13, where D is the duty cycle (output voltage divided by input voltage). Additionally, the maximum RMS input ripple current can be calculated easily by substituting the minimum input voltage of the application.

$$I_{IN\_RMS} = I_{LED} \times \sqrt{D \times (1 - D)} \quad (13)$$

The input capacitance is inversely proportional to the input ripple voltage of the converter. The peak-to-peak, input ripple voltage can be calculated as shown in Equation 14. Additionally, this equation can be used to solve for the required input capacitance to keep the input ripple voltage to a defined limit. For example, it is advisable to keep the input ripple voltage to 1% of the dc input voltage. This small amount of input voltage ripple keeps the ripple current through any bulk electrolytic capacitors to a reasonable level, which reduces their temperature and improves their lifetime.

$$\Delta V_{IN} = \frac{I_{LED} \times D \times (1 - D)}{C_{IN} \times F_{SW}} \quad (14)$$

For this design, three 2.2-µF, 100-V ceramic capacitors are placed in parallel. At 53-V input, the capacitance has dropped by approximately 60%, leaving 2.64 µF of effective capacitance, which meets the minimum requirement. For this design, with the typical 48-V input and 33.4-V output operating conditions, and an effective input capacitance of approximately 3 µF, the RMS input current is 460 mA, and the input ripple voltage is approximately 200 mV_{PK-PK}.

7 BOOT Capacitor

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. Use a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10-V or higher voltage rating.

8 Output Capacitor

During start-up, the TPS92510 uses the discharged output capacitor as a charging path for the BOOT capacitor. In order to ensure that the BOOT capacitor charges and that the converter begins switching, the value of the output capacitor must be 10 times larger than the BOOT capacitor. The BOOT capacitor is 0.1 µF, and so the minimum output capacitor must be 1 µF. If the output capacitor is chosen to be a smaller value or none at all, then the BOOT capacitor can charge through the LED string itself. However, this method of charging the BOOT capacitor generally raises the input voltage UVLO threshold to V_{OUT} + V_{BOOT_UVLO}.

The output capacitor also reduces the high-frequency ripple current through the LED string. Various guidelines disclose how much high-frequency ripple current is acceptable in the LED string. Excessive ripple current in the LED string increases the RMS current in the LED string, and therefore the LED temperature also increases. For this design, the LED ripple current is limited to 3% of the LED current, or 30 mA_{PK-PK}. First, calculate the total dynamic resistance of the LED string using the LED manufacturer's data sheet. Second, calculate the required impedance of the output capacitor given the acceptable peak-to-peak ripple current through the LED string, ΔI_{LED}. I_{RIPPLE} is the peak-to-peak inductor ripple current as calculated previously in Section 5. Third, calculate the minimum, effective, output capacitance required. Finally, increase the output capacitance appropriately due to the derating effect of applied dc voltage.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times n \quad (15)$$

$$Z_{COUT} = \frac{R_{LED} \times \Delta I_{LED}}{I_{RIPPLE} - \Delta I_{LED}} \quad (16)$$

$$C_{OUT} = \frac{1}{2 \times \pi \times F_{SW} \times Z_{COUT}} \quad (17)$$

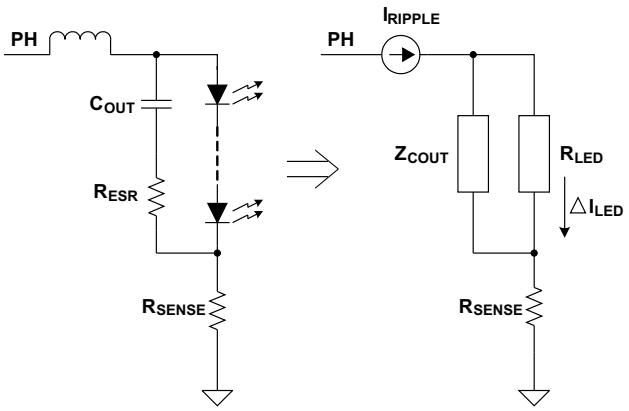


Figure 3. Choosing the Output Capacitor

In this design example, the LED string dynamic resistance is 3.276 Ω, the peak-to-peak inductor ripple current is 0.29 A, and Z_{COUT} equals 378 mΩ. Therefore, the minimum output capacitance must be 1.2 µF. Finally, a typical 1-µF, 100-V ceramic capacitor loses 40% of its initial capacitance with 33 V applied. So, C_{OUT} was chosen as two 1-µF, 100-V capacitors in order to ensure a 30-mA_{PK-PK} ripple in the LED string.

9 Rectifier Diode Power Dissipation

The rectifier diode conducts the inductor current only during the high-side MOSFET off-time. The rectifier diode must have a reverse voltage rating greater than or equal to the maximum input voltage and a current rating greater than the peak inductor current. The package size chosen for the rectifier diode must be capable of handling the power dissipation of the diode. The diode power dissipation is equal to the average diode current times the diode forward voltage. For this design, a 2-A, 60-V Schottky diode was used. Equation 18 shows approximately 160 mW in the diode. At higher switching frequencies, the junction capacitance of the diode and reverse recovery time add to the diode power dissipation.

$$P_{DIODE} = I_{D\_AVG} \times V_F \tag{18}$$

Where:

$$I_{D\_AVG} = \left(1 - \left(\frac{V_{OUT}}{V_{IN}}\right)\right) \times I_{LED} \tag{19}$$

10 Loop Compensation

This design can be compensated by using a Type-II error amplifier network in order to achieve a higher crossover frequency. The design example is compensated according to the guidelines described in the data sheet. The typical dc gain of the power stage is calculated first using Equation 20. To calculate the power stage dc gain, calculate f_M and G_V as shown in Equation 21 and Equation 22.

$$G_{DC} = \frac{167 \times V_{IN} \times f_M \times R_{SENSE}}{17 \times V_{IN} \times f_M + 1000000\left[R_{DCR} + R_{SENSE} + R_{LED} - f_M \times V_{IN} \times G_v \times \left(R_{SENSE} + R_{LED}\right)\right]} \tag{20}$$

$$f_M = \frac{117 \times 10^3 \times L \times F_{SW}}{V_{IN} - V_{OUT} + 3 \times F_{SW} \times L} \tag{21}$$

$$G_V = \frac{V_{OUT}}{117.2 \times 10^3 \times L \times V_{IN} \times F_{SW}} \tag{22}$$

For this example, f_M is 32.25 × 10^3 and G_V is 169.8 × 10^{-9}. The last unknown is the LED dynamic resistance. Sometimes, this value can be derived from the LED manufacturer's data sheet. This example uses OSRAM Golden DRAGON LEDs. The dynamic resistance of a single LED was determined to be 0.327 Ω. The design includes 10 LEDs, and therefore the total dynamic resistance of the LED string is 3.27 Ω. With these values, the dc gain of the power stage is calculated to be 1.791, or 5.06 dB. Once the dc gain of the power stage is determined, the error amplifier compensation values can be calculated.

$$C5 = \frac{gm_{EA} \times G_{DC}}{2 \times \pi \times F_{CO}} = \frac{310\left(\frac{\mu A}{V}\right) \times 1.791}{2 \times \pi \times 20\ kHz} = 4.42\ nF \quad (23)$$

$$R3 = \frac{1}{2 \times \pi \times K \times F_{co} \times C5} \quad (24)$$

The nearest standard value for C5 was chosen as 4.7 nF. C4 is chosen as one-tenth of C5, which is 470pF. The value for R3 is chosen based on Equation 24, where K is a multiplier between 1.5 and 4, and F_{co} is the desired cross-over frequency (20 kHz in this example). The range of the K-multiplier is a guideline and gives the value of R3 some flexibility, which tunes the system's phase margin near the crossover frequency. The K-multiplier is bound to a minimum and maximum value in order to yield the most benefit from the Type-II compensation network. For example, using a K-multiplier greater than 4 yields an R3 value so small that its effect on the phase margin becomes insignificant, and the error amplifier performance begins to approach a Type-I compensation network. Alternatively, using a K-multiplier less than 1.5 places the error amplifier zero frequency nearer to the crossover frequency and may not yield enough phase margin. Design the error amplifier compensation with the K-multiplier within the suggested range, and then measure the actual system and make changes to the R3 value accordingly, in order to achieve the desired phase margin. In this example, a K-value of 2 was initially chosen resulting in an R3 value of 846 Ω. Then, measurements were made and the R3 value was adjusted to 1 kΩ in order to achieve the desired phase margin.

Equation 25 shows the control-to-output transfer function of the power stage. Using a computer-aided math program, such as Mathcad™, the control-to-output gain can be plotted versus frequency.

$$G_{C20}(s) = \frac{167 \times 10^{-6} \times f_M \times R_{SENSE} \times Gi(s)}{1 + 17 \times 10^{-6} \times f_M \times Gi(s) \times He(s) - f_M \times Gv \times Gi(s) \times Z_{OUT}(s)} \quad (25)$$

Where:

$$Gi(s) = \frac{V_{IN}}{s \times L + R_{DCR} + R_{SENSE} + \frac{\left(R_{ESR} + \frac{1}{s \times C_{out}}\right) \times R_{LED}}{R_{ESR} + \frac{1}{s \times C_{OUT}} + R_{LED}}} \quad (26)$$

$$He(s) = 1 + \frac{s}{-2 \times F_{SW}} + \frac{s^2}{(\pi \times F_{SW})^2} \quad (27)$$

$$Z_{OUT}(s) = \frac{\left(R_{ESR} + \frac{1}{s \times C_{OUT}}\right) \times R_{LED}}{R_{ESR} + \frac{1}{s \times C_{OUT}} + R_{LED}} + R_{SENSE} \quad (28)$$

Figure 4 and Figure 5 show the calculated and measured control-to-output gain and phase responses. The control-to-output response shows a low dc gain, as calculated by Equation 20. It also shows the phase transitioning from 0 degrees to –180 degrees.

Figure 6 and Figure 7 show the calculated and measured compensated error amplifier gain and phase responses.

Both the calculated and measured responses correlate very well. The crossover frequency is approximately 20 kHz and the phase margin is approximately 75 degrees. Near the switching frequency, the measured data shows signs of aliasing, and the response does not correlate with the calculated model. This is an artifact of the measurement system interacting with the power stage. Below 100 kHz, the calculated and measured data correlate well.

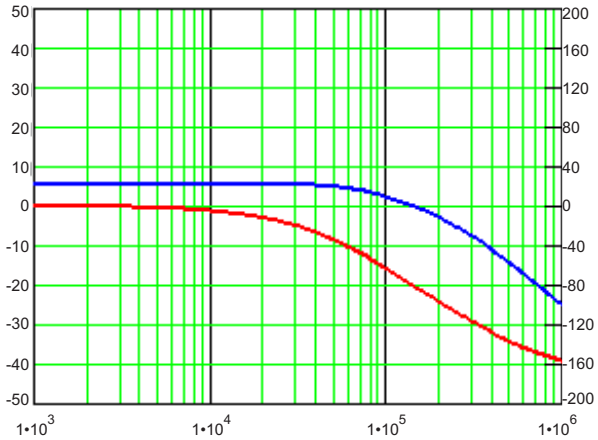


Figure 4. Calculated Control-to-Output Gain and Phase

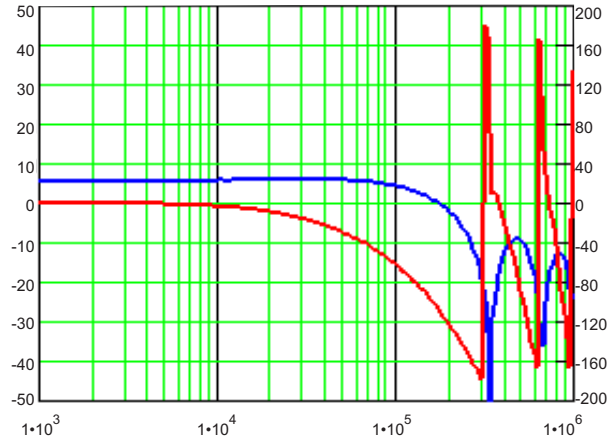


Figure 5. Measured Control-to-Output Gain and Phase

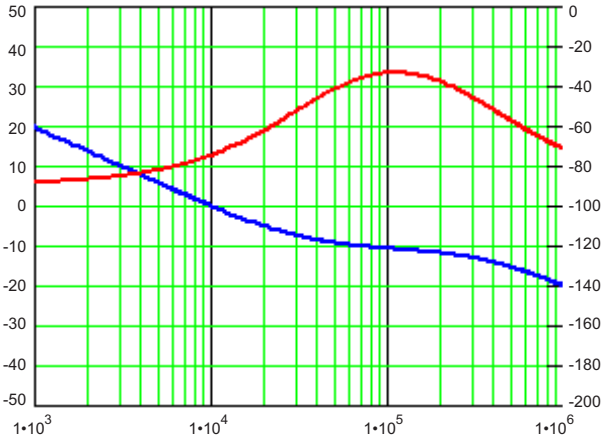


Figure 6. Calculated Error Amplifier Gain and Phase

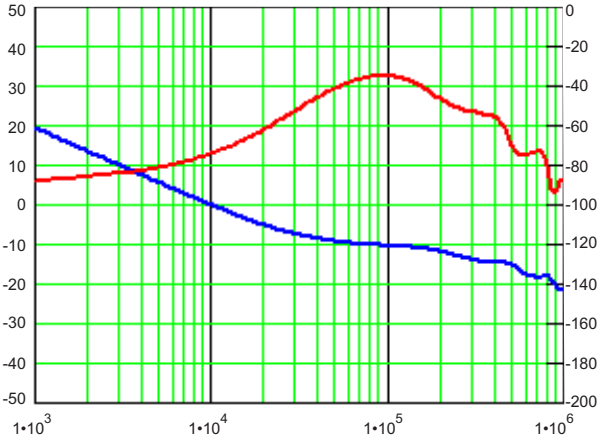


Figure 7. Measured Error Amplifier Gain and Phase

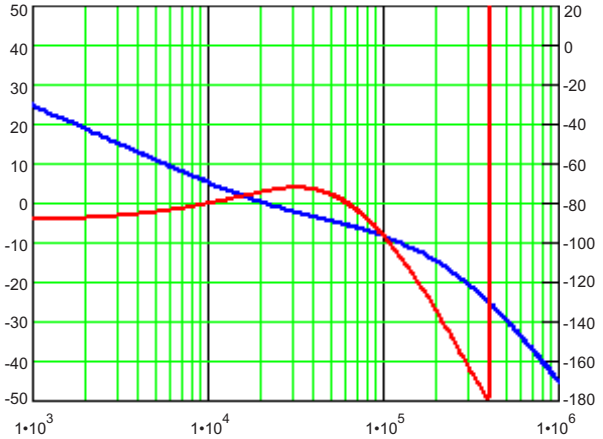


Figure 8. Calculated Complete Loop Gain and Phase

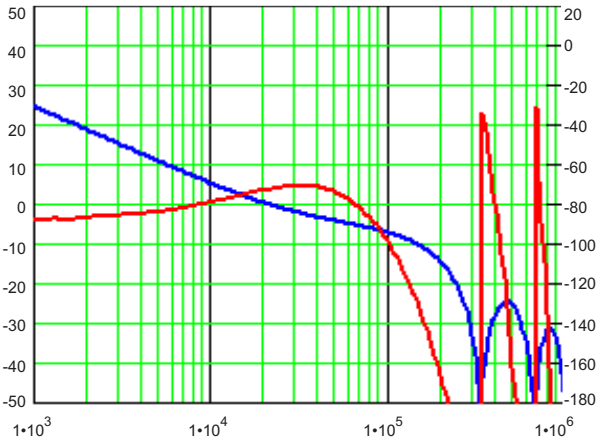


Figure 9. Measured Complete Loop Gain and Phase

11 Measuring Loop Gain and Phase

Figure 1 shows a schematic detailing the proper way to inject an ac signal and make the system gain and phase measurements. R7 is inserted in order to inject the measurement signal into the feedback system. Points A, B, and C are used to measure the various sections of the loop. Plotting B/A yields the response of the complete loop. Plotting B/C yields the control-to-output response. Plotting C/A yields the response of the compensated error amplifier.

12 Thermal Foldback Protection

The TPS92510 implements a thermal foldback protection feature to limit the LED temperature. The LED temperature is closely monitored with an NTC (negative temperature coefficient) resistor connected to the TSENSE pin of the TPS92510, which outputs 100 µA. As the LED temperature increases, the NTC resistance decreases, and the voltage across the NTC also decreases. Internally, the TSENSE voltage is compared to a 2-V ramp waveform. If the TSENSE voltage is less than 2 V, the converter begins to pulse width modulate at a fixed 6-kHz rate. As the TSENSE voltage further decreases, the duty cycle of the converter further decreases, and this reduces the delivered power to the LED load, which reduces its temperature. The NTC resistance and the developed TSENSE voltage change at a rate equal to the LED heat-sink thermal time constant, forming a low-gain, inherently stable, thermal foldback system.

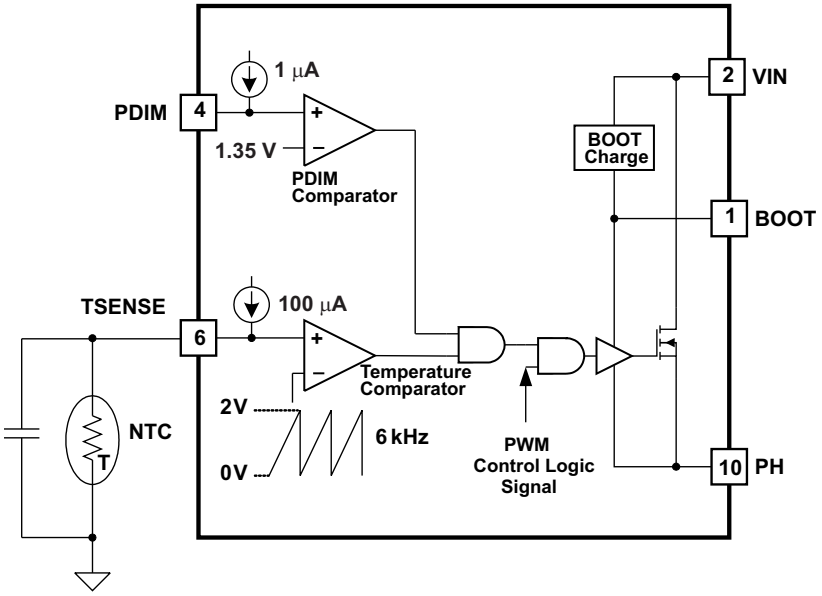


Figure 10. Thermal Foldback Functional Block Diagram

Typically, the value of the NTC resistor is chosen to reduce the output power by a known percentage at a determined maximum LED temperature. For example, without thermal foldback enabled, at 95°C ambient temperature, the measured LED temperature of this application is 125°C. The power dissipated in the LED load causes the LED temperature to raise 30°C above the ambient temperature. At 95°C ambient, limiting the LED temperature to 110ºC maximum is desirable, in other words, a 15°C rise above ambient temperature. To do this, a first approximation reduces the power delivered to the load by 50%. Because temperature is proportional to power dissipation, this reduces the 30°C rise to 15°C rise above ambient temperature. Therefore, the NTC resistance value is chosen such that at (95°C + 15°C) = 110°C ambient temperature, its resistance causes a 50% thermal foldback duty cycle, as shown in Equation 29.

$$R_{NTC} = \frac{2\ V \times DC}{100\ \mu A} = \frac{2\ V \times 0.5}{100\ \mu A} = 10\ k\Omega \quad (29)$$

For this example, a 470-kΩ NTC was chosen. At 110°C, the NTC resistance is approximately 13 kΩ. This creates a TSENSE voltage of 1.3 V and a thermal foldback duty cycle of 65%. At first glance, this resulting duty cycle seems to be too large to reduce the temperature to the desired target. However, a secondary effect is occurring. As the LED current is reduced due to the thermal foldback duty cycle, the LED output voltage also is reducing, and this reduces the power dissipated in the LED load as well. The combination of these two functions results in the desired temperature reduction

In some applications, the output voltage dependency with reduced LED current may not be so great and therefore cannot be relied on to achieve the reduced temperature. In these cases, use a lower value NTC resistor (sometimes in series with a lower value fixed resistor) to achieve the temperature reduction. This technique can be used to create an NTC value tailored for the specific application. For example, NTC resistors are offered in standard values (100k, 220k, 330k, 470k, etc). If a 330k NTC does not provide enough thermal foldback, and a 220k NTC provides too much thermal foldback, then adding some fixed

resistance in series with the 220k NTC can yield the desired performance. Providing a guideline of how much fixed resistance to add is difficult, because each application is different. Therefore, thermal testing must be performed on the final assembled product to validate if the desired performance is achieved. Then, changes can be made to the NTC value and the fixed resistance until the desired thermal performance is achieved.

Finally, locating the NTC as close as possible to the LED for the most accurate thermal sensing is extremely important. Any distance between these two components creates a thermal delta which reduces the accuracy of the sensed temperature.

13 PCB Layout

Figure 11 gives an example of a typical layout for the TPS92510. Creating a large GND pour under the integrated circuit (IC) for good electrical and thermal performance is important. The GND pin of the device must connect to the GND pour directly underneath the IC. Thermal vias can be used to connect the topside GND pour to additional printed-circuit board (PCB) layers for heat spreading. Keeping the thermal vias outside of the device thermal pad opening to prevent topside solder from wicking to the backside of the PCB is good practice. The input capacitors must be located as close as possible to the VIN pin and the GND pour. The compensation components must be located as close as possible to the COMP and GND pins in order to minimize noise sensitivity. The PH pin must be kept as small and as short as possible, because this is the noisiest node of the circuit. The VSENSE node must be kept as short as possible and shielded from noise. The RT/CLK pin is very sensitive and must be kept as short as possible.

In higher current applications, routing the load current of the current-sense resistor to the junction of the input capacitor and rectifier diode GND node may be necessary. This steers the high current away from the sensitive RT/CLK GND connection.

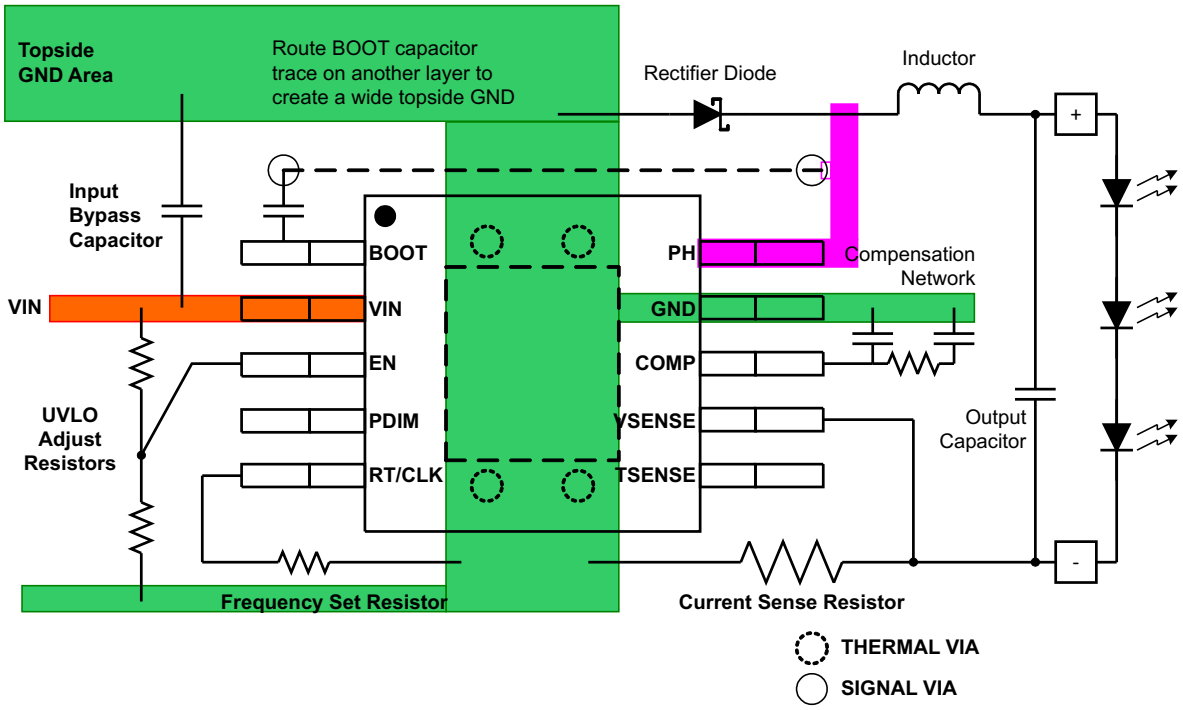


Figure 11. PCB Layout Example

14 Bill of Materials

Reference Designator	Vendor	Part Number	Value	Package
U1	TI	TPS92510DGQ	TPS92510DGQ	10-pin MSOP
D1-D10	Osram	LW W5AM	Neutral White	Golden Dragon Plus
D11, D12	Diode's Inc	B260-13-F	B260	SMA
L1	Würth	74477020	100µH	12 x 12 x 8mm
C1,C2,C3	TDK	C3225X7R2A225K	2.2µF	1210
C4	TDK	C1608X7R1H561J	560pF	0603
C5	TDK	C1608X7R1H472J	4.7nF	0603
C6	TDK	C1608X7R1C104J	0.1µF	0603
C7,C8	TDK	C3225X7R2A105K	1µF	1210
C9	TDK	C1608X7R1C103J	10nF	0603
R1	KOA	RK73H1JT_3653F	365kΩ	0603
R2	KOA	RK73H1JT_1152F	11.5kΩ	0603
R3	KOA	RK73H1JT_1001F	1kΩ	0603
R4	KOA	RK73H1JT_3483F	348kΩ	0603
R5	KOA	SR732BTR200F	0.2Ω	1206
R6	TDK	NTCG164QH474J	470kΩ	0603
R7	KOA	RK73H1JT_20R0F	20Ω	0603

15 Application Data

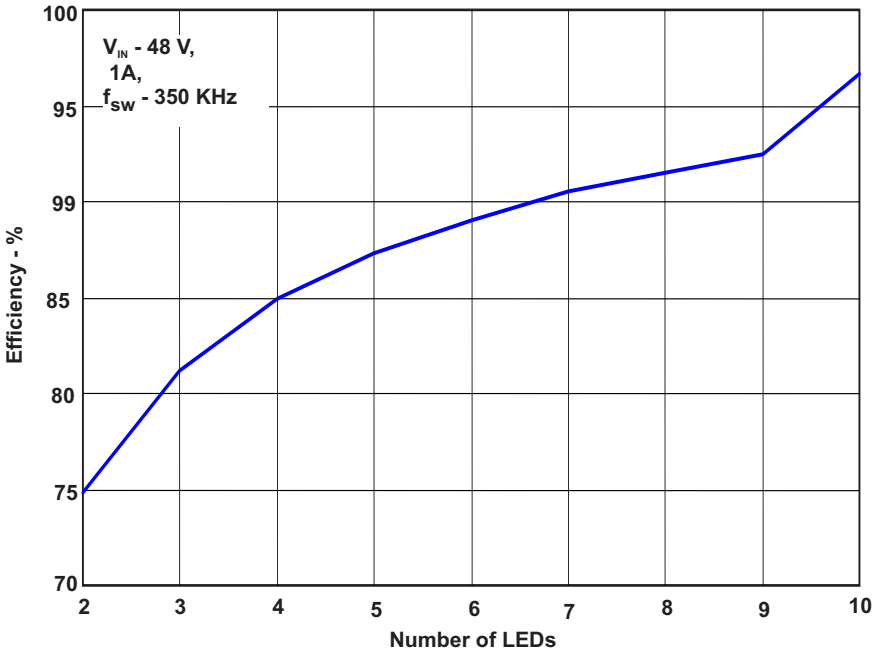
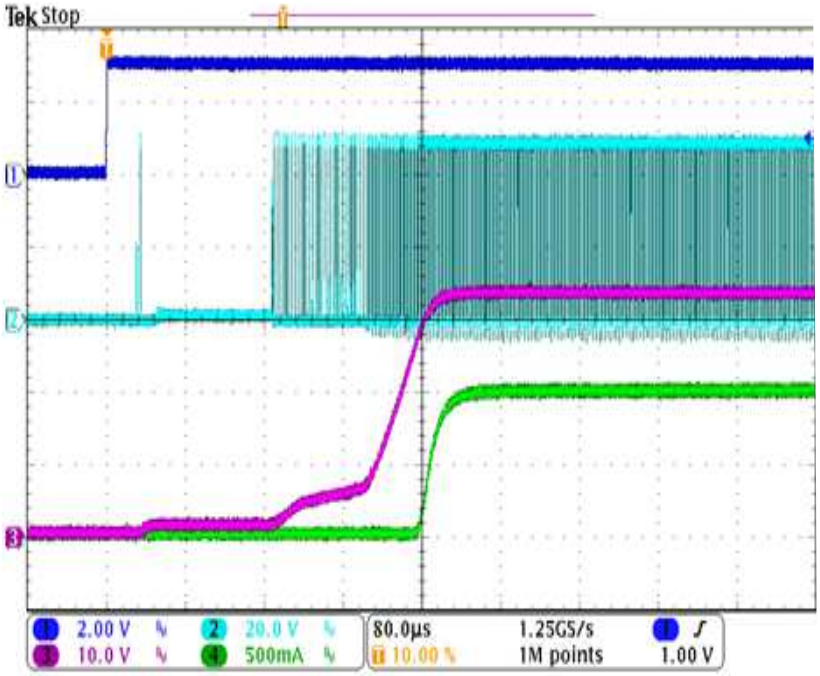
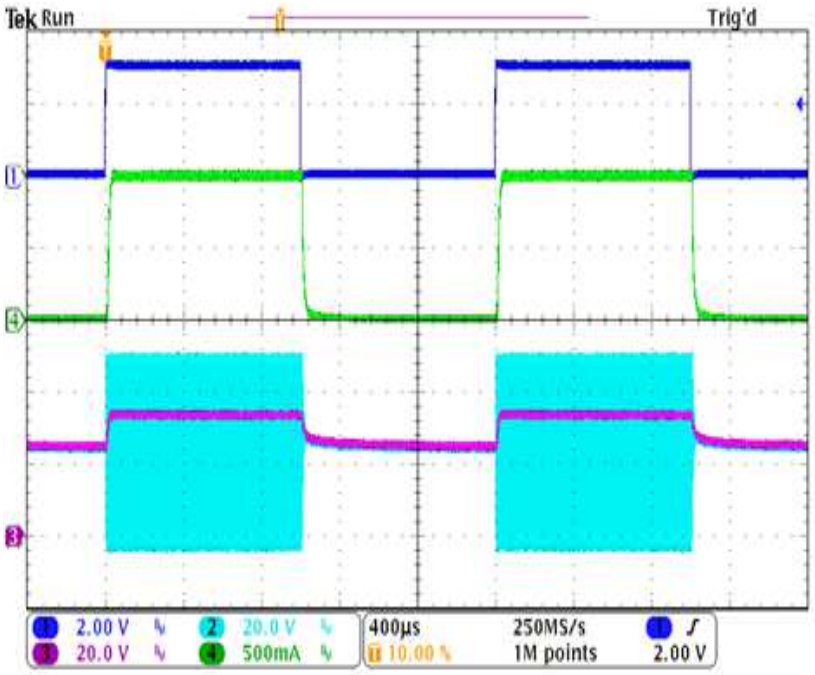


Figure 12. Efficiency vs the Number of LEDs



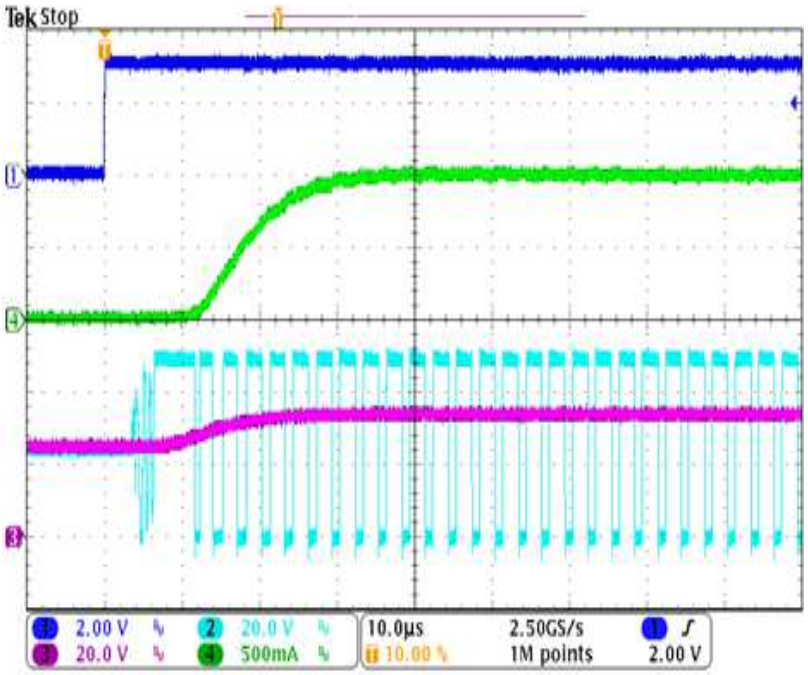
CH1: Enable, CH2: PH, CH3: Output Voltage, CH4: LED Current

Figure 13. Start-Up via Enable



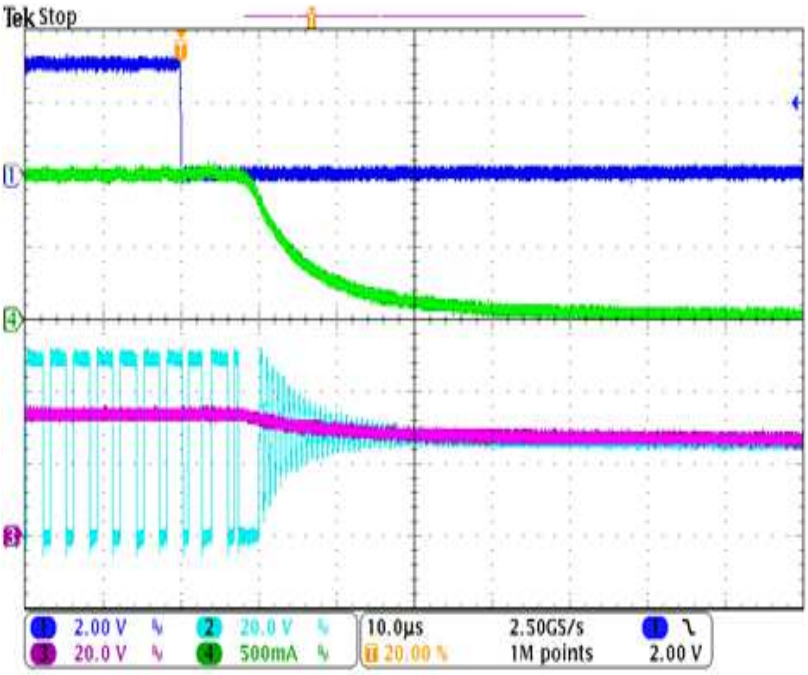
CH1: PDIM, CH2: PH, CH3: Output Voltage, CH4: LED Current

Figure 14. PWM Dimming Waveforms: 500Hz @ 50% Duty Cycle



CH1: PDIM, CH2: PH, CH3: Output Voltage, CH4: LED Current

Figure 15. Rising PWM Dimming Waveforms



CH1: PDIM, CH2: PH, CH3: Output Voltage, CH4: LED Current

Figure 16. Falling PWM Dimming Waveforms

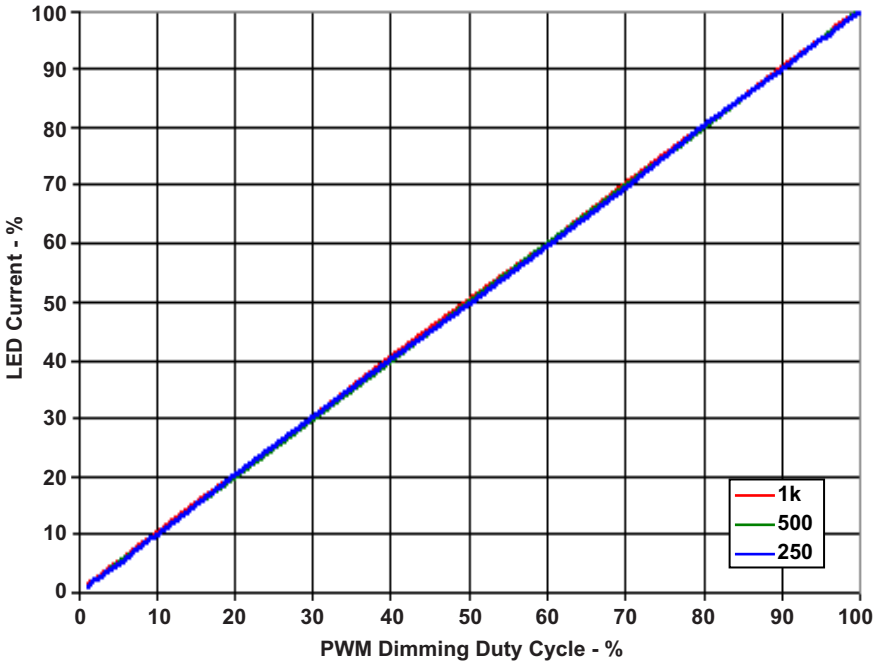


Figure 17. PWM Dimming Linearity at Various PDIM Frequencies

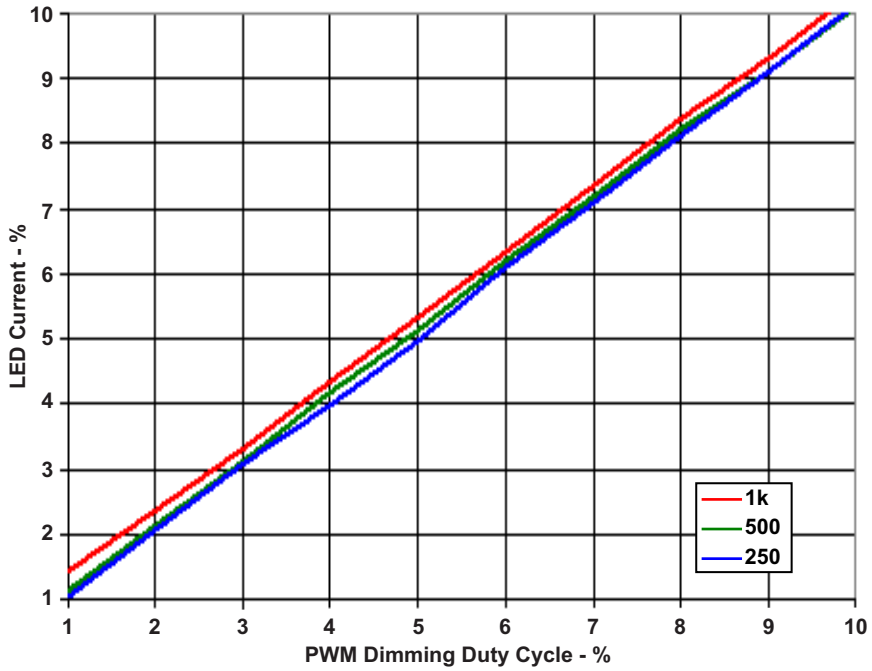


Figure 18. PWM Dimming Linearity at Various PDIM Frequencies – Low Duty Cycle

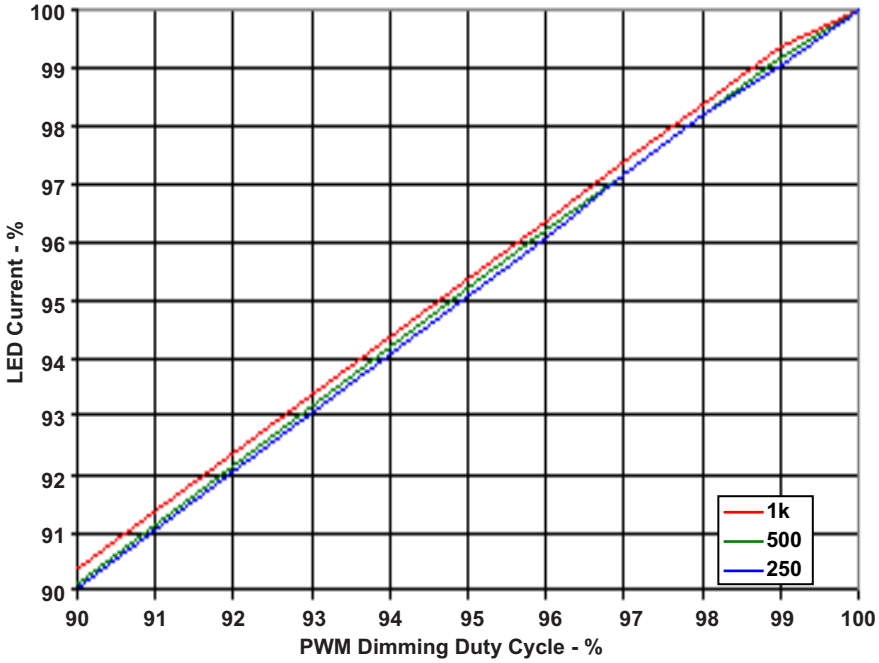
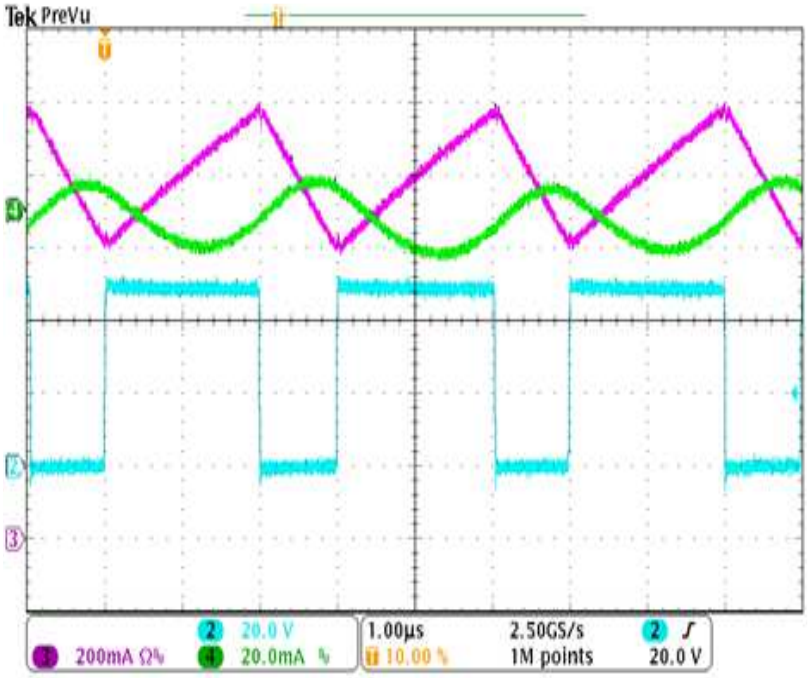
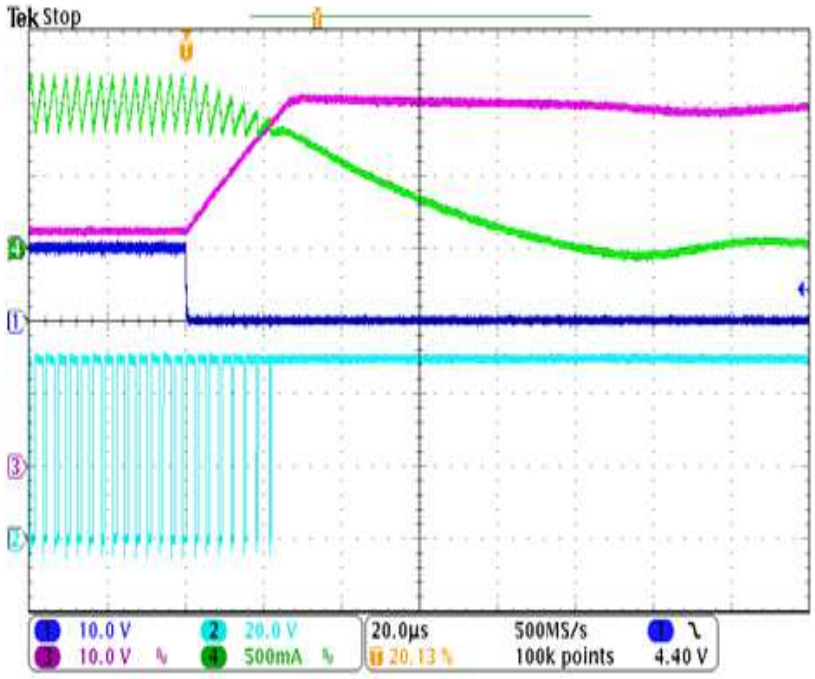


Figure 19. PWM Dimming Linearity at Various PDIM Frequencies – High Duty Cycle



CH2: PH, CH3: Inductor Current, CH4: LED Current

Figure 20. Inductor and LED Ripple Current



CH1: Open LED control signal, CH2: PH, CH3: Inductor Current, CH4: Output Voltage

Figure 21. Open LED Fault Waveform – Protection Diode From V_{OUT} to V_{IN}

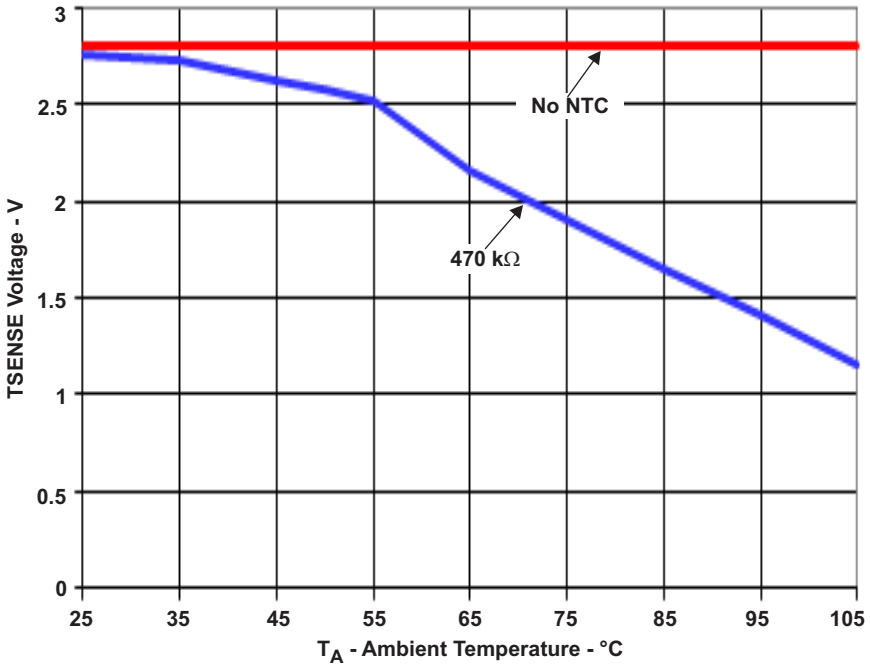


Figure 22. TSENSE Voltage vs Ambient Temperature With and Without Thermal Foldback

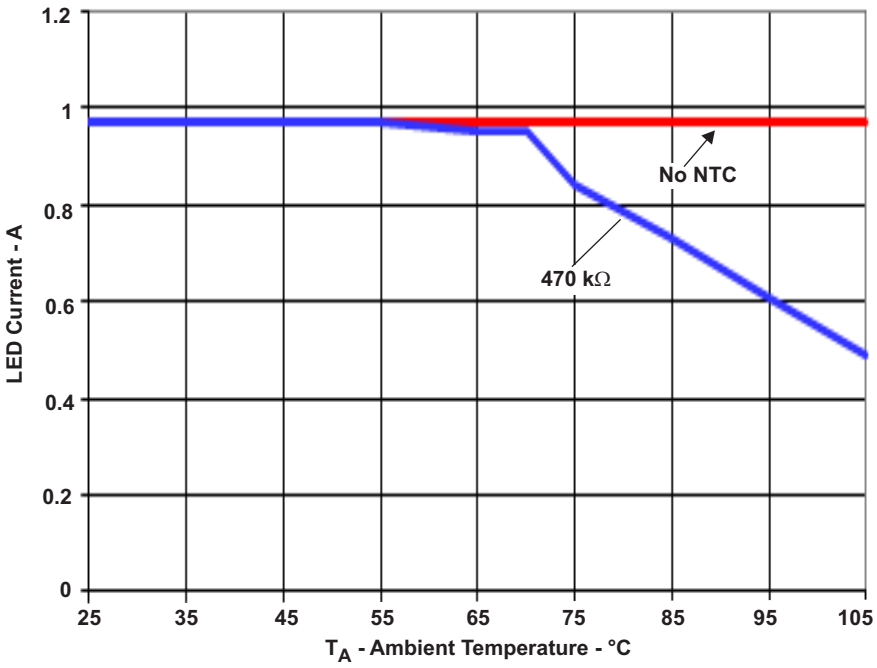


Figure 23. LED Current vs Ambient Temperature With and Without Thermal Foldback

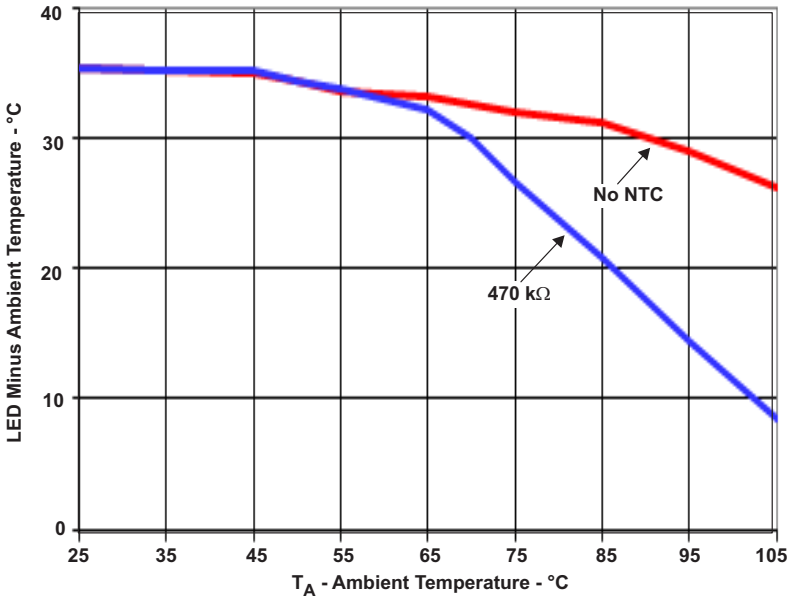


Figure 24. LED Temperature Rise vs Ambient Temperature With and Without Thermal Foldback

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