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The Right-Half-Plane Zero — A Simplified Explanation

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The Right-Half-Plane Zero — A Simplified Explanation

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In small signal loop analysis, poles and zeros are normally located in the left half of the complex s-plane. The Bode plot of a conventional or left-half-plane zero has the gain magnitude rising at 20 dB/decade above the zero frequency with an associated phase lead of 90°. This is the exact opposite of a conventional pole, whose gain magnitude *decreases* with frequency and the phase *lags* by 90°. Zeros are often introduced in loop compensation networks to cancel an existing pole at the same frequency; likewise poles are introduced to cancel existing zeros in order to maintain total phase lag around the loop less than 180° with adequate phase margin.

The right-half-plane (RHP) zero has the same 20 dB/decade rising gain magnitude as a conventional zero, but with 90° phase *lag* instead of lead. This characteristic is difficult if not impossible to compensate. The designer is usually forced to roll off the loop gain at a relatively low frequency. The crossover frequency may be a decade or more below what it otherwise could be, resulting in severe impairment of dynamic response.

The RHP zero never occurs in circuits of the buck family. It is encountered only in flyback, boost and Ćuk circuits, and then only when these circuits are operated in the continuous inductor current mode.

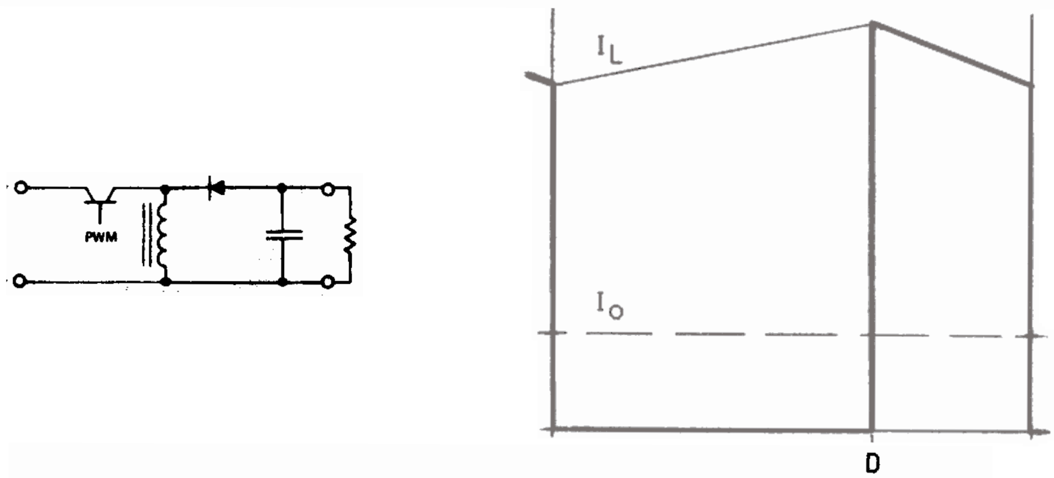


Figure 1 -- Flyback Circuit, Continuous Inductor Current Mode

Figure 1 shows the basic flyback circuit operating in the continuous mode with its current waveforms. In flyback as well as boost circuits, the diode is the output element. All current to the output filter capacitor and load must flow through the diode, so the steady-state DC load current must equal the average diode current. As shown in the Fig. 1 waveforms, the inductor current equals the peak diode current, and it flows through the diode only during the "off" or free-wheeling portion of each cycle. The average diode current (and load current) therefore equals the average inductor current, I_L, times (1-D), where D is the duty ratio (often called duty cycle).

If D is modulated by a small AC signal, $\hat{d}$, whose frequency is much smaller than the switching frequency, this will cause small changes in D from one switching cycle to the next. Figure 2 shows the effects of a small increase in duty ratio (during the positive half-cycle of the applied signal).

The first effect is that the temporarily larger duty ratio causes the peak inductor current to increase each switching cycle, with an accompanying increase in the average inductor current. If the signal frequency is quite low, the positive deviation in duty ratio will be present for many switching cycles. This results in a large cumulative increase in inductor current, whose phase lags $\hat{d}$ by 90°. This change in inductor current flows through the diode during the "off" time causing a proportional change in output current, in phase with the inductor current.

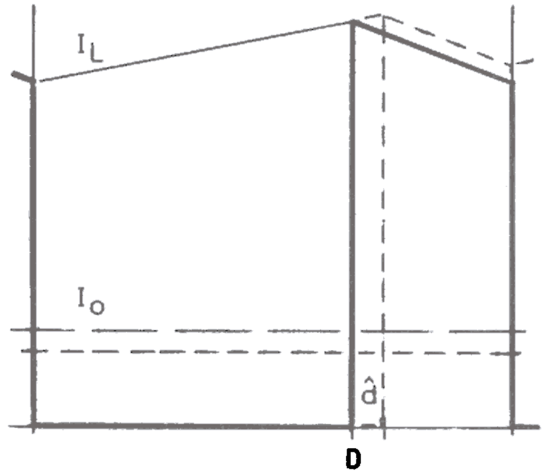


Figure 2

The second effect is more startling: The temporary increase in duty ratio during the positive half-cycle of the signal causes the diode conduction time to correspondingly *decrease*. This means that if the inductor current stays relatively constant, the average diode current (which drives the output) actually decreases when the duty ratio increases. This can be clearly seen in Figure 2. In other words, the output current is 180° out of phase with $\hat{d}$. This is the circuit effect which is mathematically the right-half-plane zero. It dominates when the signal frequency is relatively high so that the inductor current cannot change significantly.

<u>Duty Ratio Control Equations:</u> The equations for the flyback circuit are developed starting with the voltage V_L across the inductor, averaged over the switching period:

$$V_L = V_i D - V_O(1-D) \quad = (V_i+V_O)D - V_O \qquad (1)$$

Modulating the duty ratio D by a small AC signal $\hat{d}$ whose frequency is much smaller than the switching frequency generates an AC inductor voltage, $\hat{v}_L$:

$$\hat{v}_L = (V_i+V_O)\hat{d} + \hat{v}_O(1-D) \quad \simeq (V_i+V_O)\hat{d} \qquad (2)$$

Assuming V_i is constant, $\hat{v}_L$ is a function of $\hat{d}$ and of $\hat{v}_O$, the AC voltage across the output filter capacitor. At frequencies above filter resonance, $\hat{v}_O$ becomes much smaller than $\hat{v}_L$, and the second term may be omitted.

AC inductor current, $\hat{i}_L$, varies inversely with frequency and lags $\hat{v}_L$ by 90°. Substituting Eq. 2 for $\hat{v}_L$ gives $\hat{i}_L$ in terms of $\hat{d}$:

$$\hat{i}_L = \frac{\hat{v}_L}{j\omega L} = -j\frac{(V_i+V_O)}{\omega L}\hat{d} \qquad (3)$$

Referring to Figure 1, the inductor provides current to the output through the diode only during the "off" portion of each cycle:

$$I_O = I_L(1-D) \qquad (4)$$

Differentiating Eq. 4, the AC output current, $\hat{i}_O$, has two components (ref. Fig. 2 discussion) -- one component in phase with $\hat{i}_L$ and the other 180° out of phase with $\hat{d}$:

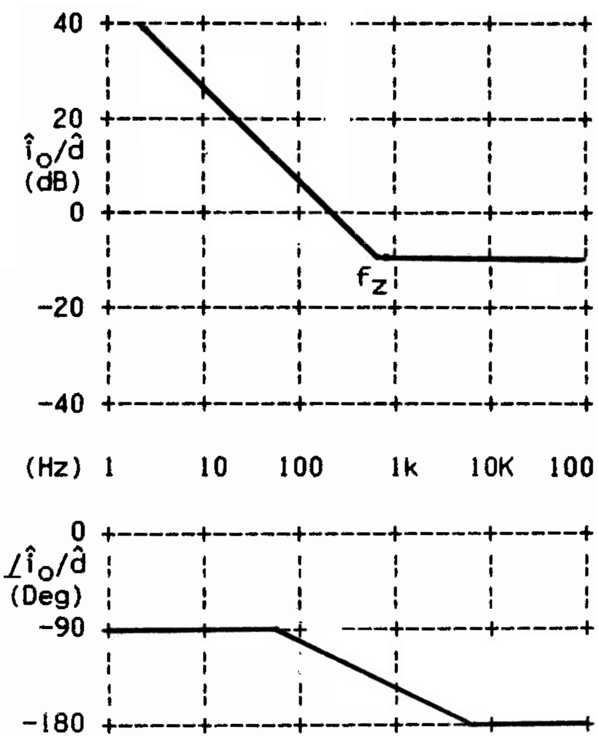
$$\hat{i}_O = \hat{i}_L(1-D) - I_L\hat{d} \tag{5}$$

Substituting Eq. 3 for $\hat{i}_L$ gives $\hat{i}_O$ in terms of the control variable $\hat{d}$. In a continuous mode flyback circuit, $(1-D) = V_i/(V_i+V_O)$:

$$\hat{i}_O = -j\frac{(V_i+V_O)(1-D)}{\omega L}\hat{d} - I_L\hat{d} = -j\frac{V_i}{\omega L}\hat{d} - I_L\hat{d} \tag{6}$$

The first term is the inductor pole, which dominates at low frequency. Its magnitude decreases with frequency and the phase lag is 90°. At a certain frequency the magnitudes of the two terms are equal. Above this frequency, the second term dominates. Its magnitude is constant and the phase lag is 180°. This is the RHP zero occurring at frequency ω_Z where the magnitudes are equal.

Figure 3 is a Bode plot of Eq. 6 (arbitrary scale values). Above f_Z, the rising gain characteristic of the RHP zero cancels the falling gain of the inductor pole, but the 90° lag of the RHP zero *adds* to the inductor pole lag, for a total lag of 180°. The Bode plot of the entire power circuit would also include the output filter capacitor pole, which combines with the inductor pole resulting in a second order resonant characteristic at a frequency well below the RHP zero. The ESR of the filter capacitor also results in an additional conventional zero.



Figure

The RHP zero frequency is calculated by equating the magnitudes of the two terms in Eq. 6, and solving for ω_Z:

$$\omega_Z = \frac{V_i}{L\ I_L} \tag{7}$$

Substitute Eq. 4 for I_L, V_O/R_O for I_O.
In a flyback circuit, $V_i/V_O = (1-D)/D$; $(1-D) = V_i/(V_i+V_O)$:

$$\omega_Z = \frac{R_O\ V_i(1-D)}{L\ V_O} = \frac{R_O\ (1-D)^2}{L\quad D} = \frac{R_O\quad V_i^2}{L\ V_O(V_i+V_O)} \tag{8}$$

Current Mode Control Equations: Equations 1, 2, 4, and 5 pertain to the flyback continuous mode power circuit, and are valid for any control method including current mode control. Eq. 3 is valid for current mode control, but it applies to the inner, current control loop. Solve Eq. 3 for $\hat{d}$ in terms of $\hat{i}_L$ and substitute for $\hat{d}$ in Eq 5:

$$\hat{i}_O = \hat{i}_L(1-D) - j\frac{\omega L\ I_L}{(V_i+V_O)}\hat{i}_L = \frac{V_i}{(V_i+V_O)}\hat{i}_L - j\frac{\omega L\ I_L}{(V_i+V_O)}\hat{i}_L \qquad (9)$$

Equations 6 and 9 are the same, except that in Eq. 6 the control variable is $\hat{d}$ for duty ratio control, while in Eq. 9 the control variable is $\hat{i}_L$ established by the inner loop and consistent with current mode control.

Unlike Eq. 6 for duty ratio control, the first term in Eq. 9 is constant with frequency and has no phase shift. This term dominates at low frequency. It represents the small signal inductor current which is maintained constant by the inner current control loop, thus eliminating the inductor pole. The second term *increases* with frequency yet the phase *lags* by 90°, characteristic of the RHP zero. It dominates at frequencies above ω_Z where the magnitudes of the two terms are equal. The RHP zero frequency ω_Z may be calculated by equating the two terms of Eq. 9. The result is the same as Eq. 7 for duty ratio control.

Figure 4 is the Bode plot of Eq. 9. The output filter capacitor will of course add a single pole and an ESR zero. Because the inductor pole is eliminated by the inner loop, the outer voltage control loop does *not* have a 2-pole resonant (second order) characteristic. However, the RHP zero is clearly still present with current mode control.

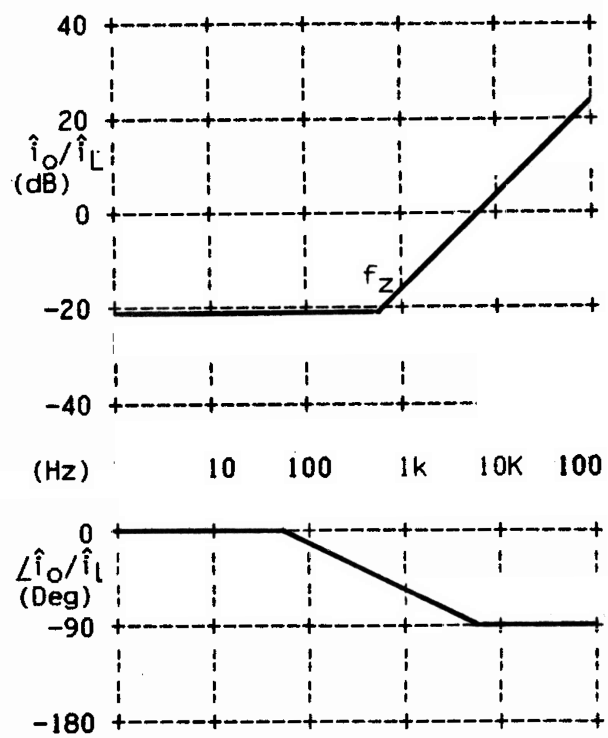


Figure 4

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