Active Clamp and Reset Technique Enhances Forward Converter Performance

Achieve Zero Voltage Transitions (ZVT), Higher Efficiency, Higher Frequency Switching and Reduced EMI/RFI

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Introduction:

The buck derived forward converter is one of the most popular switchmode topologies, second only to the infamous flyback converter. High input to output step down or up in voltage is easily achieved by using the appropriate transformer turns ratio. Galvanic isolation is frequently added between the supply and load "grounds" for increased safety and protection or to supply power to an isolated load. For these and other reasons, the forward converter has become a cost effective solution to many power management needs. With its continuing proliferation, new opportunities emerge for more efficient operation, higher switching frequencies, reduced EMI/RFI and extended duty cycle operation. This paper presents an innovative technique to properly clamp and reset the forward converter's main transformer while achieving low loss, zero voltage transitions of the power switch under wide duty cycle variations without the excessive voltage stress otherwise seen.

General Applications

Forward converters offer a cost effective solution to fill the void created between the low power flyback converter and the more complex high power bridge types. Typically, this span covers most applications between 125 and 1000 Watts, but the exact level depends on a number of variables including input voltage and its range. Using continuous inductor current operation, the forward converter utilizes a much lower peak current than it's flyback counterpart. This is advantageous with low voltage inputs, where even at 50 Watts, the peak primary current reaches tens of amps.

The conventional forward converter uses a single power switch, a definite advantage over the two switches used in the half bridge or four required by a full bridge converter. Also, the forward's switch is "low" side referenced for simplified interface to the PWM controller, although a two transistor variety was also common and similar to one half of a full bridge. But by-and-large, the single switch type is the most predominant in use today. Most off-line designs operate over a universal 85 VAC to 265 VAC input range, although some 110/220 VAC models still incorporate jumpers to accommodate both inputs. Forwards are extremely popular in DC to DC conversion, especially in Telecommunications and distributed DC bus applications. Many utilize peak current mode control and limit the duty cycle to 50% maximum, although the recent trend has been towards "stretching" this to 70% to efficiently accommodate a wider input range.

Conventional Forward Converters:

First generation forward converter designs were limited to operate below a 50% maximum duty cycle to insure proper reset of the main transformer, preventing potential saturation problems. A separate "reset" winding was incorporated in the main transformer to provide a convenient route for

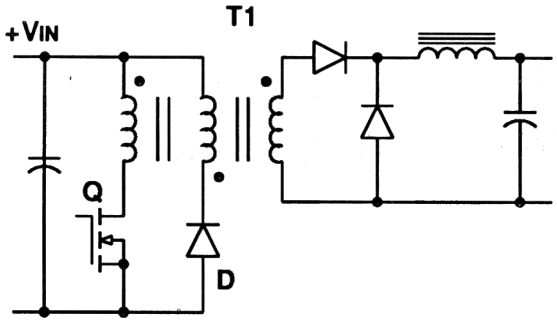


Fig 1. - Conventional Forward Converter

clamping the reset voltage amplitude to the input supply source. These two safeguards would guarantee proper operation and reset over all line and load conditions. However, a penalty is incurred due entirely to the limited maximum duty cycle. A lower transformer turns ratio results, which translates into a higher primary current than otherwise necessary. Designing for operation over a wide input voltage range exaggerates the difficulty with this approach. Very narrow duty cycles are necessary at high line to meet the 50% maximum duty cycle clamping at low line conditions. Operation over a worldwide AC input voltage span hardly results in an efficient power supply design at any set of line and load conditions since numerous compromises must be considered. It does, however, recycle the energy stored in the transformer's magnetizing inductance back to the primary side input capacitor, somewhat of a redeeming factor. The associated schematic and operational waveforms are displayed in Figures 1 and 2.

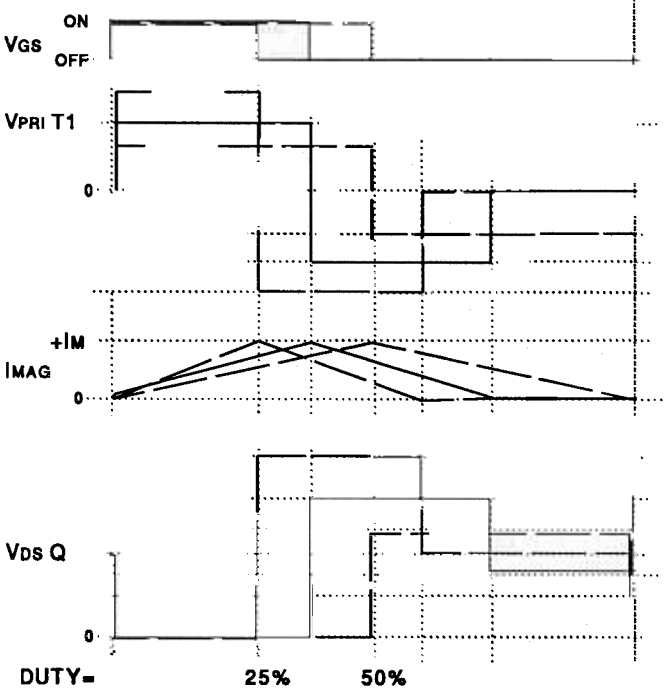


Fig 2. - Conventional Forward Converter Waveforms

"RCD" Type Forward Converter:

It wasn't long before the conventional adaptation of the forward converter gave rise to the second generation converters using a different clamp and reset technique which enabled stretching the duty cycles above the 50% barrier. Commonly referred to as the "RCD" type for its Resistor, Capacitor and Diode, these components are used to develop a varying clamp voltage into which the magnetizing energy is dissipatively discharged. However, using a high clamp voltage with an amplitude greater than twice the input supply will facilitate maximum duty cycles which can stretch beyond the 50% milestone, particularly useful in wide range input supply designs. Note that there are two penalties to be paid with this adaptation: high voltage stress on the semiconductors and power losses from the resistor in the clamp circuit. These sacrifices must be evaluated along with any potential gains from reduced primary currents and transformer cost (no reset winding) when comparing the RCD to the conventional forward design alternative. Generally, the RCD is the preferred choice for wide input ranges, especially low voltage input designs where a higher clamp/reset voltage still yields manageable low voltage semiconductors. These RCD type designs frequently require an iteration (or a few) more than their predecessors, with much of the development efforts spent on optimizing the clamp network over all operating conditions. They, too, tend to suffer from less than optimal efficiency at any line or load, just like their predecessor. Nevertheless, the RCD forward converter designs are very popular and can be made fairly efficient and

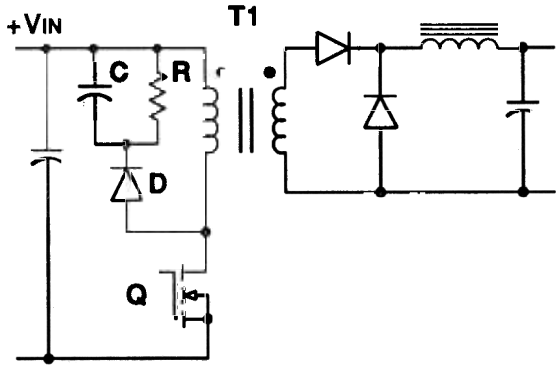


Fig 3. - RCD Forward Converter

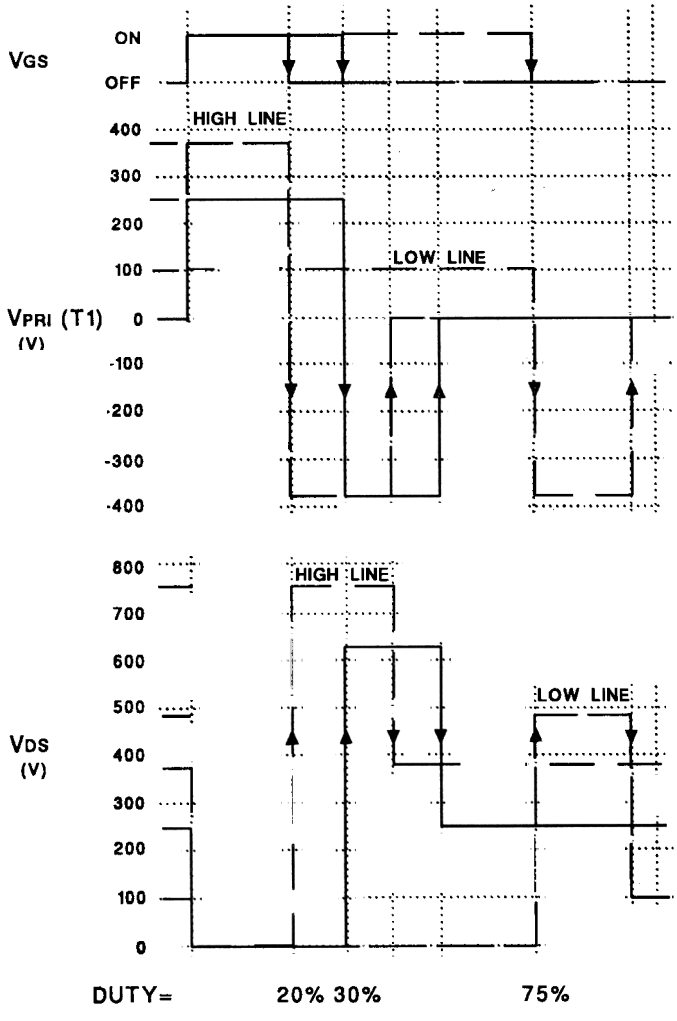


Fig 4. - Ideal RCD Forward Converter Waveforms

cost effective, but there's always room for improvement. The schematic and associated operating waveforms for this variety are shown in Figure 3 and Figure 4 respectively.

Design Tradeoffs with the RCD Forward: As shown by the waveforms of Figure 4, a high voltage exists across the power supply switch during reset of the RCD forward converter, especially in an extended duty cycle (>50% maximum) application. A good example of this is a power supply designed to operate with universal AC inputs from 85 VAC at low line to 265 VAC at high line. For the sake of this example, the maximum duty cycle will be limited to 75% at low line to keep semiconductor ratings reasonable. The resultant duty cycle needed to achieve regulation of the output (constant volt seconds applied) indicates that a 50% duty cycle is reached at 127 VAC, and a 25% duty cycle is needed at high line.

In order to insure reset of the main transformer, the applied volt-second product must be equal to the reset volt-second product according to the following relationships:

$$Vin \cdot D = Vreset \cdot (1-D)$$

$$Vreset = Vin(min) \cdot Dmax \,/\, (1-Dmax)$$

$$Vds = Vin + Vreset$$

Maximum Drain-Source Voltage: Note that in this example, the reset voltage is referenced to the high side of the input voltage (Vin). Therefore, the maximum drain voltage of the MOSFET switch is Vin plus Vreset. The worst case condition could occur at high line, and the table on the next page is a summary of the circuit voltages as a function of operating conditions for one example of an off-line converter with a 75% maximum duty cycle at low line.

TYPICAL RESET CONDITIONS
(using 80% of available t(off) for reset)

Vin (VAC)	Vin (VDC)	Duty Cycle	Vreset (VDC)	Vds(max) (VDC)
85				
132				
180				
265				

This table uses rather optimistic reset conditions. In reality, it is difficult to design an optimal RCD network to accommodate all leakage inductance load effects while maintaining a low maximum clamp voltage. Low line and light load conditions generally dictates the clamp capacitor and resistor value needed to facilitate the proper transformer reset. At higher line and load conditions, generally the clamp's resistive load is less than ideal, causing the clamp voltage to increase. In an off-line supply, this could push device ratings and safety isolation requirements above 800 VDC, potentially creating new problems, especially when safety agency regulations are considered.

Leakage Inductance Effects:

The previous examples of reset techniques do not take into account the effect of the transformer leakage inductance - which is significant. It may be the dominant factor in most off-line applications, especially where high leakage inductance is the result of facilitating safety agency spacing and isolation requirements. In these applications, the magnetizing inductance effects on the clamp capacitor voltage are minimal, and reflected load current effects will primarily govern the clamp voltage. The opposite of this may be more of the case in DC to DC converters and planar magnetic designs where much lower leakage inductance is more common in comparison to off-line designs.

In either case, certain generalizations can be used to arrive at quantitative results. For example, an off-line transformer's leakage inductance is typically somewhere between 0.1% - 1% of the magnetizing inductance, depending on a number of factors. These include core geometry or style, isolation requirements and winding configurations.

Off-line converter transformers incorporate a high primary inductance to minimize the magnetizing current and keep power losses low. If not, the peak magnetizing current could conceivably be higher than the reflected load current, reducing efficiency. Typically, the magnetizing current is designed to be between 10% - 25% of the reflected load current. Each design is unique, but this is typical of many design practices. Furthermore, primary magnetizing inductances are in the range of 1 - 5mH for most off-line, high frequency designs. This being the case, a 2.5mH primary is used for the purpose of analysis. Also, a leakage to magnetizing inductance ratio of 1% is used, corresponding to 25µH.

Lpri = 2.5mH; Llkg = 25µH

Let's look at the design of an RCD clamp network for the following design specifications.

Pout = 200W

Fswitching = 100kHz

T(period) = 10µs

Duty cycle will adjust to the varying line input, but the volt-second product will be constant. To cover the universal AC input range of 85 to 265 VAC, the duty cycle will change from its maximum of 75% at 100 VDC (rectified and filtered 80 VAC) to 19% at 400 VDC.

Vin = 100 VDC, D = 0.75 (75%)

Vin = 250 VDC, D = 0.30 (30%)

Vin = 400 VDC, D = 0.19 (19%)

The peak magnetizing current is determined by:

Imag = (Vin•T(period)•D) / Lmag

Under any of these conditions, the peak magnetizing current is 0.30 A because the transformer's volt-second products must balance. The transformer primary current can be approximated from the following relationships, ignoring output inductor charging current and any inefficiency in the entire power conversion. At full load:

Iin(DC) = Pin/Vin(min) = 200W/100V = 2A

Ipri' = Iin(DC)/Duty(max) = 2A/0.75 = 2.66A

A good estimate of light load is ten percent of the full load current for most Buck derived converters. For this 20W condition, the primary current is:

Iin(DC) = 20W / 100V = 0.2A

Ipri' = 0.2A / 0.75 = 0.266A

The actual primary current flowing in the leakage inductance is the sum of the reflected load current and the magnetizing current, ignoring the output inductor charging current for this analysis.

Imag(pk) = 0.3A

Ipri'(max) = 2.66A

Ipri'(min) = 0.27A

Ipri(max) = I(mag) + Ipri'(max) = 2.96A
(use 3A)

Ipri(min) = I(mag) + Ipri'(min) = 0.57A
(use 0.6A)

Clamp Voltage: The clamp voltage and capacitor value needs to be determined. Since the primary volt-seconds must balance each cycle, a 300 Volt clamp is the minimum value for the listed (100VDC, 75% Dmax) design conditions. Note that this condition must be met at light load, corresponding to the lower amount of leakage energy dumped into the clamp network. As the load increases, so too will the clamp voltage as more energy is transferred. Proper reset of the transformer must be guaranteed under the *worst case situation, corresponding to low line, light load conditions.* A ten percent safeguard (approximately) will be added for increased margin, resulting in a 330V clamp voltage.

The exact capacitance required is determined by the acceptable clamp capacitor ripple voltage which causes heating due to the ripple current flowing in the capacitor's Equivalent Series Resistance (ESR). A good initial estimate for this analysis is 10V of ripple at light load since this ripple will only increase with load.

VCc = 330V

dVCc = 10V at light load

Load Effects: The energy into the clamp capacitor is equal to the energy stored in the leakage inductance provided that little energy is lost in the conversion. This is generally NOT the case in many 200 Watt converters for a few reasons. First, a portion of this energy goes into charging the MOSFET switch output capacitance from essentially zero to the input voltage, plus the clamp voltage (Vin + VClamp). Another portion goes into charging the transformer primary capacitance from the input to the clamp voltage, Vc. Both of these capacitances could easily be in the same order of magnitude as the clamp capacitance, and an extensive evaluation is necessary to determine the effects. Detailed analysis of this requires the use of modelling and simulation tools, but a general comparison can be made by looking at the change in stored inductive energy in the leakage, WLlkg.

Leakage Inductance Effects Summary: Many combinations of clamp capacitance and resistance values are possible for a given application, depending on the ratio of light to full load current, the ratio of leakage to magnetizing inductances, maximum clamp voltage, transformer primary capacitance and MOSFET switch capacitance, Coss. All of these parameters need to be weighed in addition to proper reset of the transformer core under all

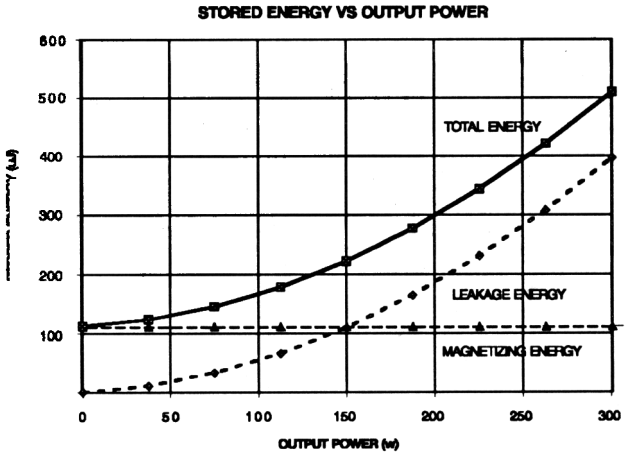


Fig 5. Load Effects on Stored Energy

operation conditions to determine the optimal combination for a given design. Beyond the scope of this presentation, an authoritative design procedure for this RCD clamp network could be generated.

Active Clamp/Reset Technique:

The newest adaptation of the common RCD type reset technique is to replace the diode with an active MOSFET switch. Its first purpose is to clamp the primary to the reset capacitor, just as diode would. A second function, which a standard rectifier is unable to provide, is to allow a controlled (switched) transfer of energy back from the reset capacitor to the primary side power stage of the converter. Current in the MOSFET switch "channel" is bidirectional during part of its active interval, but is zero during the remainder of the switching cycle. Note that the active clamp and reset techniques are inactive during the normal power transfer portion of the switching cycle, and only operate during the main switch's off-time. For the most part, conventional square wave power conversion waveforms apply to system voltages and currents during the on-time of the main switch. However, significant improvements and differences take place during the low loss clamp, reset and soft alignment of the power switch. Two pivotal benefits are obtained with this new approach: higher efficiency and zero voltage "soft" switching transitions. One adaptation of this circuit is shown in Figure 6.

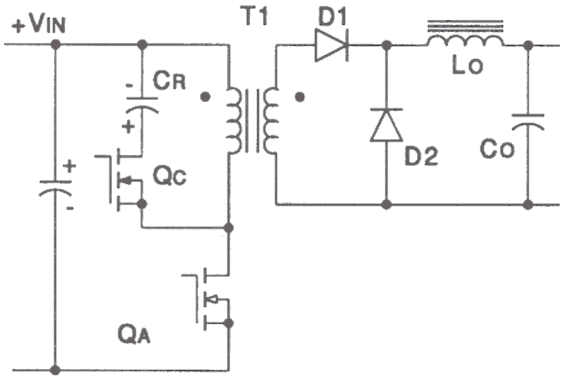


Fig 6. - Forward Converter with Active Clamp

SIGNIFICANT BENEFITS:

- "recycles" transformer magnetizing energy instead of dissipating it in a resistor
- facilitates Zero Voltage Transition of the main switch for higher efficiency
- uses lower voltage MOSFET and diodes compared to the RCD
- reduced EMI/RFI via soft switching
- eliminates lossy snubber network on primary
- operates at fixed frequency
- allows much higher frequency operation
- similar power transfer to conventional square wave switching
- duty cycles beyond 50% max are obtainable
- actively resets main transformer to third quadrant of BH curve

DIFFERENCES AND SIMILARITIES:

This new approach requires a few more parts than the other forward choices to achieve the benefits listed previously. Differences include:

- an additional high voltage MOSFET clamp/reset switch
- an isolated, variable duty cycle gate drive for the clamp/reset switch
- a modified PWM control technique to properly program the associated delays between gate drives to achieve the zero voltage transitions
- a new gate drive technique to extract the proper clamp/reset drive pulse

Nearly all other aspects of the converter primary and secondary power stage, including magnetic components are very similar to the RCD approach, although stressed less. Many existing forward converter designs can be modified for a "quick" comparison, but some changes are required in the control circuitry and in the primary power stage. Nevertheless, modifying an existing unit is probably the shortest, easiest and most direct route to an "apples-to-apples" evaluation of this improved technique.

FORWARD CONVERTER COMPARISON

Parameter	Conventional	RCD Type	Active
Efficiency	high	high	**highest**
max. Duty	< 50%	**> 50%**	**> 50%**
Voltage Stress	**lowest**	highest	high
Current Stress	higher	**lower**	**lower**
Turns Ratio	lower	**high**	**high**
I(mag),I(lkg)	**recycled**	dissipated	**recycled**
Higher Freq.	Good	fair	**best**
Complexity	**lowest**	moderate	highest

Mastering the Active Clamp Technique : There are several fundamental timing intervals with this novel approach to explore in detail, only some of which are entirely new. Overall, this technique is a blend of the attributes of conventional fixed frequency, square wave power conversion with the zero voltage transitions of the phase shifted, full bridge technique. There is one interesting new difference to note, necessary to facilitate ZVT. This active clamp technique forces a "reverse" magnetizing current to flow through the transformer for a small portion of the timing period, storing energy in the primary inductance. When released, this energy is used to position the main switch voltage to zero by discharging the MOSFET(s) output capacitance just prior to it turning on. This alignment to zero drain voltage will automatically occur each switching cycle provided that enough inductive energy is stored to overcome the opposing capacitive energy requirements of the circuit and power MOSFET(s). Zero voltage transitions can be forced over a wide variety of input voltages and a wide range of output load currents because of this "reverse" storage of energy.

First, the general circuit schematic of Figure 6 will be expanded to include the MOSFET parasitic output capacitance (Coss) and the internal body diode for clarity. The three integral components of each switch will be separately labelled and identified to demonstrate the exact current paths during each interval. The MOSFET channel (switch) is designated by "Q", the output capacitance by "C" and body diode by "D". The main switch of the power converter is referred to as switch "A" composed of "QA", "CA" and "DA", whereas the clamp/reset switch is referred to as Q"C" (etc), for clamp. "Creset" is the clamp/reset energy storage capacitor. The word "reset" was chosen instead of "clamp" so there would be no conflict with "Cc", the clamp switch output capacitor. Next, the circuit will be redrawn slightly differently as shown in Figure 7. Note the similarity between this representation of the active clamp and reset technique to the conventional half-bridge topology. The two exceptions are the non center tapped secondary of the main transformer, and "missing" connection between the input supply and the high side of the reset capacitor. Make these changes to a standard half-bridge, modify the gate drives and you've got the makings of an active clamp/reset forward. It's not quite this simple because of issues with the transformer secondaries, but there are similarities.

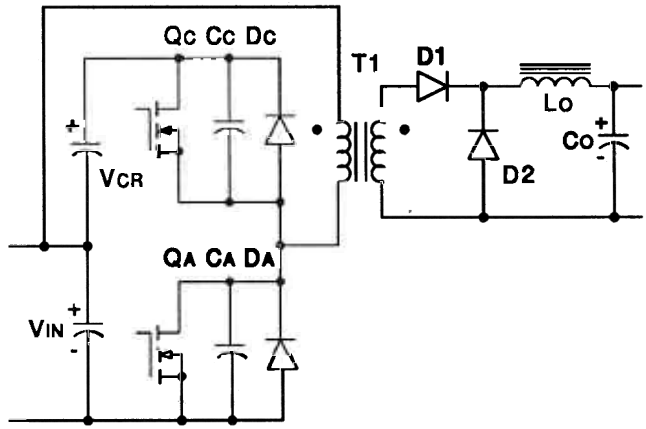


Fig 7. Active Clamp Forward Converter

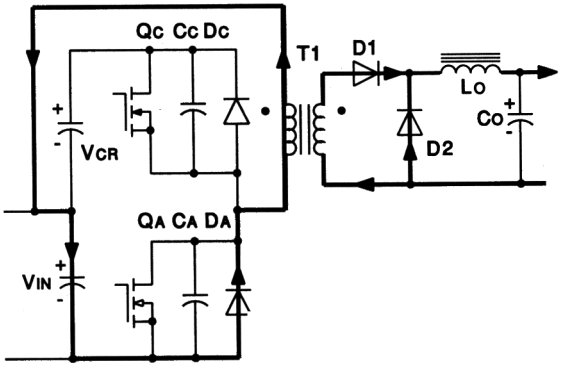
Theory of operation : One complete switching period will be broken down into eight individual sections (t0 - t8) for the purpose of this presentation. Depending on the level of interest, this technique can be described in either more, or less detail, however eight relevant ones have been selected. The gate drives, voltages and currents at all fundamental components and nodes will be analyzed during each timing interval, and the respective waveforms will be highlighted.

INITIAL CONDITIONS: time t < t0

The analysis of this technique will begin by stating the initial conditions where steady state condition have previously been established and the converter is up and running at normal output voltage and some static load condition. As for the switches, MOSFET QA, the main power switch is OFF, but has already been aligned with zero voltage across it. The clamp/reset switch QC is also OFF with a voltage across it equal to the clamp (Vcr) voltage plus the input (Vin). Previously, energy had been stored in the transformers magnetizing and leakage inductance which is now being released as a "reverse" primary current. The path followed is through the transformer from bottom to top, and into the positive terminal of the input capacitor, Cin, charged to Vin. This path continues out through the low side of Creset, and over to the main switch where it is conducted through its body diode, DA. Enough energy has been stored to continue this condition even beyond time t0 when switch QA is turned ON.

On the secondary side things are not quite so clear because of the unknown transformer leakage inductance and coupling between the windings. This can be simplified for the sake of this presentation by assuming that nearly all of the secondary (output) current is flowing through output diode D2, and that only a small amount is conducted by D1. Another assumption is that there was ample energy available on the primary side to overcome the coupling effects from the secondary to the primary winding, and facilitate the zero voltage transition of QA. Let's spare the details for now as they will be clarified in the analysis of the final timing interval, t7 to t8.

In summary, both switches are OFF and no power is being transferred from input to output. The main switch, MOSFET QA is aligned at zero volts and a reverse current flowing in the primary due to stored inductive energy is clamping the switch there



Conditions:					
t=	t	t*	t=	t	t
QA	OFF		Qc	OFF	
CA	Dischgd		Cc	Chgd	
DA	ON		Dc	OFF	
D1	ON	I < Io	D2	ON	I < Io
VPRI'	+VIN		IPRI	= -Im	(t0)
IM	Negative	Decrease			

Fig 8. Initial Conditions -- t < t0

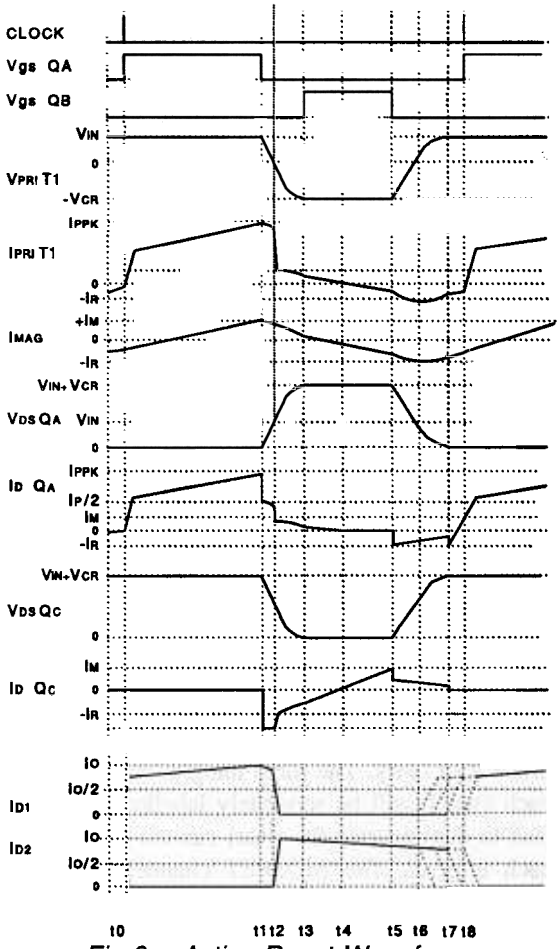
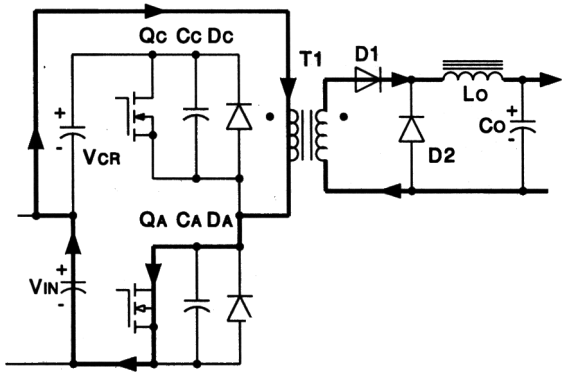


Fig 9. - Active Reset Waveforms

via its body diode, DA. A table below Figure 8 displays the various component conditions for further clarity. A preview of waveforms for the entire switching cycle is presented in Figure 9.

POWER TRANSFER: Figure 10, t0 < t < t1

This interval is nearly identical to conventional square wave power conversion. It starts out at time t0 when the forward's main switch QA is turned ON, initiating the transfer of power from the primary to the secondary via the main transformer. From the onset of this interval, switch QA was aligned with zero volts across it, and "reverse" primary current was flowing through the body diode DA, clamping the drain voltage to the lower rail. When QA is turned ON the current is diverted from the body diode to the device's channel since it's generally a lower impedance and can conduct in either direction. The transformer primary current will build to the reflected load current (Iout/N) at the rate of Vin divided by the effective series inductance. The transformers leakage inductance (Llkg) will be used for this analysis, although any other series inductance should be taken into account. As this occurs, the driven current in the transformer secondary also climbs, forward biasing diode D1. Current previously flowing in diode D2 is decreasing by the same amount rising in D1 such that the two equal the full load current. This brief transient portion of this interval could be examined in closer detail, if desired, although somewhat incidental in the overall picture. Primary current is the sum of three individual currents, the reflected output load current, the reflected output inductor charging current and also the primary magnetizing current.



Conditions:					
t=	t0	t1	t=	t0	t1
QA	OFF →	ON	Qc	OFF	
CA	Dischgd		Cc	Chg to	VCR+V1
DA	ON →	OFF	Dc	OFF	
D1	ON →	ON	D2	ON →	OFF
VPRI'	+VIN		IPRI	≈ -Im to	+IO/N
IM	Decrease	Increase			

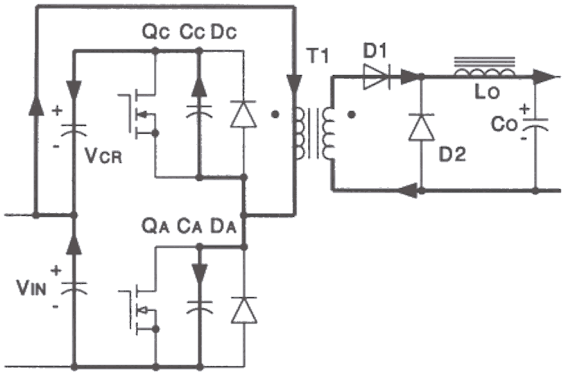
Fig 10. Power Transfer -- t0 < t < t1

Very quickly into this interval, the normal flow of power has been established and switch QA remains ON for the exact amount of time to regulate the output voltage. This is all handled by the Pulse Width Modulator (PWM) section of the control circuitry which can be achieved by a number of popular techniques and Ics. Once the correct time has been reached at the end of this interval (t1), switch QA will be turned off. But for the most part, this interval is identical to conventional switching technology.

LINEAR TRANSITION: Figure 11, t1 < t < t2

At time t1, the correct pulse width has been reached and switch QA is turned OFF. "Instantly", the current in the MOSFET device is diverted from its channel (QA) to its output capacitance, CA. The body diode (DA) is reversed biased and not pertinent. With the reflected "full" load current flowing in the primary, fueled by the large output inductor (Lo), CA charges very quickly. The voltage across the MOSFET device rises "linearly" while the voltage across the clamp MOSFET (QC) simultaneously decreases "linearly". This activity continues until time t2 when CA is fully charged to the input voltage (Vin). Similarly, the voltage across CC has decayed from its initial value of Vcr to (Vcr - Vin). This interval concludes at time t2 when the transformer's primary voltage reaches zero. For clarity, this scenario can be viewed as two capacitors in parallel (CA & CC) being driven from a "constant" current source equal to Iout/N, ending when V(CA) reaches Vin.

In minuscule detail, this linear approximation is not exact - but a useful simplification because the



Conditions:					
t =	t1	t2	t =	t1	t2
QA	ON →	OFF	Qc	OFF	OFF
CA	VCA=0	Charging to +VIN	Cc	VCR+VIN	Dschg to (VCR)
DA*	OFF	OFF	Dc*	OFF →	OFF
D1	ON →	'ON'	D2	OFF →	-OFF'
VPRI'	VIN →	0	IPRI	IPPK →	+IM
IM	Increasing →				

Dependent on Leakage & Coupling.

Fig 11. - Linear Transition -- t1 < t < t2

interval is so brief. Here's why. First, the primary current is not constant, it's actually increasing. Although the net voltage across the transformer primary is rapidly decreasing from Vin to zero, it starts out positive and stores energy in the leakage and magnetizing inductances for the duration. Superimpose this component on top of a "constant" reflected output current (due to the large output inductor) and the sum is the net primary current - still increasing. Note that the charging and discharging the two MOSFET output capacitances (CA and CC) is due to current flowing from the input supply and clamp capacitor. It is NOT cause by transferring previously stored inductive energy, as will occur later in another timing interval to align the switches back to zero voltage.

On the secondary side, an assumption is made that all of the load current continues to flow only through diode D1 during this interval. As the transformer voltage collapses to zero at t2, this situation could change depending on the design, magnetic coupling and placement of the leakage inductances in the physical transformer.

Design equations: The brief time spent in this interval can be approximated by solving the following relationship for time, dt, which corresponds to dt(2 -1).

$$\mathbf{I = C \cdot \Delta v / \Delta t}$$

The change in voltage, ΔV, is equal to Vin since the transformer goes from Vin to zero during this interval.

$$\mathbf{\Delta V = Vin}$$

The effective capacitance in this equation is the parallel combination of the two switches' output capacitances, CA and CC. To compensate for the effective capacitance of a MOSFET with high voltage applied, International Rectifier, a major MOSFET manufacturer suggest multiplying the specified Coss term by a 4/3 factor. Also, the transformer primary capacitance must be taken into account as a parallel capacitance. The net capacitance is :

$$\mathbf{C = (CA + CC) \cdot 4/3 + Cpri(T1)}$$

The primary current flowing at time t1 can be approximated by the output load (or inductor) current divided by the transformer turns ratio N. While this is a simplification, it's a fairly accurate representation provided that the output ripple current and transformer magnetizing currents are "low".

$$\mathbf{Ipri(t1) = Iout/N}$$

Duration of this timing interval can be approximated as:

$$\mathbf{dt(2\text{-}1) = \{(CA+CC) \cdot 4/3 + CpriT1] \cdot Vin \cdot N\} / Iout}$$

Note that while the primary current hasn't changed in amplitude very much, the route being taken does change. The full primary current now divides into charging the output capacitance of the main switch QA, and discharging the output capacitance of the clamp switch, QC. For the sake of simplicity, an approximation that the current divides equally can be used for analysis, although the exact ratio is a function of each device's output capacitance. Therefore, at time T1, the current in QA drops from the full load current to one-half of that, and instantly goes from zero to half of the full load current in QC. This is an approximation assuming

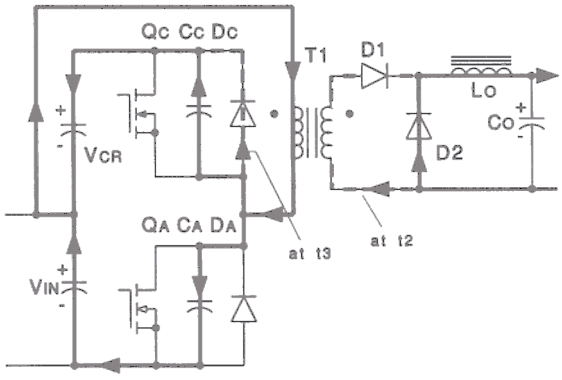
that the MOSFET switch output capacitances are identical. In a practical application they will not be the same since a smaller device is typically used for the clamp/reset function. Therefore, it's likely that slightly more than half will flow in the main switch and slightly less than that flows in the ZVT switch.

PASSIVE RESET & RESONANT TRANSITION
Figure 12, t2 < t < t3

At time t2 the transformer primary voltage has reached zero which is also reflected to its secondary. This causes the full load current to transfer from diode D1 to D2 at a rate determined primarily by the secondary leakage inductance, but is all flowing in D2 at time t2. The transformer voltage continues its reversal from zero on towards the clamp voltage, Vcr. This transition is a resonant one because the previous catalyst of reflected load current is now gone with D2 conducting. This reverse biasing of D1 also allows the reversal of T1's voltage which continues from t2 through t3 when the clamp reset voltage is reached. Current in the clamp switch QC is negative during this interval as the output capacitance is discharging. Note that at time t3 the current in QC can equal zero, but will generally be slightly negative to guarantee that the enough energy is stored in the system to reach the clamp voltage. A similar situation is present at the main switch QA where its output capacitance is charged to the clamp voltage Vcr. Any additional current flowing in the primary before turn on of the clamp/reset switch (at t3) goes towards increasing the clamp capacitor voltage.

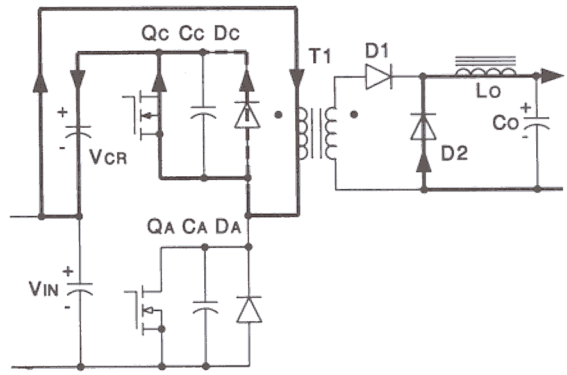
PASSIVE RESET / Imag > 0:
Figure 13, t3 < t < t4

At time t3 the transformer primary voltage has the clamp voltage applied which facilitates the reset of the magnetizing inductance. Also at time t3 the clamp/reset switch QC is turned ON which allows the reset current to transfer from the device's body diode to its channel, generally providing a lower impedance path. The main goal of turning the reset switch on, however, is to provide a path for current to later flow from the clamp capacitor reservoir to the transformer primary to facilitate the Zero Voltage Transition. But from time t3 until t4, the energy stored in the transformer's magnetizing inductance results in current is flowing back from



Conditions:					
t =	t2	t3	t =	t2	t3
QA	OFF →		Qc	OFF →	
CA	Increasing VIN	VCR +VIN	CC	Decreasing VCR → 0	
DA	OFF →		Dc	OFF → (ON) at t3	
D1	OFF →		D2	ON I = Io	
VPRI'	Decreasing 0 →	-VCR	IPRI	Decreasing +IM (t2 t3) = Im	
IM	Decreasing				

Fig 12. - Passive Reset and Resonant Transition -- t2 < t < t3



Conditions:					
t =	t3	t4	t =	t3	t4
QA	OFF →		Qc	OFF → ON	
CA	VCA=VCR +VIN		Cc	V= 0 →	
DA	OFF →		Dc	ON → OFF	
D1	OFF →		D2	ON →	
VPRI'	= -VCR		IPRI	Decreasing →	
IM	Decreasing → 0				

Fig 13. Passive Reset / Imag<0 -- t3 < t < t4

the transformer to the clamp capacitor.

Primary current decreases during this entire interval until reaching zero at time t4. It may not be necessary to explore the waveforms at time t4 in great detail. This interval was selected to demonstrate that there is a point in the overall conversion cycle when the transformer has been correctly reset and the next switching cycle could begin at t4, if necessary.

ACTIVE RESET / Imag < 0:
Figure 14, t4 < t <t5

Beginning at time t4, the transformer is actively reset by switch QC to the clamp/reset voltage, Vcr. The magnetizing current starts out at zero during this interval and is driven negative by the clamp circuit, storing energy in the magnetizing inductance. This will be used later to facilitate the Zero Voltage Transition.

Primary current initially rises at the rate determined by the clamp voltage divided by the magnetizing inductance (Vcr/Lm). However, note that a linear approximation is not valid for more that the first instant of time. This rate will never turn out to be truly linear unless a huge clamp capacitor value is used in addition to a large magnetizing inductance. This will only lead to major problems during transient response, and should be avoided.

As energy is transferred from the clamp storage capacitor to the magnetizing inductance the capacitor voltage will decrease. Note that a resonant L/C tank has been formed by these two components and must be further analyzed. The characteristic tank impedance (Zr) and frequency (ωr) need to be calculated, and the following equations apply.

$$Zr = (Lmag/Creset)^{1/2}$$

$$\omega r = 1 / (Lmag \cdot Creset)^2 \quad (\omega r \text{ in radians})$$

to convert this to frequency ;

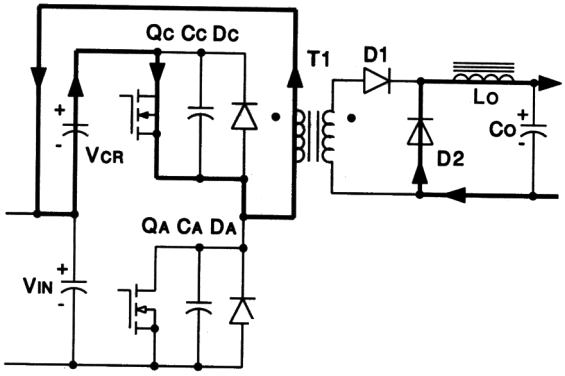
$$fres = \omega r / (2 \cdot 3.14159), \text{ or } \omega r / 6.28$$

the period of a complete resonant cycle is

$$Tres \text{ (period)} = 1 / fres$$

The active reset duration is the result of operating at a specific duty cycle and frequency, with the delay times accommodated. It is not programmed or controlled otherwise by the control circuit or PWM — just the result of performing output voltage regulation. Specific issues relating to this interval are presented elsewhere in this text.

What's really interesting is that the clamp voltage will adapt to the operating conditions and accommodate changes favorably. For example, let's arbitrarily let the main switch stay on too long which results in a higher magnetizing current (and energy) than ideal. During the time between turn off of the main switch and turn on of the reset switch, the magnetizing inductance discharges into the clamp capacitor, causing its voltage to increase. Now, when the reset switch turns on, it is at a higher voltage than previously which results in a higher reset current. This self correction will occur each cycle without the need of elaborate control circuitry.



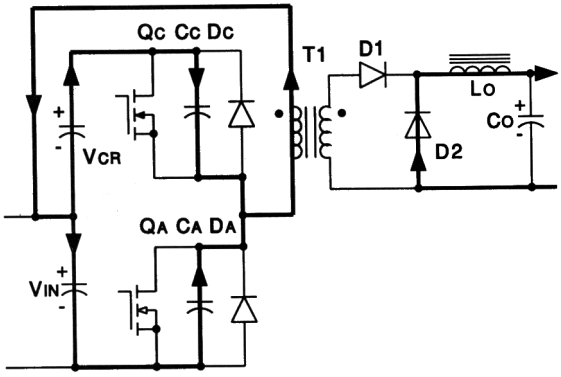
Conditions:			
t =	t4	t5	t = t4 t5
QA	OFF →		QC ON →
CA	VCA=VCR +VIN		CC Dischgd →
DA	OFF →		DC OFF →
D1	OFF →		D2 ON →
VPRI	= -VCR		IPRI 0 → Decreasing
IM	0 → Decreasing		

Fig 14. - Active Reset / Imag<0 -- t4 < t < t5

RESONANT TRANSITION:
Figure 15, t5 < t < t6

The reset switch is turned OFF at time t5 causing the primary current to divert from the device's channel (QC) to its output capacitance (CC). The voltage across the switch begins to increase, forcing the "source" node towards the lower supply rail from its initial amplitude of Vcr. The transformer primary voltage similarly begins to collapse, but note that the magnetizing current is still increasing from its level at time t5. Even though the voltage across the magnetizing inductance is decreasing, there is still voltage across it until time t6 causing the current to increase, but at a reduced rate.

Note also that a change has occurred in the drain current of the main switch, QA. No current was flowing in the device during the previous interval timing, but it does begin at time t5. The drain of QA was held at the clamp voltage (Vcr) while the clamp/reset switch QC was ON until t5. Once turned off, the primary current simultaneous charges the clamp switch output capacitor (CC) and discharges the main switch output capacitance CA. Since these are modelled in parallel, the total primary current is divided between the two circuits



Conditions:					
t =	t5	t6	t =	t5	t6
QA	OFF →		Qc	ON →	OFF
CA	Discharging V=VCR +VIN	VIN	Cc	Charges 0 →	VCR
DA	OFF →		Dc	OFF →	
D1	OFF →		D2	ON	
VPRI'	Increase (-VCR) →	0	IPRI	Decreasing →	-IR
IM	Decreasing →	-IR			

Fig 15. - Resonant Transition -- t5 < t < t6

as determined by the ratio of their output capacitances. The point here is that QA instantly sees some of the primary current to discharge its output capacitance which continues through this, and the next timing interval.

Over on the secondary side, nothing has changed since the last interval. The output inductor is discharging its stored energy, released as a "constant" output current. Diode D2 is commutating this current to the load, and D1 is off and reversed biased.

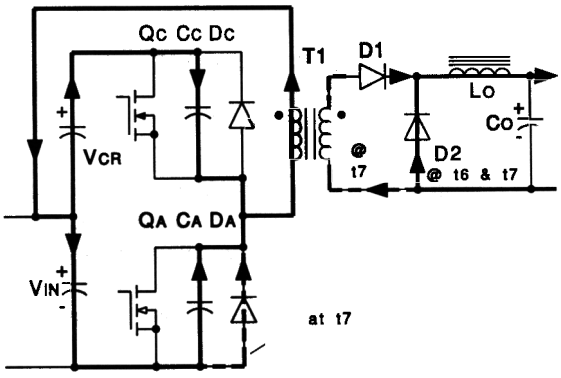
This interval concludes at time t6 when the voltage across the transformer is zero and the primary current has reached its lowest negative value (Ir) for the switching cycle.

RESONANT TRANSITION:
Figure 16, t6 < t < t7

The transition momentum established in the previous timing interval continues through this one as well, but with a few minor differences. First, notice that the primary current has reversed its slope, and, although negative, is now headed back towards zero. The transformer voltage reverses as well, since the transitioning node starts out at Vin and goes to zero at time t7. This will position it with the full input supply voltage across it, and no voltage across the main switch at the conclusion of the cycle.

This resonant interval is fueled by the energy stored in the magnetizing inductance from the Active Reset interval. Enough inductive energy must have been stored to overcome the opposing capacitive energy requirements of the two MOSFET switches, QA and QC. To accommodate all operating conditions, it is likely that the primary current at time t7 will always be small, but non-zero to facilitate ZVT. Any excess current will be funneled to the body diode of QA at time t7 for the main switch, and will go towards recharging the clamp capacitor voltage (Vcr) at the clamp/reset switch position. What is beneficial is that the peak to peak magnetizing current is constant over line and load conditions in normal operation, so little overdesign is necessary.

Depending on the secondary circuit inductance and coupling to the primary winding, the load



Conditions:					
t =	t6	t7	t =	t6	t7
QA	OFF	→	Qc	OFF	→
CA	VIN →	0	Cc	VCR →	VCR +VIN
DA	OFF →	ON	Dc	OFF	→
D1	OFF	ON*	D2	ON →	ON*
VPRI'	0 →	+VIN	IPRI	-IR →	Increasing
IM	-IR →	Increasing			

Depending on leakage.

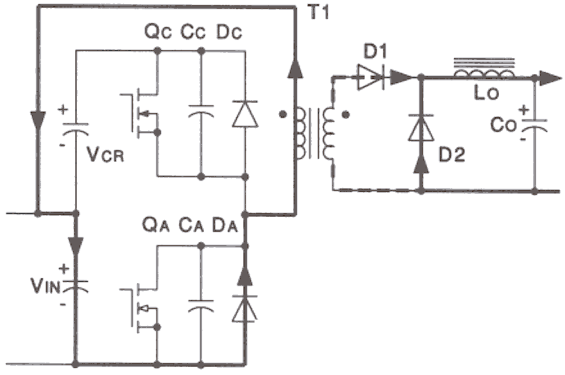
Fig 16. - Resonant Transition -- t6 < t < t7

current could transfer from D2 to D1 during this interval. After all, the transformer primary voltage has reached the same amplitude that it does for normal operation, however notice that the current is reversed. Its clear that no power is being transferred from the primary to the secondary, however the secondary voltage could be identical to that while QA is on. Two situations are most prominent for the load side. One is that the load current completely transfers from diode D2 to D1, but this would couple back to the primary in opposition to the resonant tank current, and dominate. The effect of this would be to re-position the main switch with the full input voltage across it, and the benefits of ZVT will go unrealized. The other situation is that diode D2 conducts the complete current and diode D1 is fully off. This would infer some rather lousy (bad) coupling between the transformers primary and secondary windings, which is possible. Several approaches to this Active reset technique introduce series inductance on the secondary side to properly execute and attain this transition and are listed in this topic's Appendix for further information. A third, but remote possibility is that both D1 and D2 conduct half of the load current each. While this will occur at some point during this or the next interval, it's obvious that this condition will not last for long as it might in other topologies and adaptations. Since numerous possibilities exist depending on the exact transformer coupling, circuit parasitics and potential use of external series inductances, it is best to leave this section for a more detailed analysis by the user.

When time t7 is reached, the main switch QA is positioned with zero volts across it due to the active reset technique and resonant circuit elements. The active clamp/reset switch is positioned to its highest amplitude with the full input and clamp voltage across its drain to source terminals. Current flowing is very low and is used to maintain the switches clamped in this position.

CIRCULATION INTERVAL:
Figure 17, t7 < t < t8

This brief interval lasts between the time the main switch is completely positioned with zero volts across it and when it is turned ON at time t8. Basically, this interval is used to accommodate all resonant circuit tolerances, ranges of input voltage and magnetizing current. Very little activity takes



Conditions:					
t =	t7	t8	t =	t7	t8
QA	OFF	→	Qc	OFF	
CA	VCA=0	→	Cc	VCC =VCR +VIN	
DA	ON	→	DC	OFF	
D1	=ON →	I=Io/?	D2	ON →	I=Io/?
VPRI'	=VIN	VIN	IPRI	Increasing →	
IM	Increasing →				

Fig 17. Circulation Interval -- t7 < t < t8

place on the primary side since the last interval, but the previously stated issue of secondary side currents applies to this interval as well. For the most part, the circuit simply "coasts" along until the main switch is re-asserted at time t8, or t0 of the successive switching cycle.

Details of the individual current paths within each of the switches is displayed in Figure 18 and 19.

Practical Design Considerations

There's plenty to gain in efficiency, power density and reduced EMI/RFI by switching a conventional forward converter design to this active clamp/reset technique. For comparison, one place to start is with an existing power supply. Each of the previous items should be measured and characterized for a conclusive, apples-to-apples comparison. What will be required is an additional switch, capacitor, gate drive solution and some control or drive circuitry. One approach is to add these components on a circuit board which can be wired into the existing unit. Advanced driver ICs, for example, the UC3714 and UC3715 are available to and convert a generic PWM input into the two required gate drive outputs. The circuitry used to decipher the two gate drives and timing delays for this, and other ZVT applications are built into these driver ICs which also feature high current, MOSFET compatible gate drive outputs. Although all of the achievable benefits from higher frequency operation may not be realizable with this approach, it offers a quick evaluation of the technique with a minor engineering effort.

ZVT Limitations: As with other Zero Voltage Switching (ZVS), Zero Current Switching (ZCS), Zero Voltage Transitions (ZVT) and Multi-Resonant Converter (MRC) designs, this active reset technique also has limitations because of the resonant tank circuit requirements. As previously stated, the main limitation is the ability to store enough inductive energy in the leakage and magnetizing inductances to overcome the opposing capacitive energy demands of the MOSFET output capacitances. What is favorable, however, is that the peak magnetizing current is constant with the converter in regulation, and so too is the stored inductive energy. The

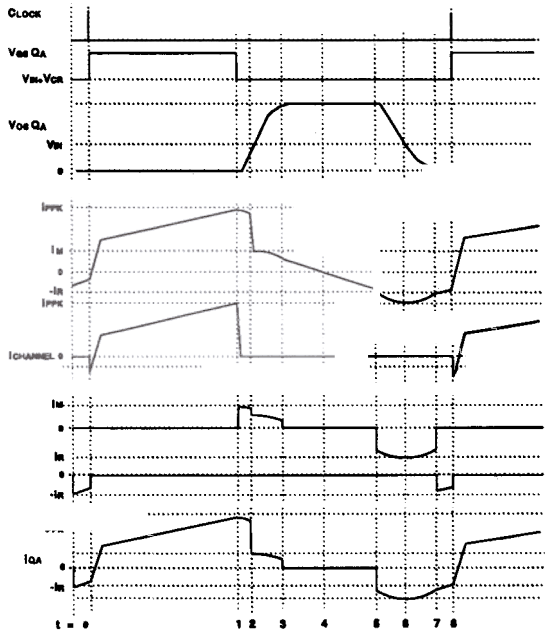


Fig 18. - Main Switch Waveforms (Qa)

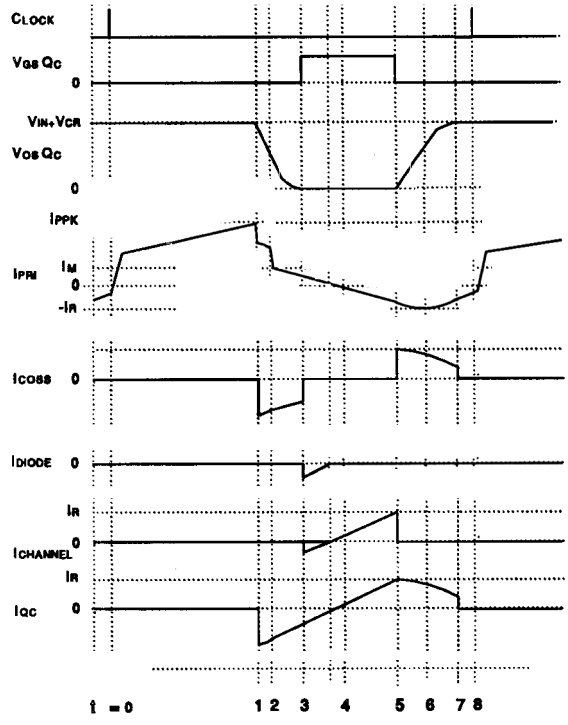


Fig 19. Clamp Switch Waveforms (Qc)

obstructing capacitive load of the switches, and transformer primary is constant as well. Therefore, once designed properly, the circuit will resonate to facilitate the zero voltage transitions over all line and load conditions. This relationship is identified by:

$$Lmag \cdot Imag^2/2 + Llkg \cdot Ipri^2/2 > Cr \cdot (Vin+Vcr)^2/2$$

where Cr is the total resonant capacitance, the parallel combination of the two MOSFET output capacitors in parallel with the transformer primary capacitance

The magnetizing current is totally dependant on the exact transformer design, a function of the ferrite material permeability and number of turns. Leakage inductance is effected by the winding design and technique, and the energy is effected by the output load current (squared) reflected to the primary. This term will go towards zero when the load current decreases, so don't rely on it to make the transitions possible at light load. Magnetizing inductance is the more significant energy term as far as limiting factors are concerned.

B-H Characteristics

One area which is significantly different between the Active clamp/reset technique and its predecessors is found in the transformer's B-H curve operation. In most conventional designs, the transformer is driven in the first quadrant where both H (ampere-turns) and B (flux density) are positive. When the main switch turns off, the transformer resets down the B-H curve back towards the ferrite material's residual flux density, Br. The "negative" voltage across the primary facilitates this reset, and the magnetizing current reduces until it reaches zero. At this point, reset is complete, and this is when the main switch drain voltage will drop to the input voltage, Vin, in a standard design. Operation is primarily limited to the first quadrant of the B-H curve, although any parasitic oscillations could push it into the second quadrant for a brief time. A severe resonance could extent this into the third quadrant, but this is unlikely to occur in most designs because of EMI considerations.

The active reset/clamp technique is significantly different from this description following the driven section of the first quadrant operation. When the main switch turns off, the voltage across the primary reverses, just like the conventional approach. The magnetizing current decreases when the transformer primary voltage reverses, which continues until it's clamped by the clamp/reset capacitor, Cr. Up to this point, the two techniques are the same until the magnetizing current reaches zero.

By design, just prior to the magnetizing current reaching zero the clamp/reset switch is turned on and the device channel is on, and in parallel with the body diode. The stage has now been set for a bidirectional flow of current as opposed to the function of the diode in the conventional type

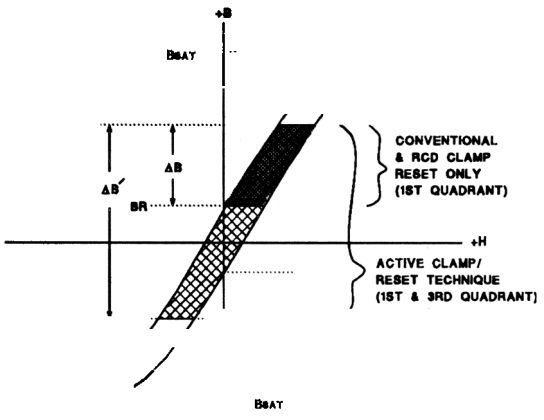


Fig 20. - B-H Curve Differences

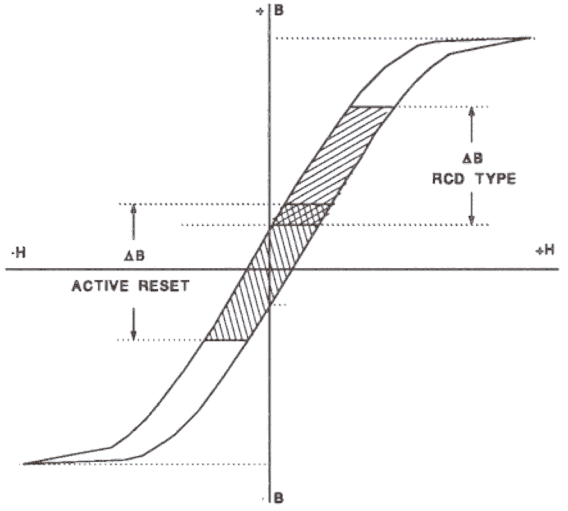


Fig 21. B-H Curve Operational Differences

converters. Now, current reverses and is driven negatively by the clamp voltage applied across the transformer primary, thus driving the core into the second, then third quadrant. Current continues to build while the switch is on, and energy is transferred from the clamp/reset capacitor to the magnetizing inductance. The significant difference with this approach is the ability to drive into the third quadrant, necessary to facilitate the zero voltage transition when later released. A comparison of the B-H characteristics is shown in Figures 20 and 21.

Core Losses and Considerations

This third quadrant operation will **NOT** lead to higher core losses than the conventional designs, despite false, but perceived higher voyage in flux density. Here's why. When the main switch is on, B-H operation is in the upper right handed direction, but usually occurring in the first quadrant only. Whatever amount of change in B, or H took place still does, only it doesn't begin from where it did before at the residual flux density, Br. With the active clamp/reset technique, operation begins from the third quadrant when the main switch is turned on. Normal operation is now centered about the B-H axis origins instead of somewhere in the first quadrant. The net changes in B, and H, are the same, assuming that same volt-second product is applied to the transformer, which is the case to maintain regulation of the output. So delta B, hence core losses are the same, and there is no penalty in core losses for the different mode of operation.

At lower frequencies, or with better core materials where core loss is not the dominant factor, the active reset technique offers the benefit of higher flux density swings. By the operating characteristic just described, the core can now be used at double its first quadrant ability as the total flux density swing encompasses both first and third quadrant operation. Theoretically, it allows complete operation from the negative to positive saturation flux densities, -Bsat to +Bsat, although that's stretching things a bit. Nevertheless, this mode of operation allow reducing the number of turns in each winding by half. Assuming the magnetizing current is negligible in comparison to the load current, this wider operation provides the means to "double-up" on the copper used in each winding and still fit into the existing bobbin window, reducing copper losses.

Semiconductor Stress

Voltage stresses on the primary side power semiconductors are either the same, or lower than in a conventional square wave design. As indicated by the waveforms, the peak voltage is actually reduced in comparison to the standard design and there's no penalty of higher currents as seem in a zero current switched converter, nor higher voltages of the variable frequency, zero voltage switched designs. Conduction losses in the transformer and switch body diode will be slightly higher due to transferring of energy during times where the previous current was zero. However, these losses should be fairly low since the reset magnetizing current is a small percentage of the typical load current. Nothing should be different on the secondary side of the isolation boundary as far as the rectifiers current ratings are concerned, although lower reverse voltage rating is possible.

Increases in Efficiency

The first obvious improvement will be the absence of MOSFET turn-on loss, specifically the one caused by discharging its own output capacitance, CA. The savings realized is:

$$Pcoss(QA) = Coss \cdot Vin^2/2 \cdot Fconv$$

This corresponds to about 3.2 watts saved at high line in an off-line application switching at 250 kHz. For supplies under 100 watts, this amounts to a significant savings.

Power savings can amount to a bit more if an external capacitor was placed in parallel with the MOSFET to reduce turn-off losses. This common design practice slows the voltage rise across the device's terminals which does reduce power loss assuming that the current is the same. One problem with this, however, is what transpires at turn-on of the same switch. Any capacitance across the drain to source is dissipatively discharged by the switch the next time it turns on. This would be eliminated completely with the active reset control technique.

Finally, the elimination of the switching power lost at turn on due to the simultaneous overlap of falling drain voltage and rising drain current will amount to a few watts saved in most designs. Since this loss is dependant on each applications specific power requirements, gate drive and parasitic elements, it becomes difficult to globally quantify. But small as it might be, it does exist and will be eliminated as the resonant tank positions the main switch to zero voltage.

Other Applications

The most likely extension of this technology is for use in the Flyback converter. There will be significant differences in the power waveforms because the flyback is an energy storage technique as opposed to the forward's energy transfer approach. However, the basic power stage schematic and gate drive timing relationships are still applicable.

Summary

Significant advantages in performance and efficiency can be realized with the active clamp/reset technique in comparison to the conventional approach. It does require an additional isolated MOSFET switch and modifications to the control/drive circuitry to accommodate the additional switch and delay times. However, it does open the door to much higher frequency operation with higher efficiency and lower EMI/RFI, ultimately resulting in higher power density. As existing power supply designs are stretched even further for higher power and reduced size and cost, numerous technical obstacles are bound to derail the progression beyond some point. And as this day draws closer, advanced switching technologies like this active clamp/reset technique, and other ZVT adaptations, are destined to command designers' attention.

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