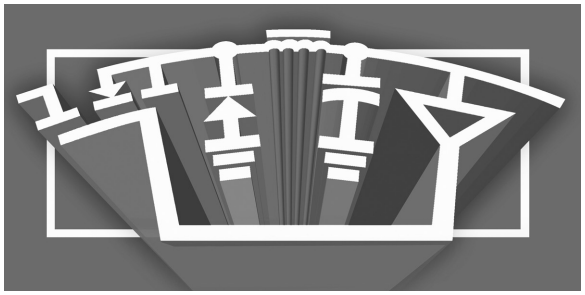


Power Supply Design Seminar

Interleaving Contributes Unique Benefits to Forward and Flyback Converters

Topic Categories:
Specific Power Topologies
Single-Switch Forward
Isolated Flyback Designs
Power Supply Control Techniques

Reproduced from
2004 Texas Instruments Power Supply Design Seminar
SEM1600, Topic 5
TI Literature Number: SLUP231

Power Seminar topics and online power-training modules are available at:
power.ti.com/seminars

Texas Instruments

Interleaving Contributes Unique Benefits to Forward and Flyback Converters

Brian Shaffer

ABSTRACT

A 200-W interleaved forward converter design example illustrates how an interleaved topology can reduce the size and cost of power filtering components and also enhance dynamic load response. In this comprehensive design review, the converter operates from a standard 48-V telecom input voltage and outputs 12 V at 200 W in a half-brick footprint. Operating at a switching frequency of 500 kHz per phase, over 90% efficiency is achieved without the use of synchronous rectifiers. The two-inductor interleaved forward converter is compared against a one inductor interleaved forward converter, a push-pull converter, and a half-bridge converter. A 200-W interleaved flyback converter with an isolated regulated output voltage is also presented. This flyback topology has the potential for operation over the universal AC line voltage range, with the added benefit of achieving a high power-factor input characteristic without additional PFC circuitry.

I. INTRODUCTION

In recent years the usefulness of interleaving power stages has become apparent. The best known application is in powering microprocessors, commonly referred to as voltage regulator modules (VRMs). In VRM applications, the converters are non-isolated from input to output. This paper presents the benefits of interleaving power stages for isolated applications. It shows that the two-inductor (2L) interleaved forward converter topology or the interleaved flyback converter topologies are appropriate choices for many high-power applications.

The forward converter shown in Fig. 1 is one of the most studied topologies. Derived from the simple buck converter, the forward converter delivers energy from the input source to the output filter inductor during the on time of the main switch. In contrast, the flyback converter shown in Fig. 3 delivers energy to the output filter capacitor only during the off-time of the main power switch. This different power transfer characteristic has a dramatic impact on the transfer function and the power levels at which a flyback converter is applicable.

The concept of interleaving enables these converter topologies to operate at increased power levels. The benefits of interleaving include:

- Reduced RMS current in the input capacitors enabling the use of less expensive and fewer input capacitors
- Ripple current cancellation in the output capacitor, enabling the use of less expensive and fewer output capacitors
- Reduction of peak currents in primary and secondary transformer windings (2L interleaved forward converter)
- Improved transient response as a result of reduced output filter inductance and higher output ripple frequency
- Separation of heat generating components allowing for reduced heatsink requirements.
- Improved form factor for low profile solutions
- Reduced EMI as a result of reduced peak currents (2L interleaved forward converter)

II. SINGLE FORWARD CONVERTER

For the single forward converter shown in Fig. 1 the following quantities are evaluated and compared to "1L" or "2L" interleaved forward converters, push-pull converters, and half-bridge converters.

Comparison Quantities:

- Transformer peak currents
- Transformer RMS currents
- Minimum transformer turns ratio
- Input capacitor AC RMS current
- Output inductor peak-to-peak ripple current
- Output capacitor AC RMS current
- Power switch peak voltage
- Output rectifier peak voltage
- Output rectifier peak current.

Table 1 summarizes the equations for the above quantities. In Table 6 these equations are evaluated for a 200 W design example and compared to the results from the other topologies listed above. In Table 7, 500 W design examples are compared.

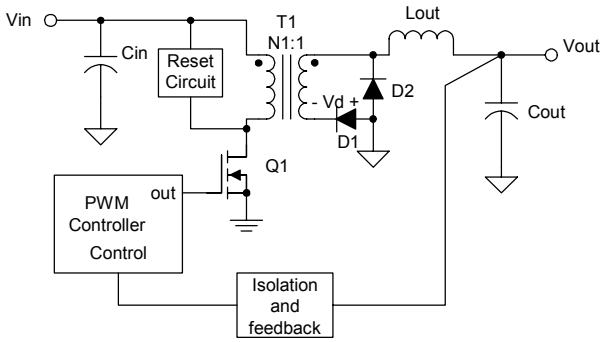


Fig. 1. Single forward converter power stage.

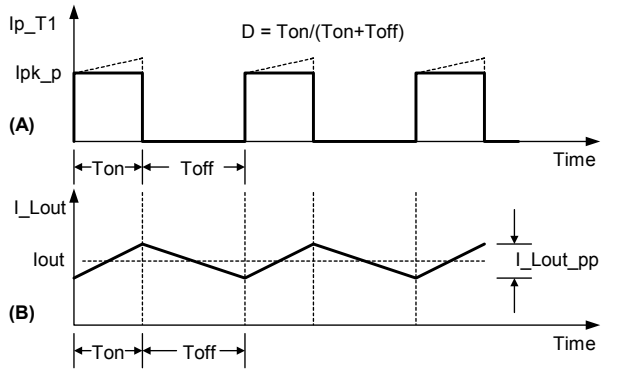


Fig. 2. Forward converter waveforms, (A) Primary transformer current, (B) output inductor current (D = 0.4).

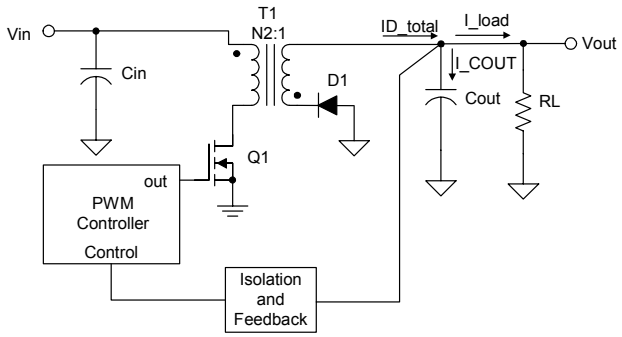


Fig. 3. Single flyback converter.

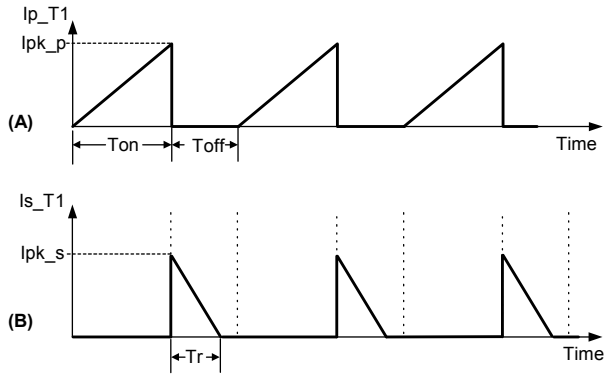


Fig. 4. Flyback converter waveforms, (A) Primary transformer current, (B) secondary transformer current (D = 0.6).

TABLE 1. SINGLE-FORWARD CONVERTER EQUATIONS

Parameter	Single Forward
Ipk_s_T1	Iout
Ipk_p_T1	$\frac{Iout}{N1}$
Irms_s_T1	$Iout * \sqrt{D\max}$
Irms_p_T1	$\frac{Iout}{N1} * \sqrt{D\max}$
Nx_min	$\frac{Vin\_\min * D\max}{Vout + Vd}$
Icin_acrms	$\frac{Iout}{N1} * \sqrt{D * (1 - D)}$
I_Lout_pp	$\frac{(Vout + Vd) * (1 - D\max)}{Lout * Fs}$
Icout_acrms	$\frac{I\_Lout\_pp}{2} * \sqrt{\frac{1}{3}}$
Vpk_Q1	$\frac{Vin\_\min}{1 - D\max}$ or $\frac{Vin\_\max}{1 - D\min}$
Vpk_D1	$Vin\_\min * \frac{D\_\max}{1 - D\_\max} * \frac{1}{N1}$
Vpk_D2	$\frac{Vin\_\max}{N1}$
Ipk_D1	Iout

III. INTERLEAVED FORWARD CONVERTERS

Fig. 5 contains a representation of two power stages in an interleaved configuration where two output inductors (2L) are used which allows the duty cycle of each power stage to go above fifty percent. This is beneficial in many reset techniques presently being used today such as, resonant reset, RCD clamps, or active reset techniques. By allowing the duty cycle of the converter to be centered around 50%, it is possible to minimize the AC RMS ripple currents in the input and output capacitors at the expense of higher peak voltages on the power switches. This leads to a fewer number of and less expensive input and output capacitors. In general, semiconductor devices are more reliable and cost effective than capacitors, so the increased voltage stress on the power switches and output rectifiers is considered desirable when compared to having more expense and a lager number of input and output capacitors. Fig. 7 depicts an alternative configuration for interleaved forward converters where only one output inductor (1L) is required. It is shown that the 1L topology has higher peak and RMS transformer currents than the 2L topology.

In Fig. 5 the term “phase” is defined as any one of the individual power stages in the interleaved configuration. Fig. 6 contains the operating waveforms for the 2L interleaved forward converter of Fig. 5 operating at a duty cycle of 0.4. By examining Fig. 6 it becomes clear how to write the expressions for the input and output capacitor ripple currents when the duty cycle of each phase is less than or equal to 0.5 or one divided by x (1/x) where x is the number of phases being interleaved. The effect of interleaving on the duty cycle is to increase the effective duty cycle by the number of phases in the circuit and reduce the peak current by the same factor. In Fig. 5 there are two phases so the effective duty cycle is increased by a factor of two and the peak currents are reduced by the same amount. Another way of describing this phenomenon is to realize that the frequency of the input and output currents are increased by a factor of two over the switching frequency of each individual phase and the power throughput of each phase is inversely proportional to the number of phases.

For the interleaved forward converters shown in Figs. 5 and 7 the same quantities that were evaluated for the single forward converter are again evaluated and used to compare these interleaved converters against each other and to push-pull converters, or half-bridge converters.

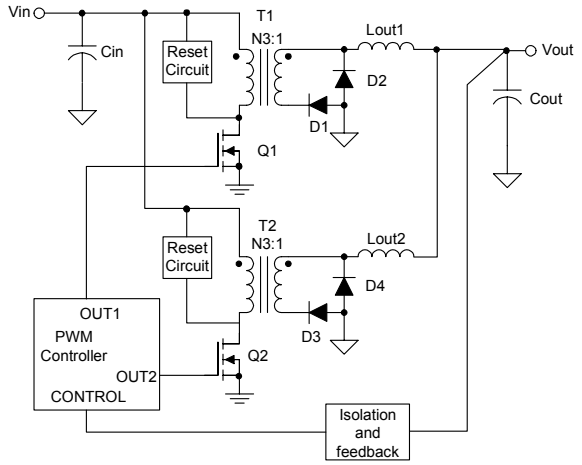


Fig. 5. "2L" interleaved forward converter (Dmax ≥ 0.5).

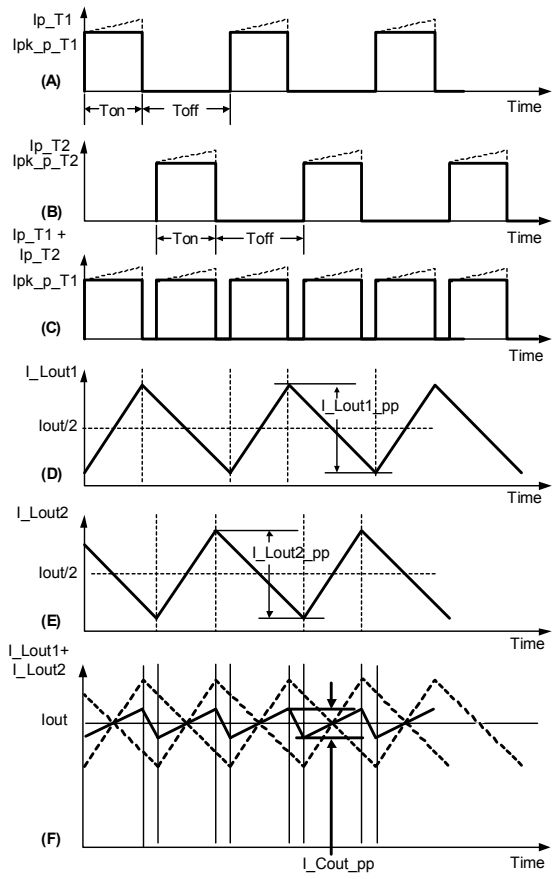


Fig. 6. 2L interleaved forward waveforms, D = 0.4 (A) Primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms (A) and (B) seen at the input capacitor, (D) output inductor current of phase 1, (E) output inductor current of phase 2, (F) sum of output inductor currents.

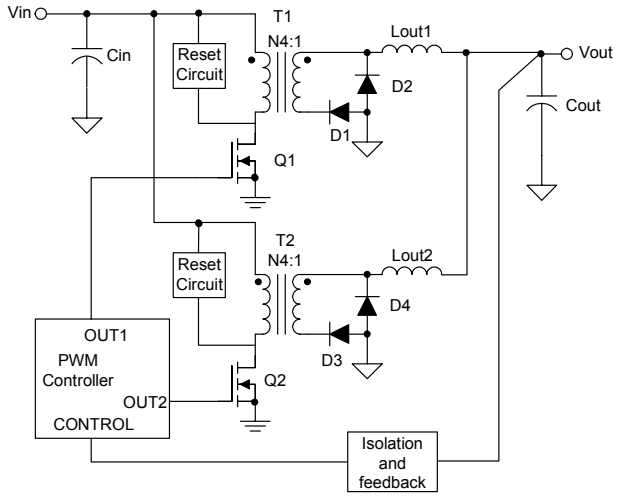


Fig. 7. "1L" interleaved forward converter (Dmax < 0.5).

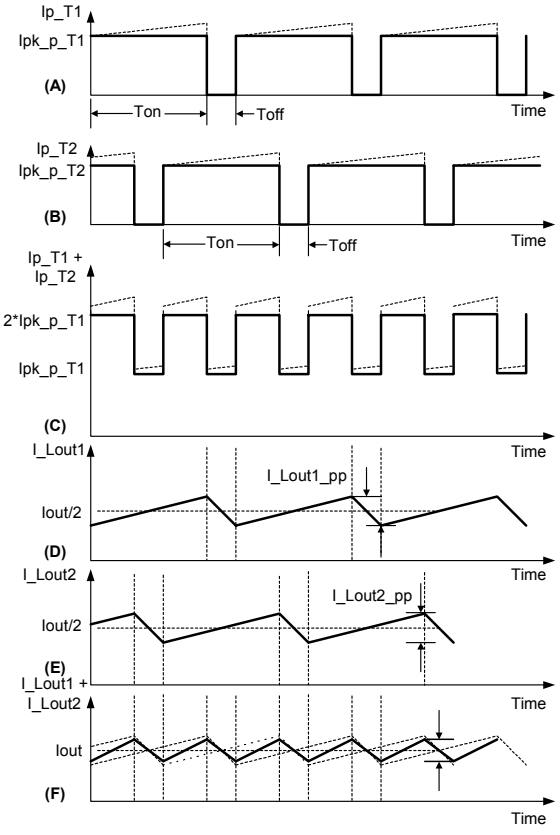


Fig. 8. 2L interleaved forward waveforms, D = 0.8, (A) Primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms (A) and (B) seen at the input capacitor, (D) output inductor current of phase 1, (E) output inductor current of phase 2, (F) sum of output inductor currents.

Interleaved Forward Converter with Two Output Inductors (2L)

Primary and Secondary Transformer Windings Peak Currents (D ≤ 0.5)

In Fig. 5, the peak secondary current, Ipk_s_T1, is cut in half for two phases.

$$Ipk\_s\_T1 = \frac{Iout}{2}$$

The peak current in the primary winding is then calculated by transforming the secondary current to the primary winding, by dividing it by the turns ratio of the transformer.

$$Ipk\_p\_T1 = \frac{Ipk\_s\_T1}{N3} = \frac{Iout}{2*N3}$$

Transformer RMS Currents (D ≤ 0.5)

The equivalent RMS current of the waveform in Fig. 6A, Irms_p_T1, equals:

$$Irms\_p\_T1 = Ipk\_p\_T1 * \sqrt{D}$$
$$= \frac{Iout}{2*N3} * \sqrt{D}$$

The secondary winding RMS current is then,

$$Irms\_s\_T1 = \frac{Iout}{2} * \sqrt{D}$$

Minimum Transformer Turns Ratio

The equation for calculating the turns ratio for the 2L interleaved forward converter is no different than that for the single forward converter. In the following equation and throughout this paper the quantity Dmax represents the maximum duty cycle of each phase. In the cases where the effective duty cycle is a multiple of the number of phases, a multiplier is added to the equation.

$$N3\_\min = \frac{Vin\_\min * D\max}{Vout + Vd}$$

Input Capacitor AC RMS Current (D ≤ 0.5)

The AC RMS current in the input capacitors is calculated for two different operating conditions. The initial analysis that follows presents the equations for the case where the maximum duty cycle of each phase is less than 0.5 and then, the case where the duty cycle is greater than 0.5 is presented in a later section. For the following calculations refer to Fig. 6C, which is the summation of the input current waveforms in the primary of transformers T1 and T2. In general, the AC RMS current in the input capacitor as a result of the transformer's input current waveform is:

$$Iacrms = \sqrt{Irms^2 - Idc^2}$$

where Irms = The RMS equivalent of the transformer current – [A]

Idc = The DC equivalent of the transformer current – [A]

hence,

$$Icin\_acrms$$
$$= Ipk\_p\_T1 * \sqrt{2*D*(1-2*D)}$$

$$Icin\_acrms$$
$$= \frac{Iout}{2*N3} * \sqrt{2*D*(1-2*D)}$$

Output Inductor Peak-to-Peak Ripple Current (D ≤ 0.5)

The output inductor ripple current for each of the phases is calculated in the same manner as with a single forward converter. By factoring in the off time and the output voltage the peak-to-peak ripple current for each output inductor is given by:

$$I\_Lout\_pp = \frac{(Vout + Vd) * (1 - D)}{Lout * Fs}$$

where, Lout = Lout1 = Lout2

Fs = The switching frequency of each phase in Hertz

Output Capacitor AC RMS Current (D ≤ 0.5)

The following discussion refers to Fig. 6F, which is the sum of the individual output inductor ripple currents shown in Figs 6D and 6E. Assuming that each of the phases is 360/x degrees offset from one another with equal duty cycles the effective duty cycle of the summed inductor current waveform is x times the individual duty cycle of each phase. The output capacitors are exposed to this summed current waveform and the resultant AC RMS current is the portion of the waveform that causes heating in the output capacitors. The peak-to-peak ripple current of the summed inductor current waveform is expressed by the following equation.

$$ILout\_total\_pp = \frac{(Vout + Vd) * (1 - 2 * D)}{Lout * Fs}$$

The AC ripple current in the output capacitors for the 2L interleaved forward topology, Icout_acrms, is then:

$$Icout\_acrms = \frac{ILout\_total\_pp}{2} * \sqrt{\frac{1}{3}}$$

Output Capacitor RMS Ripple Current Cancellation (D ≤ 0.5)

Taking the ratio of the output capacitor AC RMS current in the 2L interleaved case and the AC RMS current of the single forward converter reveals an important reason why interleaving is beneficial. For all values of D less than 0.5, the following equation is less than one which means that the peak-to-peak ripple current seen by the output capacitors is less than the non-interleaved case. The same is true for the cases where D > 0.5.

$$\frac{Icout\_acrms\_2L}{Icout\_acrms\_FWD} = \frac{1 - 2 * D}{1 - D}$$

Power Switch Peak Voltage

The peak voltage on the power switch is a result from the requirement that the volt second product on the primary transformer winding average to zero. The longer the on-time the more negative the reset voltage must be in order to maintain a volt second balance. Assuming that the reset voltage is a square wave and that the reset voltage is present throughout the entire off time of the main switch, the volt second balance equation is expressed as:

$$Vin * D - Vreset * (1 - D) = 0$$

$$Vreset = \frac{Vin * D}{1 - D}$$

From Fig. 5, the peak voltage on the power switch, Vpk_Q1 is equal to the sum of the input voltage and the reset voltage.

$$Vpk\_Q1 = Vin + \frac{Vin * D}{1 - D} = \frac{Vin}{1 - D}$$

Fig. 9, Vpk_Q1/Vin, depicts the penalty that is paid as the duty cycle is increased. When the duty cycle has reached 0.5 the peak voltage on the switch is equal to twice the input voltage.

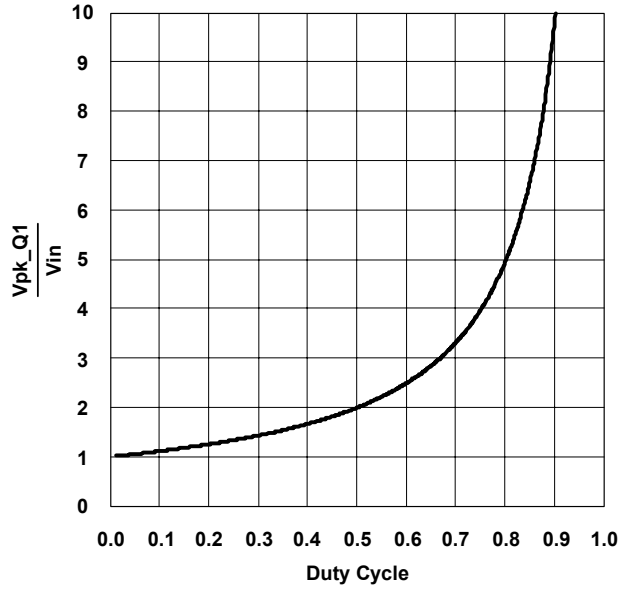


Fig. 9. Normalized peak voltage on the main switch vs. duty cycle.

Fig. 9 which shows the normalized peak voltage on the main switch applies to interleaved converters as well as non-interleaved converters. In Fig. 5 where the duty cycle is allowed to go above 0.5, it is expected that the peak voltage on the main switch is greater than that seen by the main switch for the complementary design using Fig. 7. For example, consider the case where the maximum duty cycle for the 2L design is allowed to go to 0.8 and the corresponding maximum duty cycle for the 1L design is limited to 0.4, then the peak voltage on the switch in the 2L design is 2.86 (5/1.75) times greater than that for the 1L design. The drawback in peak voltage stress for designs using the 2L configuration is immediately obvious, but the reduction in the input and output capacitor AC RMS currents outweighs this disadvantage.

Output Rectifier Peak Voltage and Current

The peak voltage on the output rectifiers in the 2L interleaved case is given by,

$$Vpk\_D1 = \frac{Vin * D}{1 - D} * \frac{1}{N3}$$

The peak current in the output rectifiers for the 2L interleaved forward configuration is equal to one half of the load current because the output current is made up of the sum of the individual phase currents.

Transformer RMS Currents (D > 0.5)

In the 2L interleaved flyback converter, the equations for determining the RMS current in the transformer windings when the duty cycle is greater than 0.5 are the same as the case where the maximum duty cycle is less than 0.5. The RMS current in the transformer windings increases proportionally to the square root of the increase in duty cycle. For example, a doubling in the maximum duty cycle only increases the RMS current in the winding by forty-one percent. This increase is offset by the reduction in AC RMS current in the input and output capacitors. Because the failure rate of capacitors due to overheating is much more of a concern than heat in a magnetic component, the tradeoff of increased RMS current in the transformer for a reduction in AC RMS currents in the input and output capacitors is worthwhile.

Input Capacitor RMS Current (D > 0.5)

As was stated earlier, the circuit configuration of Fig. 5 is allowed to go above 50% duty cycle. In such an operating mode, the equations for determining the input and output ripple currents change slightly. Referring to Fig. 8, the total RMS equivalent current of the waveform in Fig. 8(C), Iin_rms, equals:

$$Iin\_rms = Ipk\_p\_T1 * \sqrt{2 * (D - 0.5)} + Ipk\_p\_T1$$

The DC equivalent current of the current waveform in Fig. 8(C), Iin_dc, equals:

$$Iin\_dc = Ipk\_p\_T1 * (2 * (D - 0.5)) + Ipk\_p\_T1$$

The AC RMS current in the input capacitor as a result of the transformer's input current waveform is then:

$$Icin\_acrms = Ipk\_p\_T1 * \sqrt{4 * (D - 0.5) * (1 - D)}$$

Substituting Ipk_p_T1 from above yields:

$$Icin\_acrms = \frac{Iout}{2 * N3} * \sqrt{4 * (D - 0.5) * (1 - D)}$$

Fig. 10 depicts the normalized AC RMS input current for the circuit shown in Fig. 5 for duty cycles from zero to one. The normalization factor defines the AC RMS current in the input capacitors as a function of the peak current in the primary windings, Iout/(2xN3).

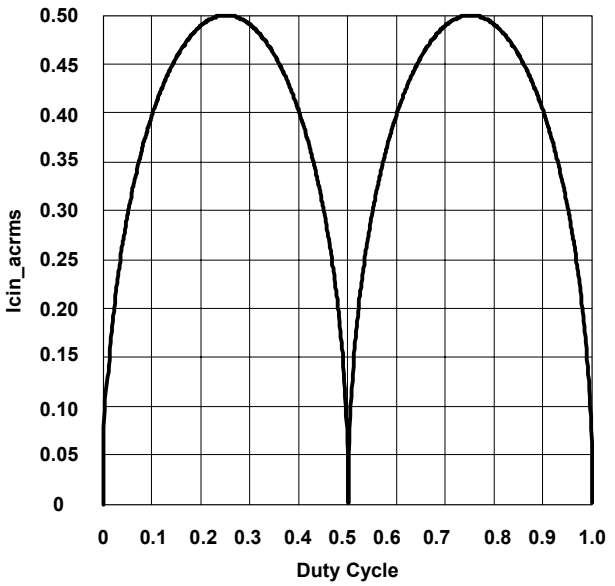


Fig. 10. Normalized AC RMS ripple current seen by the input capacitor vs. duty cycle.

Output Inductor Ripple Current (D > 0.5)

The equation for determining the individual phase ripple current is not changed from the case where the maximum duty cycle is limited to 0.5. It is still directly proportional to the output voltage and off time and inversely proportional to the value of the output inductor.

Output Capacitor RMS Ripple Current (D > 0.5)

In order to develop the expression for the output capacitor ripple current it must first be understand how the output inductor ripple currents sum for this case where the duty cycle is allowed to be greater than 0.5. The summation of the individual output inductor phase currents, which is the total peak-to-peak ripple current in the output capacitor as a function of duty cycle is given by the following equation [9]:

$$ILout\_total\_pp = (I\_Lout\_pp) * (KI)$$

$$I\_Lout\_pp = \frac{(Vout + Vd) * (1 - D)}{Lout * Fs}$$

$$KI = \frac{x * \left(D - \frac{m}{x}\right) * \left(\frac{m+1}{x} - D\right)}{D * (1 - D)}$$

where x = number of phases (2 for our example)

m = floor(x*D) is the maximum integer that does not exceed the product of x and D.

I_Lout_pp = peak-to-peak inductor ripple current in each phase. [A]

KI = cancellation effect of interleaving on the individual peak-to-peak inductor ripple current.

Normalizing the equation for ILout_total_pp to the amount of ripple current per phase gives the cancellation effect, KI that is present as a result of interleaving power stages at various operating duty cycles.

For x = 2,

$$KI = \begin{cases} \dfrac{(1-2D)}{1-D} \; if \; D \le 0.5 \\ \dfrac{(2D-1)}{D} \; if \; D > 0.5 \end{cases}$$

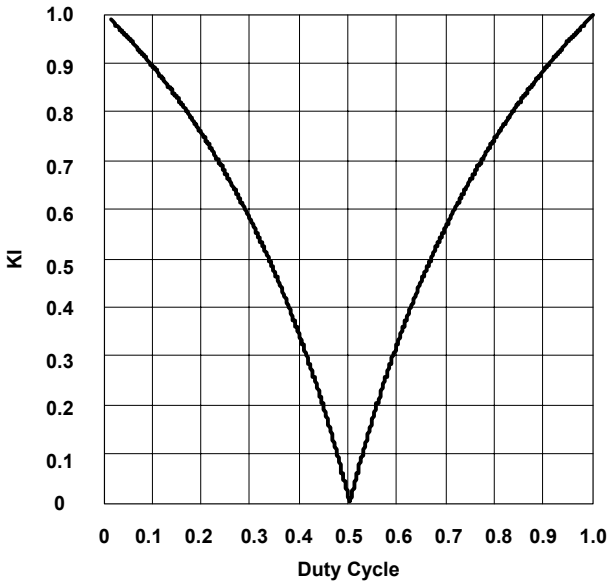


Fig. 11. Cancellation effect on output capacitor ripple current normalized to the ripple current of a single phase vs. duty cycle.

By examining the preceding graphs for the entire range of possible duty cycles, it becomes clear that the optimal operating point for each phase is at a duty cycle equal to one divided by the number of phases with a phase relation of 360 degrees divided by x (360/x). The optimal operating point is not always achievable given a wide input range and semiconductor limitations, but the closer the circuit operates near the optimal point the lower the RMS currents in the input and output capacitors will be. At any operating point, Fig. 11 is used to determine the actual amount of peak-to-peak ripple current in the output capacitors given the peak-to-peak ripple current of each individual phase and the operating duty cycle. Because the current waveform after the summation of the individual ripple currents is still a triangle wave, the AC RMS component which flows through the output capacitor is calculated as follows:

$$Icout\_acrms = \frac{ILout\_total\_pp}{2} * \sqrt{\frac{1}{3}}$$

Power Switch Peak Voltage (D > 0.5)

The equation for determining the peak voltage on the power switches is the same as for the single case and the condition where the duty cycle is less than 0.5.

Output Rectifier Peak Voltage (D > 0.5)

The equation for determining the peak voltage on the output rectifiers is the same as for the single case.

Output Rectifiers Peak Current (D > 0.5)

The peak current in the output rectifiers does not change as a function of duty cycle. It is still equal to half of the load current.

Appendix B contains the empirical circuit waveforms for a 200-W 2L interleaved forward converter design. Figs B7, B8, and B9 demonstrate the ripple current cancellation effect with two interleaved power stages. Figs. B10 and B11 show the improvement in the output transient response which is achievable by interleaving power stages.

A. Interleaved Forward Converter with One Output Inductor (1L)

The circuit configuration in Fig. 7 does not allow for an operating duty cycle greater than 0.5. As a result D4 and Lout2 are removable from Fig. 5 provided that the secondary of T2 is connected to the input side of the remaining output inductor. If the duty cycle were to go above 0.5 in Fig. 7, the forward diodes D1 and D3 would create a short across the secondary of the transformers. With the removal of D4 and Lout2 the resultant peak secondary transformer current is now equal to the full load current. The current waveforms for the 1L configuration are depicted in Fig. 12. Table 3 summarizes the equations that are used in Table 6 to compare the 1L interleaved forward converter to the other topologies listed in this paper.

TABLE 2. "2L" INTERLEAVED FORWARD CONVERTER EQUATIONS

Parameter	Interleaved Forward (2L)
Ipk_s_T1	$\frac{Iout}{2}$
Ipk_p_T1	$\frac{Iout}{2*N3}$
Irms_s_T1	$\frac{Iout}{2}*\sqrt{D\max}$
Irms_p_T1	$\frac{Iout}{2*N3}*\sqrt{D\max}$
Nx_min	$\frac{Vin\_\min * D\max}{Vout+Vd}$
Icin_acrms	D ≤ 0.5; $\frac{Iout}{2*N3}*\sqrt{2*D*(1-2*D)}$ D>0.5; $\frac{Iout}{2*N3}*\sqrt{4*(D-0.5)*(1-D)}$
I_Lout_pp	$\frac{(Vout+Vd)*(1-D\max)}{Lout*Fs}$
ILout_total-pp	$\frac{(Vout+Vd)*(1-D)}{Lout*Fs} * \frac{2*\left(D-\frac{m}{2}\right)*\left(\frac{m+1}{2}-D\right)}{D*(1-D)}$ *where* $m = floor\,(2*D)$
Icout_acrms	$\frac{ILout\_total\_pp}{2}*\sqrt{\frac{1}{3}}$
Vpk_Q1	$\frac{Vin\_\min}{1-D\max}$ or $\frac{Vin\_\max}{1-D\min}$
Vpk_D1	$Vin\_\min * \frac{D\_\max}{1-D\_\max} * \frac{1}{N3}$
Vpk_D2	$\frac{Vin\_\max}{N3}$
Ipk_D1	$\frac{Iout}{2}$

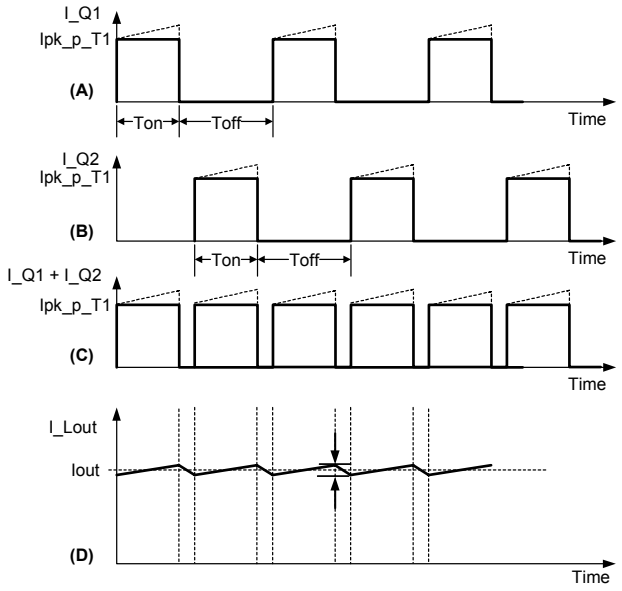


Fig. 12. 1L interleaved forward converter waveforms (A) primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms "a" and "b" seen at the input capacitor, (D) output inductor current (D = 0.4).

Comparison of 2L and 1L Transformer RMS Currents

One major benefit of using two output inductors as opposed to one output inductor is that the resulting RMS currents in the transformers are significantly reduced. Consider the following comparison:

2L primary input RMS current:

$$Irms\_p\_T1\_2L = \frac{Iout}{2*N3} * \sqrt{D\max\_2L}$$

1L primary input RMS current:

$$Irms\_p\_T1\_1L = \frac{Iout}{N4} * \sqrt{D\max\_1L}$$

Ratio of 2L RMS transformer current to 1L RMS transformer current:

$$\frac{Irms\_p\_T1\_2L}{Irms\_p\_T1\_1L} = \frac{1}{2} * \frac{N4}{N3}\sqrt{\frac{D\max\_2L}{D\max\_1L}}$$

As a specific example, consider the case where the load current is equal in both circuits and the duty cycle for the 2L power stages is 0.8 with the duty cycle for the 1L power stages equal to 0.4. In this example the turns ratio, Nx_min, for each of the transformers is equal, then:

$$\frac{Irms\_p\_T1\_2L}{Irms\_p\_T1\_1L} = \frac{1}{\sqrt{2}}$$

By configuring the circuit with two output inductors it allows operating duty cycles of greater than 50%, reducing the RMS currents in the transformer by a factor of the square root of two, and reduces the conducted EMI produced because the peak currents are reduced.

TABLE 3. "1L" INTERLEAVED FORWARD CONVERTER EQUATIONS

Parameter	Interleaved Forward (1L)
Ipk_s_T1	$Iout$
Ipk_p_T1	$\frac{Iout}{N4}$
Irms_s_T1	$Iout * \sqrt{D\max}$
Irms_p_T1	$\frac{Iout}{N4} * \sqrt{D\max}$
Nx_min	$\frac{Vin\_\min * 2 * D\max}{Vout + Vd}$
Icin_acrms	$\frac{Iout}{N4} * \sqrt{2 * D * (1 - 2 * D)}$
I_Lout_pp	$\frac{(Vout + Vd) * (1 - 2 * D\max)}{Lout * Fs}$
Icout_acrms	$\frac{I\_Lout\_pp}{2} * \sqrt{\frac{1}{3}}$
Vpk_Q1	$\frac{Vin\_\min}{1 - D\max}$ or $\frac{Vin\_\max}{1 - D\min}$
Vpk_D1	$\frac{Vin}{N4} * \frac{1}{1 - D\_\max}$
Ipk_D1	$Iout$

Summary of 2L vs. 1L Interleaved Forward Converters

Advantages of 2L interleaved forward topology vs. 1L interleaved forward topology:

- Reduced transformer peak currents
- Reduced RMS transformer currents by $\sqrt{2}$
- Reduced transformer heating by a factor of 2
- Reduced input capacitor RMS currents
- Reduced output capacitor RMS currents
- Reduced inductor currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward topology vs. 1L interleaved forward topology:

- Increased component count
- Possible increase in area of components
- Increased peak voltage stress on primary switch when duty cycle is greater than 0.5
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

B. Push-Pull Circuit Topology

Fig. 13 shows a push-pull converter. In general, a push-pull converter would be considered for the same applications as the interleaved forward converter. The same quantities as defined above are presented here for the push-pull topology and are used to identify the drawbacks of the push-pull converter when being compared to the 2L interleaved forward converter. For the push-pull topology the maximum duty cycle for each switch is limited to 0.5 in order to avoid cross conduction between the switches. Typical waveforms for the push-pull topology are depicted in Fig. 14. Table 4 summarizes the equations for the push-pull topology.

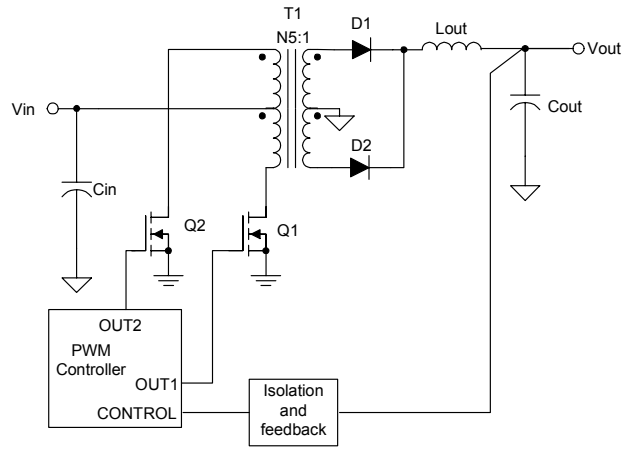


Fig. 13. Push-pull converter.

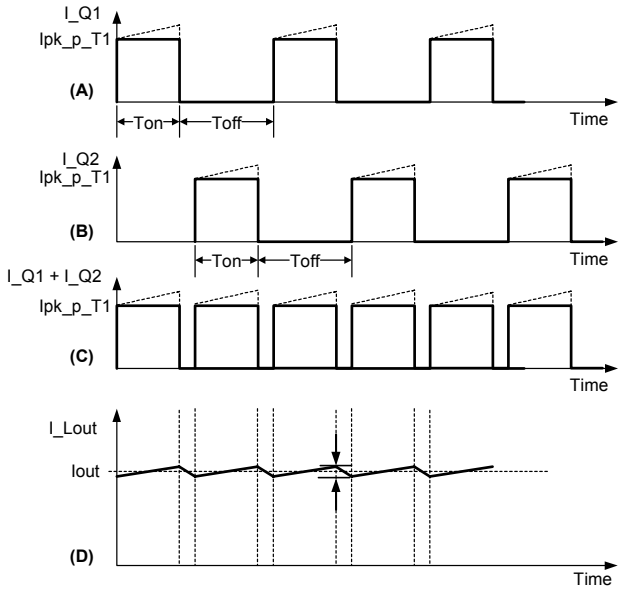


Fig. 14. Waveforms for push-pull converter (D = 0.4).

TABLE 4. PUSH-PULL CONVERTER EQUATIONS

Parameter	Push Pull
Ipk_s_T1	$Iout$
Ipk_p_T1	$\frac{Iout}{N5}$
Irms_s_T1	$Iout * \sqrt{D\max} + \frac{Iout}{2} * \sqrt{1 - 2 * D\max}$
Irms_p_T1	$\frac{Iout}{N5} * \sqrt{D\max}$
Nx_min	$\frac{Vin\_\min * 2 * D\max}{Vout + Vd}$
Icin_acrms	$\frac{Iout}{N5} * \sqrt{2 * D\max * (1 - 2 * D\max)}$
I_Lout_pp	$\frac{(Vout + Vd) * (1 - 2 * D\max)}{Lout * Fs}$
Icout_acrms	$\frac{I\_Lout\_pp}{2} * \sqrt{\frac{1}{3}}$
Vpk_Q1	$2 * Vin\_\max$
Vpk_D1	$\frac{2 * Vin\_\max}{N5}$
Vpk_D2	$\frac{2 * Vin\_\max}{N5}$
Ipk_D1	$Iout$

Summary of Push-Pull vs. 2L Interleaved Forward Converter

Advantages of 2L interleaved forward converter vs. push-pull topology:

- Reduced transformer peak currents
- Reduced transformer RMS secondary current
- Reduced peak voltage stress on primary switches
- Reduced peak voltage stress on output rectifiers
- Reduced inductor currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward converter vs. push-pull topology:

- Increased component count
- Possible increase in area of components
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

C. Half-Bridge Circuit Topology

The main benefit of the half-bridge topology over the previous topologies is that the peak voltage on the power switches is only equal to the input voltage. Referring to Fig. 15, the same quantities listed above are compared against the 2L interleaved forward converter. In the half-bridge topology the maximum duty cycle for each switch is limited to 0.5 in order to avoid cross conduction between the switches. Typical waveforms for the half-bridge topology are depicted in Fig. 16. Table 5 summarizes the equations for the half-bridge topology.

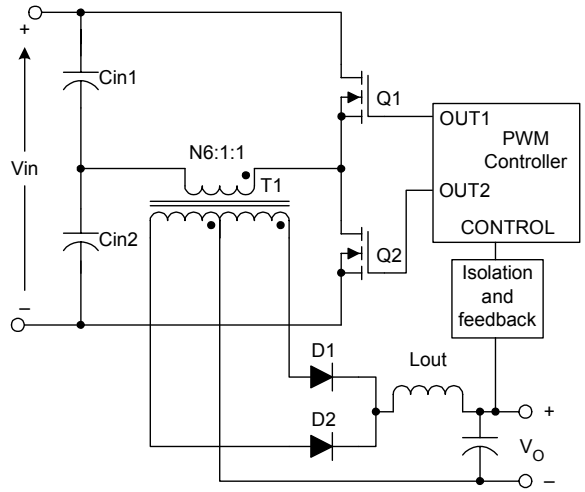


Fig. 15. Half-bridge converter.

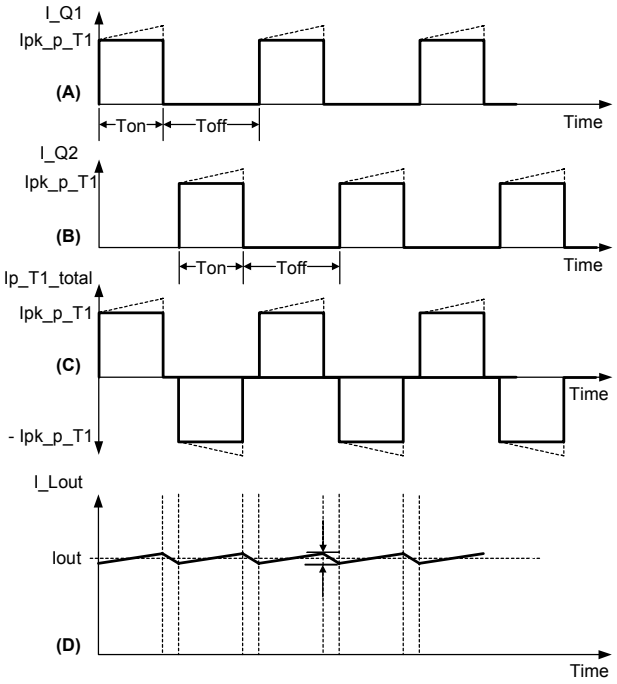


Fig. 16. Waveforms for half-bridge converter power stage (D = 0.4).

TABLE 5. HALF-BRIDGE CONVERTER EQUATIONS

Parameter	Half Bridge
Ipk_s_T1	$Iout$
Ipk_p_T1	$\frac{Iout}{N6}$
Irms_s_T1	$Iout * \sqrt{D\max} + \frac{Iout}{2} * \sqrt{1-2*D}$
Irms_p_T1	$\frac{Iout}{N6} * \sqrt{2*D\max}$
Nx_min	$\frac{\frac{Vin\_\min}{2} * 2 * D\max}{Vout + Vd}$
Icin_acrms	$\frac{Iout}{N6} * \sqrt{D\max * (1-D\max)}$
I_Lout_pp	$\frac{(Vout + Vd) * (1-2*D\max)}{Lout * Fs}$
Icout_acrms	$\frac{I\_Lout\_pp}{2} * \sqrt{\frac{1}{3}}$
Vpk_Q1	$Vin\_\max$
Vpk_D1	$\frac{Vin\_\max}{N6}$
Vpk_D2	$\frac{Vin\_\max}{N6}$
Ipk_D1	$Iout$

Summary of HB vs. 2L Interleaved Forward Converter

Advantages of 2L interleaved forward converter vs. half-bridge topology:

- Reduced transformer peak currents
- Reduced transformer RMS currents
- Reduction of EMI energy due to lower peak currents
- Reduced peak voltage stress on output rectifiers
- Reduction of EMI energy at higher frequencies due to longer allowable on times
- Reduced inductor currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward converter vs. half-bridge topology:

- Increased component count
- Increased peak voltage stress on primary switches
- Possible increase in area of components
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

Table 6 contains 200-W design examples for each of the buck derived topologies and Table 7 contains 500-W design examples. The following assumptions were made:

- The output inductance values are equal for all topologies (2L output inductors carry only half the load current).
- The duty cycle for the 1L interleaved forward converter is ½ of that for the 2L interleaved forward converter
- The switching frequency is equal to 500 kHz
- The input range is 36 Vdc – 75 Vdc
- The output voltage is 12 V for all topologies.

TABLE 6. COMPARISON TABLE FOR 200-W DESIGN EXAMPLES

200 W	Topology				
Parameter	**Forward**	**Interleaved Forward (2L)**	**Interleaved Forward (1L)**	**Push Pull**	**Half Bridge**
Dmax	0.52	0.52	0.26	0.45	0.45
Lout – (µH)	3.20	3.20	3.20	3.20	3.20
Ipk_s_T1 – (A)	16.7	8.3	16.7	16.7	16.7
Ipk_p_T1 – (A)	11.6	5.8	11.6	6.7	13.4
Irms_s_T1 – (A)	12.0	6.0	8.5	13.8	13.8
Irms_p_T1 – (A)	8.3	4.2	5.9	4.5	12.7
Nx_min	1.44	1.44	1.44	2.49	1.25
Icin_acrms – (A)	5.8	1.1	5.8	2.0	6.7
I_Lout_pp – (A)	3.9	3.9	3.9	0.8	0.8
Ilout_total_pp – (A)	N/A	0.3	N/A	N/A	N/A
Icout_acrms – (A)	1.1	0.1	1.1	0.2	0.2
Vpk_Q1 – (V)	75.0	75.0	48.6	150.0	75.0
Vpk_D1 – (V)	27.1	27.1	33.8	60.2	60.2
Vpk_D2 – (V)	52.1	52.1	52.1	60.2	60.2
Ipk_D1 – (A)	16.7	8.3	16.7	16.7	16.7

TABLE 7. COMPARISON TABLE FOR 500-W DESIGN EXAMPLES

500 W	Topology				
Parameter	**Forward**	**Interleaved Forward (2L)**	**Interleaved Forward (1L)**	**Push Pull**	**Half Bridge**
Dmax	0.52	0.52	0.45	0.45	0.45
Lout – (µH)	3.20	3.20	3.20	3.20	3.20
Ipk_s_T1 – (A)	41.7	20.8	41.7	41.7	41.7
Ipk_p_T1 – (A)	28.9	14.5	16.7	16.7	33.4
Irms_s_T1 – (A)	30.0	15.0	28.0	34.5	34.5
Irms_p_T1 – (A)	20.9	10.4	11.2	11.2	31.7
Nx_min	1.44	1.44	2.49	2.49	1.25
Icin_acrms – (A)	14.5	2.8	5.0	5.0	16.6
I_Lout_pp – (A)	3.9	3.9	0.8	0.8	0.8
Ilout_total_pp – (A)	N/A	0.3	N/A	N/A	N/A
Icout_acrms – (A)	1.1	0.1	0.2	0.2	0.2
Vpk_Q1 – (V)	75.0	75.0	65.5	150.0	75.0
Vpk_D1 – (V)	27.1	27.1	26.3	60.2	60.2
Vpk_D2 – (V)	52.1	52.1	30.1	60.2	60.2
Ipk_D1 – (A)	41.7	20.8	41.7	41.7	41.7
For this example the max duty cycle for the 1L interleaved forward converter was increased to 0.45.					

IV. SINGLE FLYBACK CONVERTER IN DISCONTINUOUS CONDUCTION MODE (DCM)

Fig. 3 shows a single flyback converter. Table 8 summarizes the design equations that are used to compare it against its interleaved counterpart shown in Fig. 17. More detail on how to derive these equations is given in the following section dealing with the interleaved flyback topology.

TABLE 8. SINGLE FLYBACK CONVERTER EQUATIONS

Parameter	Flyback
Ipk_s_T1	$N2 * Ipk\_p\_T1$
Ipk_p_T1	$\frac{Vin\_\min * Ton\_\max}{Lp}$
Irms_s_T1	$N2 * Ipk\_p\_T1 * \sqrt{\left(\frac{Tr}{3 * Ts}\right)}$
Irms_p_T1	$Ipk\_p\_T1 * \sqrt{\left(\frac{D}{3}\right)}$
Nx_min	$\frac{Vpk\_Q1 - Vin\_\max}{Vout + Vd}$
Icin_acrms	$Ipk\_p\_T1 * \sqrt{\left(\frac{D}{3}\right) * \left(1 - \frac{3 * D}{4}\right)}$
Icout_acrms	$N2 * Ipk\_p\_T1 * \sqrt{\left(\frac{Tr}{3 * Ts}\right) * \left(1 - \frac{3 * Tr}{4 * Ts}\right)}$
Vpk_Q1	$Vin\_\max + N2 * (Vout + Vd)$
Vpk_D1	$\frac{Vin\_\max}{N2} + Vspike$
Ipk_D1	$N2 * Ipk\_p\_T1$

D. Interleaved DCM Flyback Converter

The circuit depicted in Fig. 17 is an interleaved flyback converter. The duty cycle for each phase of an interleaved flyback is not limited to less than 50% because the secondaries inherently have high output impedance and resemble a current source. Fig. 18 shows the input and output ripple currents and their intended overlap at an individual phase duty cycle of 60 percent. This section and the following example show that the interleaved flyback converter is applicable to power levels twice as high as the single flyback converter.

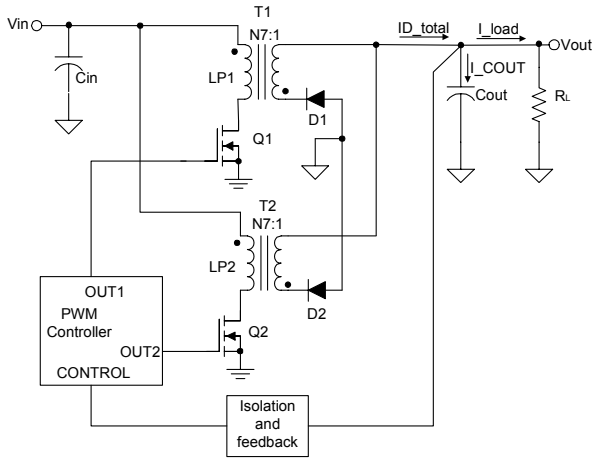


Fig. 17. Interleaved flyback converter.

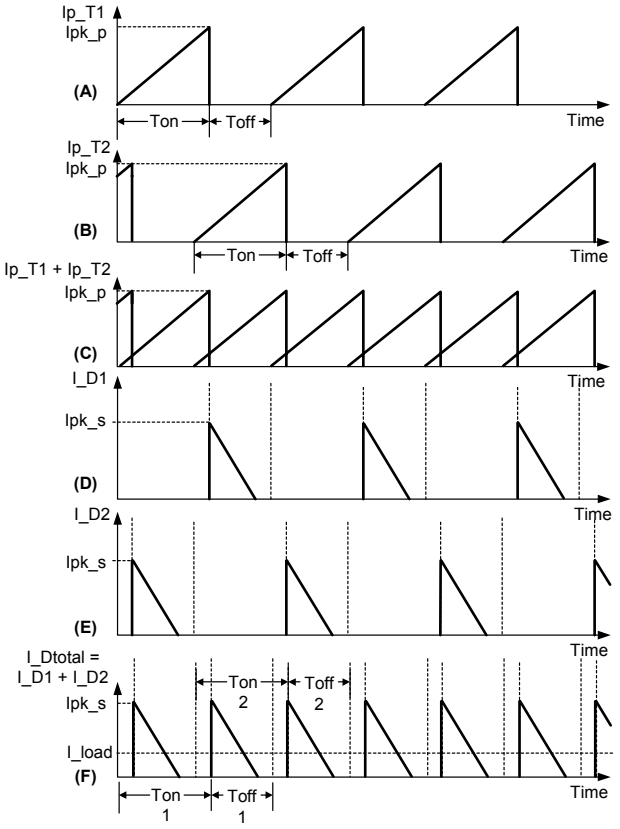


Fig. 18. Interleaved flyback converter waveforms, (A) primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms "a" and current waveform "b" seen at the input capacitor, (D) secondary transformer current of phase 1, (E) secondary transformer current of phase 2, (F) sum of current waveforms "d" and current waveform "e" just prior to the output capacitor (D = 0.6).

E. Design Equations for an Interleaved DCM Flyback Converter

As with the single interleaved flyback, the first step is to understand the balance equations that allow the DCM flyback converter to regulate its output voltage. Fig. 17 shows an interleaved flyback circuit and Fig. 18 the associated current waveforms for DCM operation. Line regulation is achieved by varying the duty cycle of the power switch such that the product of the switch on time and the input voltage is a constant. This results in constant peak inductor current which translates to a constant output power. During the period when Q1 or Q2 is on, energy is transferred from the input capacitor, Cin, to the primary inductance, Lp, of the transformer. The magnitude of this stored energy per phase is given by:

$$Win = \frac{1}{2} * Lp * (Ipk\_p)^2$$

where Ipk_p is the peak primary current for each phase.

No energy is transferred to the secondary circuit during this period. When Q1 is off, all the energy stored in the flyback transformer is delivered, by way of the secondary winding, to the output filter capacitor and load. Because there are two power stages in parallel, each power stage only needs to deliver one half (½) of the total input power. The average input power is given by:

$$Pin = \frac{Win1}{Ts} + \frac{Win2}{Ts}$$

where,

$$Win1 = \frac{Lp1 * Ipk\_p\_T1^2}{2}$$

$$Win2 = \frac{Lp2 * Ipk\_p\_T2^2}{2}$$

$$Ts = \frac{1}{Fs}$$

With the assumptions that Lp1 = Lp2 and Ipk_p_T1 = Ipk_p_T2, the above equation simplifies to:

$$Pin = \frac{Lp1 * Ipk\_p\_T1^2}{Ts}$$

The peak primary current (Ipk_p_T1) is dependent on the input voltage (Vin), the primary inductance, Lp, and the on time of Q1 (Ton):

$$Ipk\_p\_T1 = \frac{Vin * Ton}{Lp}$$

The average power output is related to the output voltage and load resistance, by:

$$Po = \frac{Vo^2}{RL}$$

Taking into account the efficiency of the power converter gives a more accurate calculation for the peak input current.

$$Pin = \frac{Po}{\eta}$$

where η is the efficiency of the power converter.

Substituting for pin and Ipk_p_T1 in the above equations yields:

$$\frac{Vo^2}{\eta * RL} = \frac{(Vin * Ton)^2}{Lp * Ts}$$

The DC output voltage is therefore:

$$Vout = Vin * Ton * \sqrt{\frac{\eta * RL}{Lp * Ts}}$$

or

$$Vout = Vin * D * \sqrt{\frac{\eta * RL * Ts}{Lp}}$$

$$D = \frac{Ton}{Ts}$$

Note that for a discontinuous flyback converter, the output voltage varies directly with both Vin and the square root of RL.

Because of the parallel power stages the transformer peak and RMS currents are reduced by a factor of 2.

F. Power Switch Peak Voltage

The turns ratio of the transformer is determined by setting an upper limit on the peak voltage seen by the primary switch, Vpk_Q1 = Vpk_Q2, with some ample margin to accommodate any leakage inductance spikes that may be present on the drain waveform. In general, the peak voltage on the main switches is selected to fit into the lowest voltage rated switches possible.

$$Vpk\_Q1 = Vin + N7 * (Vout + Vd)$$

G. Primary Inductance Selection to Ensure DCM

In order to guarantee that the power stage remains in the discontinuous conduction mode throughout the entire input voltage range the maximum on time is selected according to the following equation, at Vin_min.

$$Ton\_\max = \frac{(Vo + Vd) * N7 * 0.8 * Ts}{Vin\_\min + N7 * (Vo\_Vd)}$$

$$D\max = \frac{Ton\_\max}{Ts}$$

The primary inductance is then calculated as:

$$Lp = \frac{(Vin\_\min * Ton\_\max)^2}{\frac{Pout}{2 * \eta} * 2 * Ts}$$

Here, the output power is divided by two because the above equation is setting the inductance for each power stage and each power stage only needs to deliver half of the total input power.

H. Transformer Primary Peak Current

The transformer primary peak current is equal to:

$$Ipk\_p\_T1 = \frac{Vin\_\min * Ton\_\max}{Lp}$$

I. Transformer RMS Currents

Calculate the primary RMS current, Irms_p_T1:

$$Irms\_p\_T1 = Ipk\_p\_T1 * \sqrt{\frac{D}{3}}$$

The DC component of the primary transformer current, Idc_p_T1, is:

$$Idc\_p\_T1 = Ipk\_p\_T1 * \frac{D}{2}$$

The secondary currents have the same shape as the primary current. The only adjustments in the equations are to replace the primary peak current with N7*Ip_pk and change D to Tr/Ts where Tr is the ramp down time of the secondary current. Because the circuit was designed to operate in DCM, Tr is required to be less than Toff and hence it is not valid to simply replace D by 1-D as would be the case for the continuous conduction mode (CCM).

$$Tr = Ipk\_s\_T1 * \frac{L\sec}{V\sec}$$

where,

$$Ipk\_s\_T1 = N7 * Ipk\_p\_T1$$

$$L\sec = Lp * \left(\frac{1}{N7}\right)^2$$

$$V\sec = Vout$$

hence,

$$Tr = \frac{Ipk\_p\_T1 * Lp}{N7 * Vout}$$

The secondary RMS current is then:

$$Irms\_s\_T1 = N7 * Ipk\_p\_T1 * \sqrt{\frac{Tr * Fs}{3}}$$

The DC component of the secondary transformer current, Idc_s_T1, is:

$$Idc\_s\_T1 = N7 * Ipk\_p\_T1 * \frac{Tr * Fs}{2}$$

J. Input Capacitor RMS Current

The AC component of the primary current waveform, Icin_acrms which is the AC RMS current that flows through the input capacitors, is calculated in Appendix A. There is not a closed form expression given so implementing the equations in an automated calculation program like MathCAD™ is suggested.

K. Output Capacitor RMS Current

The AC component of the secondary current waveform, Iacrms_s_T1, which is the RMS current in the output capacitors, is given by:

$$Icout\_acrms = Iacrms\_s\_T1$$

$$Icout\_acrms = N7 * Ipk\_p\_T1 * \sqrt{\frac{2 * Tr * Fs}{3} * \left(1 - \frac{3 * 2 * Tr * Fs}{4}\right)}$$

L. Output Rectifier Peak Current

The peak secondary current is equal to the peak diode current

$$Ipk\_D1 = N7 * Ipk\_p\_T1$$

Summary of Interleaved-Flyback vs. Single-Flyback Converter

Advantages of interleaved flyback converter vs. single flyback:

- Reduced transformer and semiconductor peak currents
- Reduced transformer and semiconductor RMS currents
- Reduced input and output capacitor RMS currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of interleaved flyback converter vs. single flyback:

- Increased component count
- Possible increase in component area
- Control complexity of interleaved drive signals for Dmax greater than 50%

TABLE 9. INTERLEAVED FLYBACK CONVERTER EQUATIONS

Parameter	Interleaved Flyback
Ipk_s_T1	$N7 * Ipk\_p\_T1$
Ipk_p_T1	$\frac{Vin\_min * Ton\_max}{Lp}$
Irms_s_T1	$N7 * Ipk\_p\_T1 * \sqrt{\left(\frac{Tr}{3 * Ts}\right)}$
Irms_p_T1	$Ipk\_p\_T1 * \sqrt{\left(\frac{D}{3}\right)}$
Nx_min	$\frac{Vpk\_Q1 - Vin\_max}{Vout + Vd}$
Icin_acrms	D<=0.5; $Ipk\_p\_T1 * \sqrt{\left(\frac{D}{3}\right) * \left(1 - \frac{3 * D}{4}\right)}$ D>0.5; See Appendix A
Icout_acrms	$N7 * Ipk\_p\_T1 * \sqrt{\left(\frac{2 * Tr}{3 * Ts}\right) * \left(1 - \frac{3 * 2 * Tr}{4 * Ts}\right)}$
Vpk_Q1	$Vin\_max + N7 * (Vout + Vd)$
Vpk_D1	$\frac{Vin\_max}{N7} + Vspike$
Vpk_D2	$\frac{Vin\_max}{N7} + Vspike$
Ipk_D1	$N7 * Ipk\_p\_T1$

M. Interleaved Flyback Design Example

As an example consider the following design specifications for an interleaved flyback converter designed to operate in DCM:

- Vin_max = 375 Vdc
- Vin_min = 85 Vdc
- Vout = 12 V
- Pout = 200 W
- Fs = 50 kHz
- $\eta = 0.85$
- RL_min = $(Vout)^2$ / Pout = 0.72 Ω

Table 10, DCM single flyback converter vs. interleaved flyback converter, summarizes the values for the equations given in Tables 8 and 9. From these comparisons it is evident that the effect of interleaving power stages is to reduce the peak currents and the RMS currents to manageable levels, even for a 200-W example which would normally be considered outside of the reasonable power levels for a DCM flyback converter.

TABLE 10. DESIGN VALUES FOR 200-W FLYBACK EXAMPLES

200 W	Topology	
Parameter	**Flyback**	**Interleaved Flyback**
Dmax	0.505	0.505
Lp – (µH)	78.3	157
Ipk_s_T1 – (A)	122.3	61.1
Ipk_p_T1 – (A)	10.96	5.5
Irms_s_T1 – (A)	39.9	20.0
Irms_p_T1 – (A)	4.5	2.2
Nx_min	11.15	11.15
Icin_acrms - (A)	3.5	1.6
Icout_acrms – (A)	34.8	20.4
Vpk_Q1 – (V)	520.0	520.0
Vpk_D1 – (V)	33.6	33.6
Vpk_D2 – (V)	N/A	N/A
Ipk_D1 – (A)	122.3	61.1

V. HIGH POWER FACTOR (HIGH-PF) INTERLEAVED FLYBACK TOPOLOGY

A useful modification to the circuit in Fig. 17 is to use the DCM flyback converter as an isolated power factor correction (PFC) stage. The modified circuit is shown in Fig. 19. The main modification between Fig. 17 and 19 is that in Fig. 19 Cin is very small and as a result of the rectifier bridge and AC input, the voltage across Cin is a rectified sine wave at twice the AC line frequency. Also Cout is very large in order to suppress the line frequency ripple voltage on the output and to withstand a holdup time design requirement. In Fig. 19 the converter is operated in discontinuous conduction mode and the bandwidth of the control loop is intentionally much less than the line frequency so as to make the on time constant throughout one half of the line cycle. By operating the converter and control loop in this manner the average input current from the line resembles the wave shape of the line voltage, which by definition results in high power factor correction. With the converter operating in discontinuous conduction mode, this control technique allows unity power factor when used with converter topologies like flyback, Cuk, and SEPIC [3]. The instantaneous and average input current for one line cycle is shown in Fig. 20.

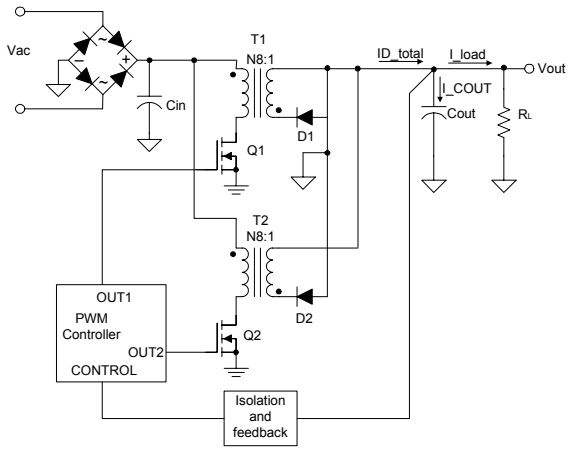


Fig. 19. High power factor (high-PF) interleaved flyback converter.

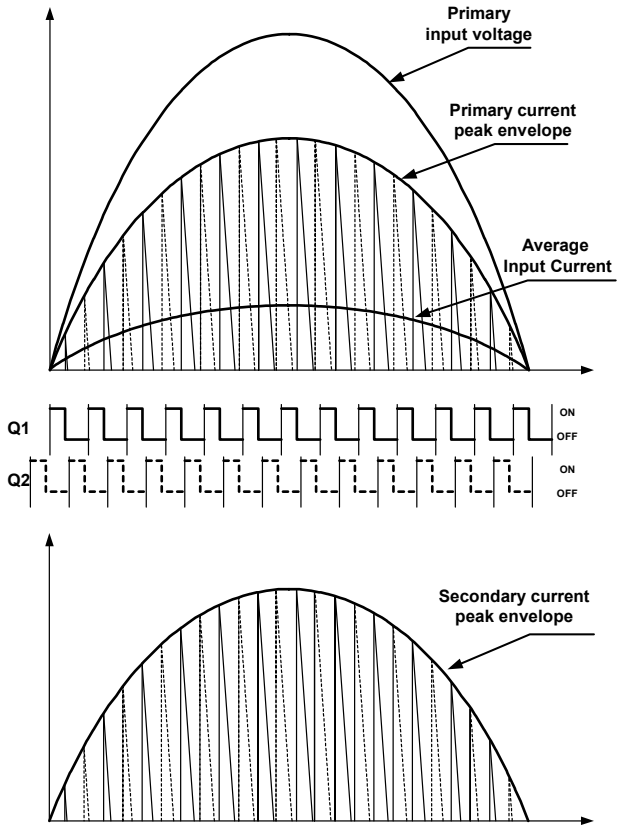


Fig. 20. (A) Input waveforms for high-PF interleaved flyback converter power, (B) Q1 power switch on and off times, (C) Q2 power switch on and off times, (D) secondary current waveform for high-PF interleaved flyback converter power stages.

VI. CONCLUSION

In recent years the usefulness of interleaving power stages has become apparent. The most well known application is in the powering of state-of-the-art microprocessors, commonly referred to as voltage regulator modules (VRMs). In VRM applications the power stages are non-isolated from their input to their output. This paper presented the benefits that interleaved topologies can have for isolated applications and in doing so has shown that the two inductor interleaved forward converter topology or the interleaved flyback converter topology are appropriate choices for many high power applications.

REFERENCES

[1] Abraham I. Pressman*, "Switching Power Supply Design"*, second edition, McGraw Hill ISBN 0-07-052236-7

[2] Michael T. Zhang, Milan M. Jovanovic and Fred C. Y. Lee "Analysis and Evaluation of interleaving Techniques in Forward Converters" in *IEEE Power Electronics* Vol. 13, No. 4, July 1998, pp. 690-698

[3] L. Rossetto, G. Spiazzi, P. Tenti, 'Control Techniques for Power Factor Correction Converters", University of Padova–Italy, Department of Electrical Engineering

[4] Bill Andreycak, "Controlled ON-Time, Zero Current Switched Power Factor Correction Technique" *Unitrode Power Supply Seminar* SEM-800, 1991 (SLUP095)

[5] K.H. Liu, Y.L.Lin, "Current Waveform Distortion in Power Factor Correction Circuits Employing Discontinuous-Mode Boost Converters," PESC Conf. Proc. 1989, pp. 825-829

[6] Raoji Patel, Glenn Fritz, "Switching Power Supply Design Review – 60 Watt Flyback Regulator" *Unitrode Power Supply Design Seminar SEM-100*, 1983 (SLUP058)

[7] User's Guide, "UCC28221 Evaluation Module", Texas Instruments, (SLUU173)

[8] UCC28220/1 Data Sheet, Texas Instruments, (SLUS544)

[9] Peng Xu, "Multiphase Voltage Regulator Modules with Magnetic Integration to Power Microprocessors", Dissertation submitted to the Faculty of the Virginia Polytechnic Institute and State University

[10] Lloyd H. Dixon, "Magnetics Design for Switching Power Supplies", *Unitrode Magnetics Design Handbook,* (MAG100A), 1999 (SLUP132)

[11] "UCC28220, UCC28221 Data Sheet – Interleaved Dual PWM Controller with Programmable Max Duty Cycle", Texas Instruments (SLUS544), September 2003

[12] Lloyd H. Dixon, "Minimizing Winding Losses in Magnetic Devices", Unitrode Power Supply Seminar, SEM-1400, (SLUP171) 2001

APPENDIX A.
CALCULATION OF THE AC RMS INPUT CURRENT FOR THE INTERLEAVED FLYBACK CONVERTER

This program calculates the ac rms current of two ramp waveforms which have the same duty cycle, but are 180 degrees out of phase from one another.

$Vin := 85$

$Lp := 156 \cdot 10^{-6}$

$Ts := \frac{1}{50000}$

$D := 0.51$

$Ton1 := D \cdot Ts$

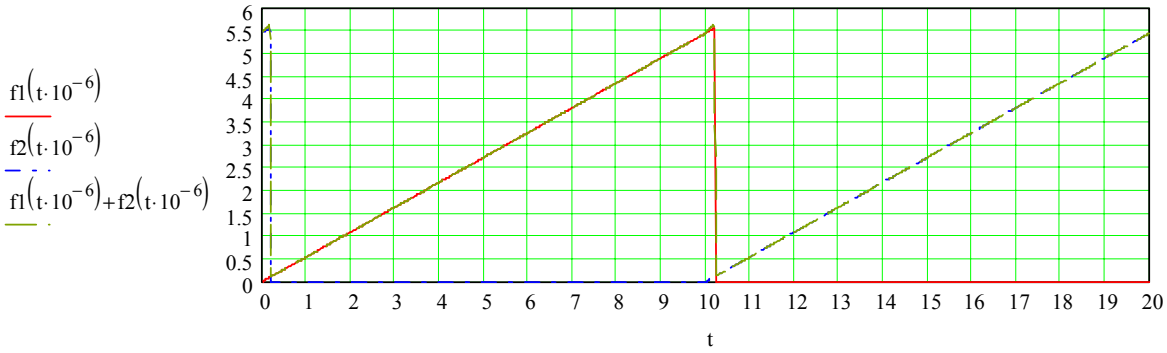
$Ton2 := Ton1$

$Ipk := \frac{Vin}{Lp} \cdot Ton1$

$Ipk = 5.558$ Amps

$$f1(t) := \begin{cases} \frac{Ipk}{Ton1} \cdot t & \text{if } t \le Ton1 \\ 0 & \text{otherwise} \end{cases}$$

$$f2(t) := \begin{cases} \frac{Ipk}{Ton2} \cdot (t + 0.5 \cdot Ts) & \text{if } 0 \le t \le (Ton2 - 0.5 \cdot Ts) \\ \frac{Ipk}{Ton2} \cdot (t - 0.5 \cdot Ts) & \text{if } t > 0.5 \cdot Ts \\ 0 & \text{otherwise} \end{cases}$$



$$Iin\_rms := \sqrt{\frac{1}{0.5 \cdot Ts} \cdot \int_0^{0.5 \cdot Ts} (f1(t) + f2(t))^2 \, dt}$$

$Iin\_rms = 3.266$ Arms

$$Iin\_dc := \frac{1}{0.5 \cdot Ts} \cdot \left[\int_0^{0.5 \cdot Ts} (f1(t) + f2(t)) \, dt \right]$$

$Iin\_dc = 2.861$ Adc

$$Iin\_acrms := \sqrt{Iin\_rms^2 - Iin\_dc^2}$$

$Iin\_acrms = 1.575$ Arms

APPENDIX B.
TWO INDUCTOR INTERLEAVED FORWARD CONVERTER DESIGN EXAMPLE

Specifications:

- V_{IN} = 36 V to 75 V
- $V_{UVLO-ON}$ = 34 V ±4%
- $V_{UVLO-OFF}$ = 32 V ±4%
- $V_{OVLO-OFF}$ = 85 V ±4%
- $V_{OVLO-ON}$ = 83 V ±4%
- V_{OUT} = 12 V ±3%
- Vripple < 1%
- P_{OUT} = 200 W
- $I_{OUT,MAX}$ = 16.7 A
- f_{SW} = 500 kHz (per phase)
- Isolation: 500 V
- PWM controller (UCC28221)
- Form factor: ½ brick

N. Topology: Interleaved Forward with Resonant Reset

The example schematic is shown in Fig. B1. The selection of the power stage is covered below. For information regarding the selection of the components around the PWM control chip refer to the application section in Reference 11.

O. Transformer Design

The transformer area product equation given in Reference 10 on page 4 through 8 provides an estimation of the required core size. In this example the transformer core was smaller than the predicted size from the area product estimate, but its operation and suitability for this application was verified at the extreme operating conditions. The transformer is a custom design from Payton America Inc (part number, 50863). The specifications are:

- Number of primary turns = 7 turns
- Primary magnetizing inductance = 35 µH
- Secondary number of turns = 5 turns
- Primary auxiliary winding = 5 turns

P. Input capacitor Selection

Referring to Table 6, the input capacitor AC RMS ripple current is 1.1 Arms at low line. The maximum AC RMS ripple current in the input capacitors occurs at high line. Evaluating the AC RMS ripple current equation at Vin-max yields a maximum current of 2.98 Arms. The selected film capacitors have an RMS current rating of 12 Amps which easily satisfies this requirement.

Q. Output Inductor Selection

The output inductor is equal to 3.2 µH, which yields a peak-to-peak output ripple current in each phase of 6.39 A at high line and 4.5 A at low line. This amount of ripple current is on the high side, but by factoring in the benefits of ripple current cancellation due to the interleaved power stages, the actual peak-to-peak ripple current seen by the output capacitor is only 4.3 A at high line and 0.343 A at low line.

R. Output Capacitor Selection

Because of the reduced peak-to-peak ripple current seen by the output capacitors, it is possible to use output capacitors with higher ESR than would be allowed for a single forward converter with the same amount of output inductance. In this example, the design specifications dictate that the design have less than 1% total output ripple voltage under worst case conditions, which is at high line. It is customary to allow the resistive portion of the output capacitor to account for half of the output ripple voltage specification. Hence, the maximum allowable equivalent series resistance (ESR) of the output capacitor is 0.014 Ω. The example design used three capacitors with 0.045 Ω of ESR each. Each capacitor has a capacitance of 82 µF.

S. Circuit Schematic

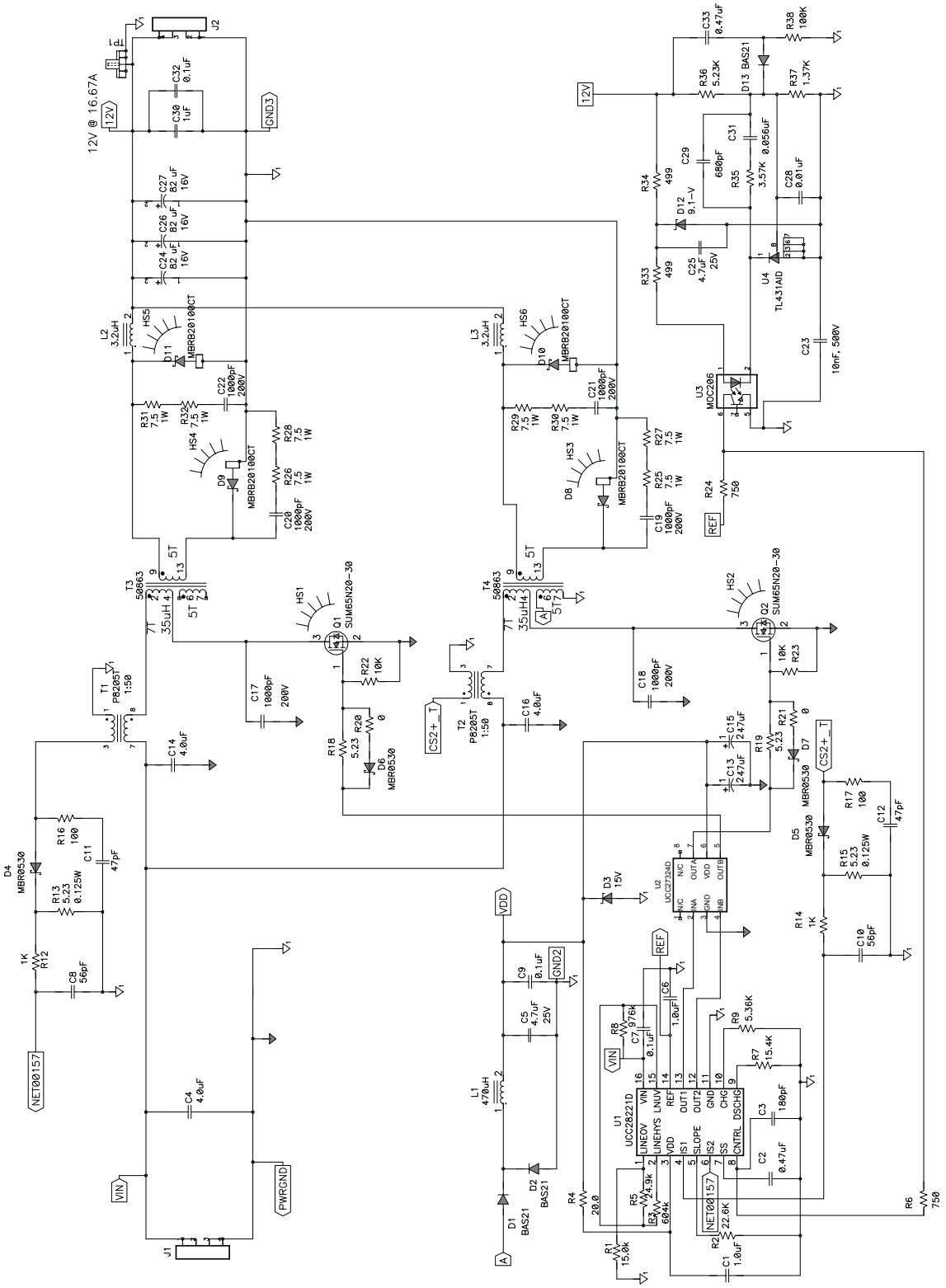


Fig. B1. 2L interleaved forward converter design example.

T. Layout

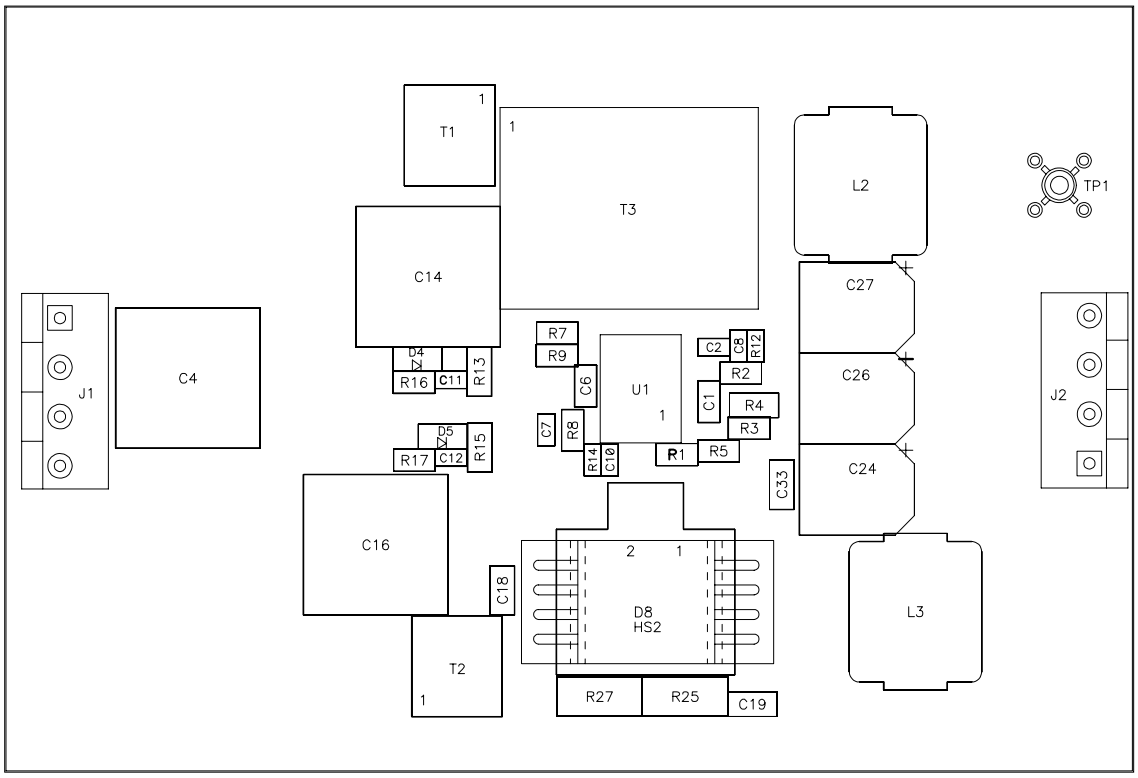


Fig. B2: Top view of PCB layout.

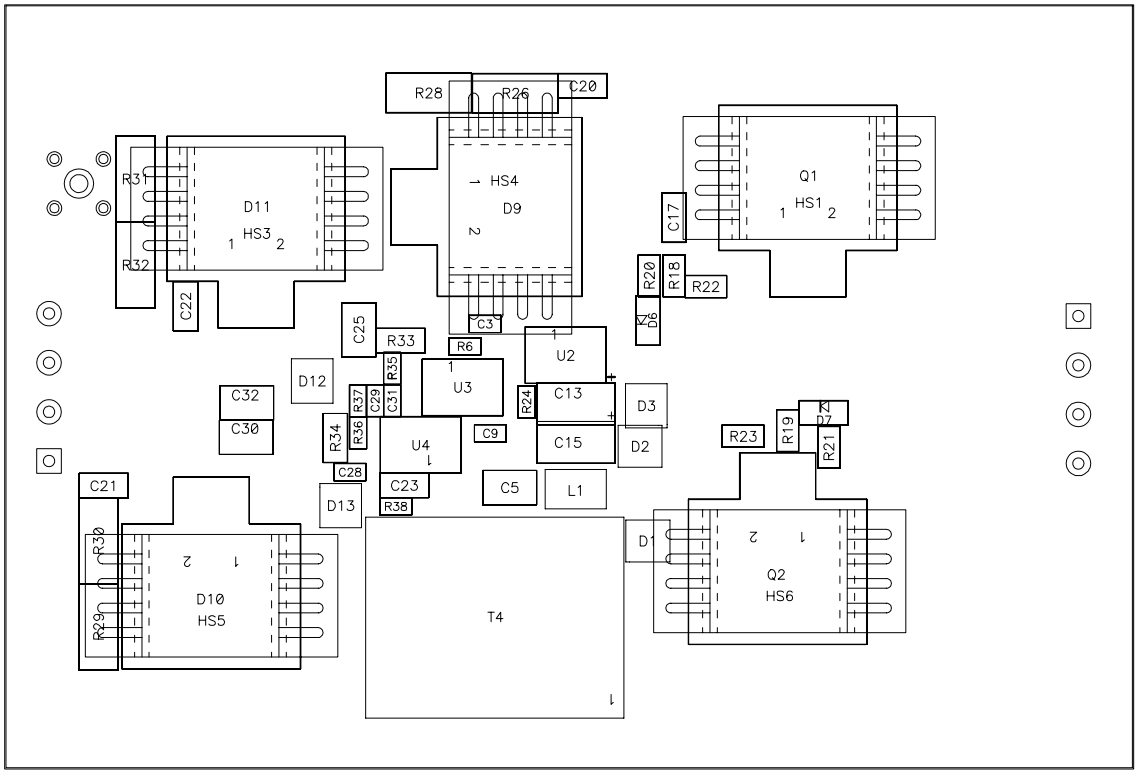


Fig. B3. Bottom view of PCB layout.

U. Drain Voltage Waveforms

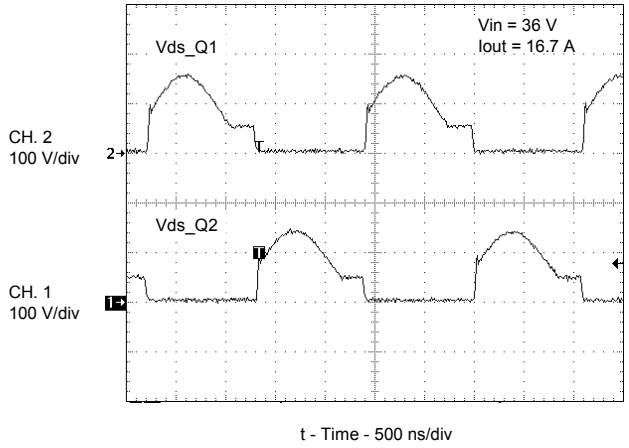


Fig. B4. Q1 and Q2 drain voltages (Vin = 36 V, Iout = 16.7 A).

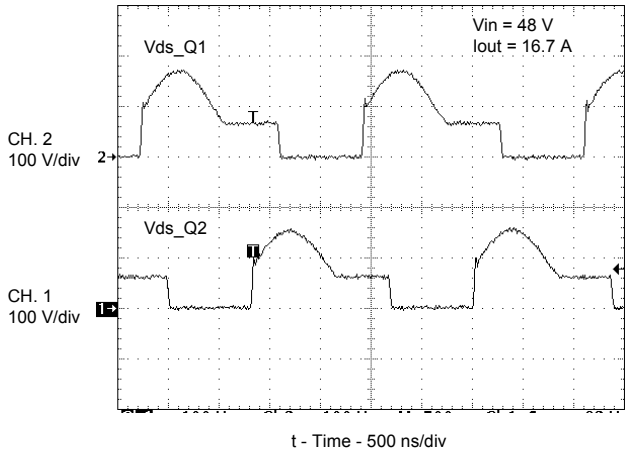


Fig. B5. Q1 and Q2 drain voltages (Vin = 48 V, Iout = 16.7 A).

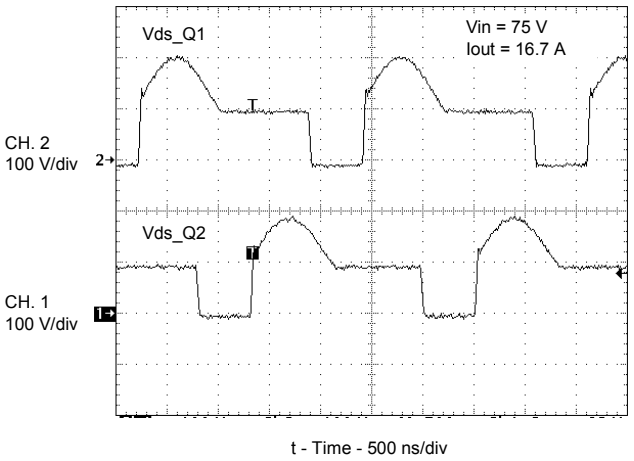


Fig. B6. Q1 and Q2 drain voltages (Vin = 75 V, Iout = 16.7 A).

V. Output Inductor Peak-to-Peak Ripple Current

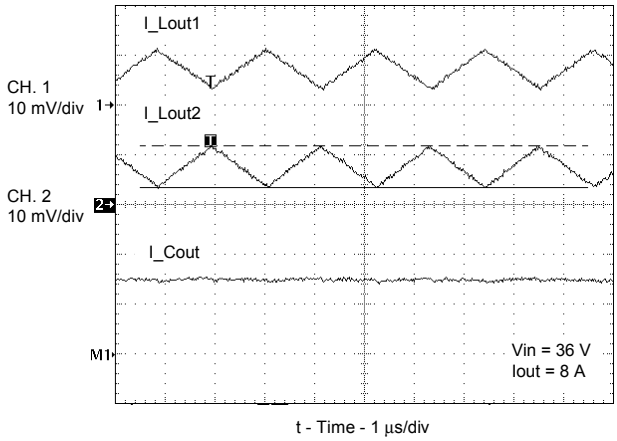


Fig. B7. Output inductor ripple currents and capacitor ripple current (Vin = 36 V, Iout = 8 A).

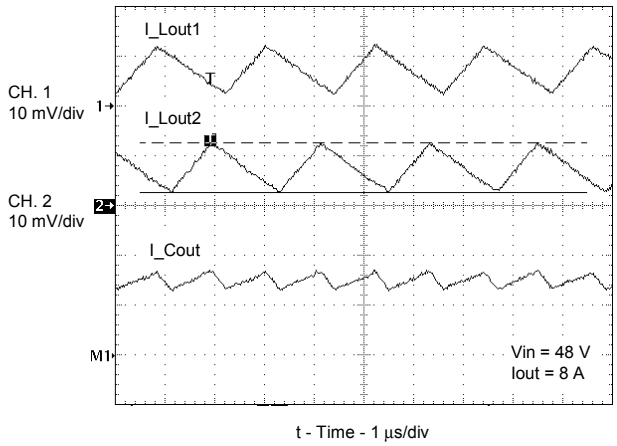


Fig. B8. Output inductor ripple currents and capacitor ripple current (Vin = 48 V, Iout = 8 A).

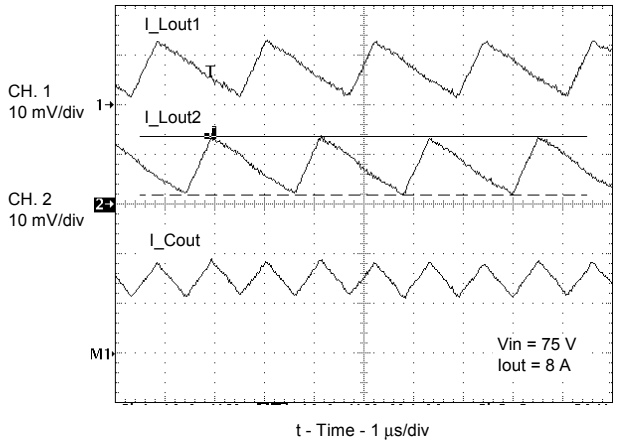


Fig. B9. Output inductor ripple currents and capacitor ripple current (Vin = 75 V, Iout = 8 A).

W. Transient Response 2 Phases and then 1 Phase

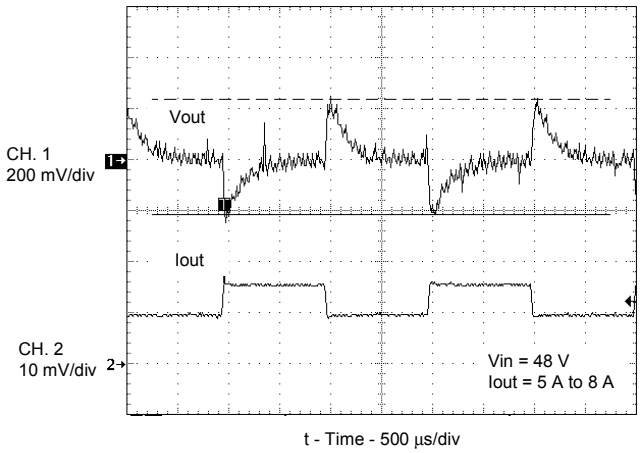


Fig. B10. Output transient response with 2 phases active (Vin = 48 V, Iout = 5 A to 8 A).

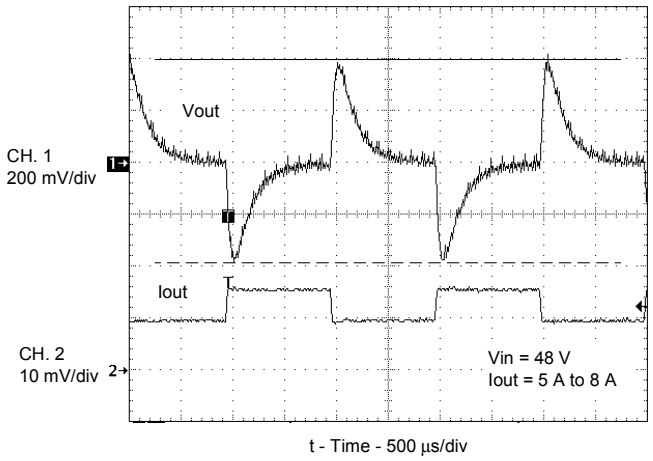


Fig. B11. Output transient response with only one phase active (Vin = 48 V, Iout = 5 A to 8 A).

X. Efficiency Curves

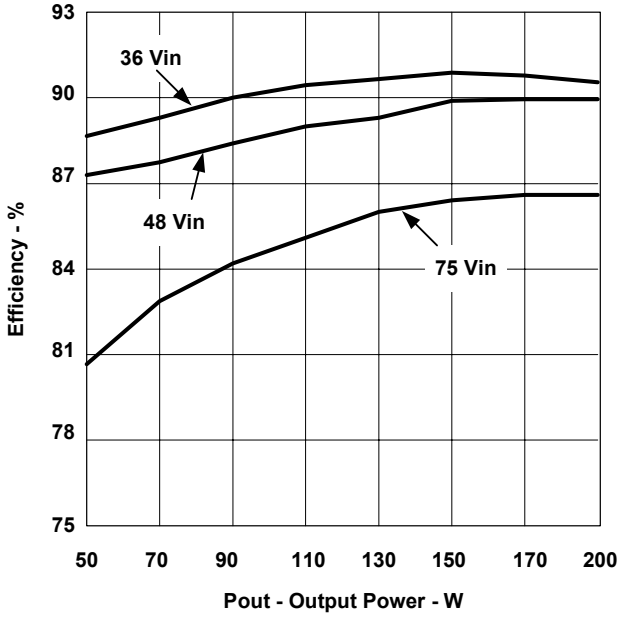


Fig. B12. Efficiency vs. output power.

TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page
support.ti.com

TI E2E™ Community Home Page
e2e.ti.com

Product Information Centers

Americas	Phone	+1(972) 644-5580
Brazil	Phone	0800-891-2616
Mexico	Phone	0800-670-7544
	Fax	+1(972) 927-6377
	Internet/Email	support.ti.com/sc/pic/americas.htm

Europe, Middle East, and Africa

Phone

European Free Call	00800-ASK-TEXAS (00800 275 83927)
International	+49 (0) 8161 80 2121
Russian Support	+7 (4) 95 98 10 701

Note: The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

Fax	+(49) (0) 8161 80 2045
Internet	support.ti.com/sc/pic/euro.htm
Direct Email	asktexas@ti.com

Japan

Phone	Domestic	0120-92-3326
Fax	International	+81-3-3344-5317
	Domestic	0120-81-0036
Internet/Email	International	support.ti.com/sc/pic/japan.htm
	Domestic	www.tij.co.jp/pic

Asia

Phone

International	+91-80-41381665
Domestic	Toll-Free Number

Note: Toll-free numbers do not support mobile and IP phones.

Australia	1-800-999-084
China	800-820-8682
Hong Kong	800-96-5941
India	1-800-425-7888
Indonesia	001-803-8861-1006
Korea	080-551-2804
Malaysia	1-800-80-3973
New Zealand	0800-446-934
Philippines	1-800-765-7404
Singapore	800-886-1028
Taiwan	0800-006800
Thailand	001-800-886-0010

Fax	+8621-23073686
Email	tiasia@ti.com or ti-china@ti.com
Internet	support.ti.com/sc/pic/asia.htm

A122010

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265