

# Flyback transformer design considerations for efficiency and EMI



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# AC/DC power supplies widely use the flyback converter given its simplicity and wide operating range, and because it eliminates the output filter inductor and free-wheeling rectifier required for forward-mode topologies.

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Three main topology components dominate flyback-converter performance: the primary switch, secondary rectifier and transformer. This paper focuses on the importance of transformer design, since this single component has a profound impact on converter efficiency and electromagnetic interference (EMI). This paper will discuss the various conflicting design requirements, the often-neglected subtleties of core loss and snubber clamp level, and ways to improve transformer performance.

## Introduction

Many AC/DC and DC/DC power supplies, from very low power levels to as much as 150 W or more, use the flyback converter. Often maligned and not always fully understood, the transformer is the heart of the flyback power supply and probably the most important component. When designed and implemented well, the transformer can deliver the required performance cost-effectively. When poorly designed, it can cause EMI issues, low efficiency and possible thermal overstress issues.

This paper will discuss the causes of the major losses in the flyback transformer. In particular, we will review core loss in light of recent research findings that highlight the significant impact of duty cycle and DC bias. The significant contribution of proximity effect on AC copper loss is also discussed.

We will review wire-size selection and winding methods to reduce AC copper loss. The effect of snubber clamp voltage levels and the

often-neglected absorption of magnetizing energy by the snubber is also highlighted.

For conducted EMI, we will outline the causes of common-mode (CM) EMI, suggesting various winding structures and techniques to ensure good CM balance.

Finally, through several examples we will show how transformer construction can have a significant impact on both efficiency and conducted EMI. In these examples, we changed none of the other components – only the transformer – in order to demonstrate how a well-designed transformer can simultaneously improve both efficiency and EMI.

## The flyback topology

The flyback transformer is not really a transformer in the conventional sense; it is actually a coupled inductor. **Figure 1** is a simplified schematic of a flyback converter. The flyback transformer in this example has three windings: primary, secondary and bias (sometimes called the auxiliary winding).

When the primary switch turns on, the input voltage is imposed across the primary winding. Since the dot-end of the primary winding is connected to ground, the dot-end of both the secondary and auxiliary windings will be negative and proportional to the input voltage. The respective rectifier diodes on those windings will thus be reverse-biased. While the primary switch remains on, current builds up in the primary winding at a rate dependent on the input voltage and the primary magnetizing inductance,  $L_p$ .

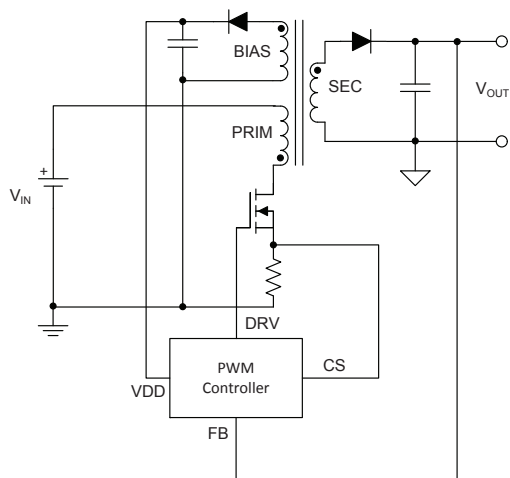


Figure 1. Simplified schematic for a typical flyback converter.

Once the current in the primary reaches the level

required by the pulse-width-modulation (PWM) controller for regulation, the primary switch is turned off. The primary current then transfers to the secondary winding and the current decays at a rate proportional to  $V_{OUT}$ . In this way, the energy stored in the transformer during the buildup of primary current gets released to the load and output capacitor during the flow of secondary current. This is, of course, a simplified explanation; for more detailed descriptions of the flyback topology and modes of operation, see references [1], [2] and [3].

Based on this description, the flyback transformer actually operates as a coupled inductor, where current builds up to a peak value in the primary winding and then decays back down in the secondary winding during the flyback interval. Thus, when designing the flyback transformer and assessing the losses, you must consider it more of an inductor than a transformer.

### Flyback operation

Figure 2 shows the different operating phases of the flyback converter during a single switching cycle, with the corresponding voltages and currents shown in Figure 3. During the primary switch on-time interval in Figure 2a, current flows from

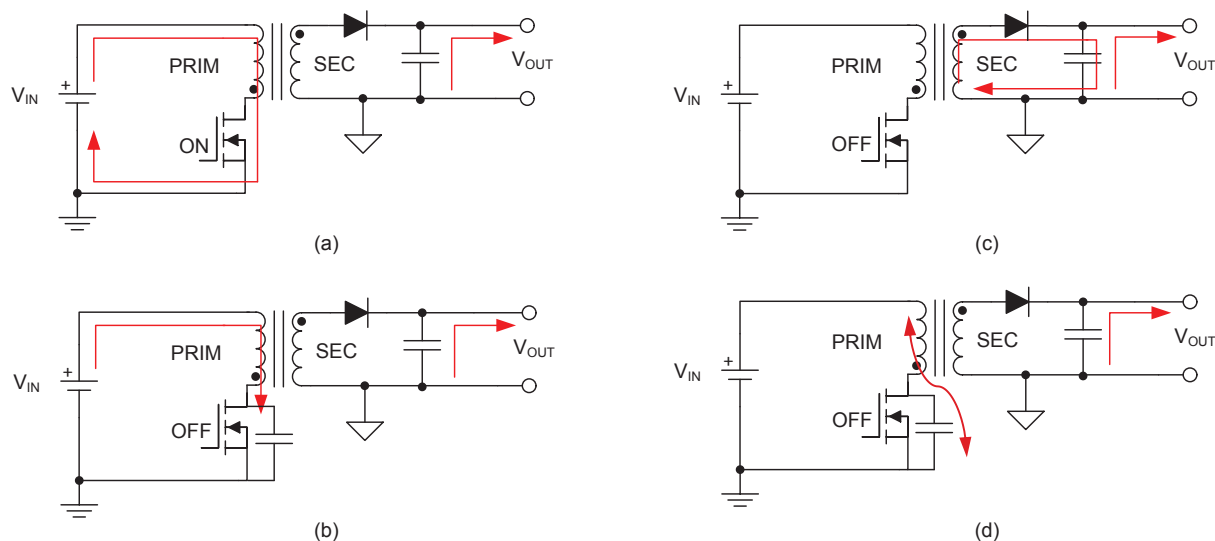
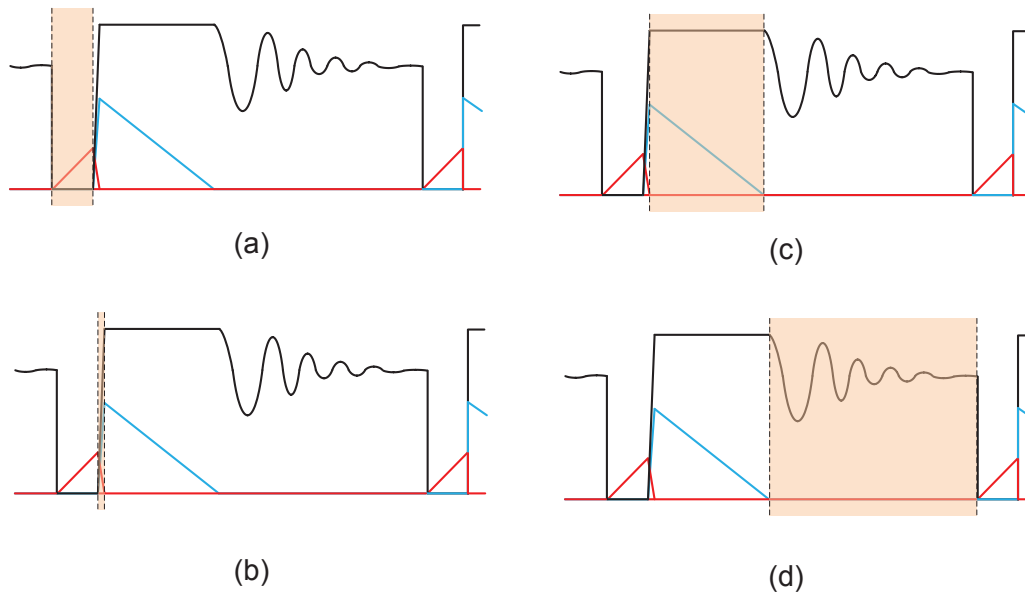


Figure 2. Flyback converter operating intervals per switching cycle: primary switch on-time (a); primary switch turn-off, transition interval (b); secondary rectifier clamping and conduction interval (flyback interval) (c); discontinuous conduction mode (DCM) ringing interval (d).



**Figure 3.** “Idealized” flyback converter voltages and currents, with highlighted operating intervals per switching cycle: primary switch on-time (a); primary switch turn-off, transition interval (b); secondary-rectifier clamping and conduction interval (flyback interval) (c); DCM ringing interval (d).

the input-voltage source through the transformer’s magnetizing inductance, storing energy in the inductor air gap. During the transition interval in **Figure 2b**, the primary current transitions to the secondary, while the transformer’s primary voltage swings positive. When the transformer primary voltage swings sufficiently more positive than  $V_{IN}$ , the output flyback diode becomes forward-biased and clamps the voltage. Subsequently, during the interval in **Figure 2c**, the secondary current will decay linearly (since the voltage across the secondary winding is negative). During the interval in **Figure 2c**, some or all of the energy previously stored in the transformer’s magnetizing inductance will be released to the secondary-side storage capacitor and to the load.

In discontinuous conduction mode (DCM), all of the energy stored in the inductance during the primary on-time interval is delivered to the secondary during the flyback interval. In this mode, the secondary current decays to zero at the end of the flyback interval. Subsequently, the interval in **Figure 2d** is the DCM ringing interval, where the magnetizing inductance resonates with the total parasitic

capacitance on the switch node. The losses in the transformer core and the AC resistance (ACR) of the windings dampen this ringing.

In continuous conduction mode (CCM), the interval in **Figure 2d** does not occur because the primary on-time commences before the secondary current decays to zero. In CCM, not all of the energy stored in the transformer’s magnetizing inductance transfers to the secondary during each switching cycle.

### Flyback transformer losses

The flyback transformer is responsible for a large percentage of the total losses in a flyback power stage. There are four categories of losses:

- Core losses.
- Copper (winding) losses.
- Transition losses.
- External losses.

Core losses occur in the transformer’s ferrite core and depend on the core’s flux density (amplitude, duty cycle and flux-density rate of change), frequency of operation, core size or volume, and

properties of the chosen ferrite material. Different materials optimized for different frequency and peak flux-density ranges will exhibit varying core-loss characteristics. We will describe core losses in more detail in the next section.

The flow of current through the resistance of the windings causes copper or winding losses. Most designers refer to it as copper loss because copper is by far the most commonly used wire material given its low resistance, ease of manufacture and wide availability.

Copper loss breaks down further into DC loss and AC loss. DC loss is caused by DC or low-frequency root-mean-square (rms) current flowing through the DC resistance (DCR) of the winding. Maximizing the wire cross-sectional area and minimizing the wire length minimizes DCR.

AC loss is caused by high-frequency electromagnetic effects from the magnetic field produced by the time-variant current flowing in the wires. AC loss can be very significant, especially for large wire diameters. We will discuss AC losses in more detail later.

Transition losses refer to the losses associated with the transition or commutation of transformer current from the primary to secondary winding. In this region, the rate of change of the currents ( $di/dt$ ) is very high, so the currents will have large high-frequency harmonic content. Also in this region, since both primary and secondary currents flow simultaneously, the flyback transformer behaves more like a conventional high-frequency transformer, and so high-frequency effects and ACR

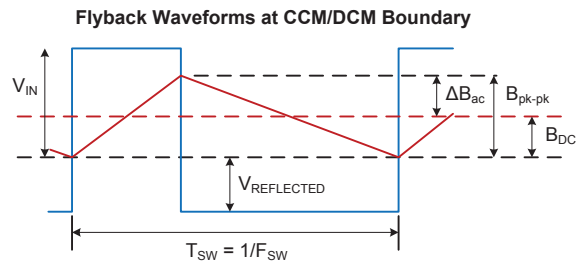
are significant causes of loss. As transition loss is beyond the scope of this topic, see reference [4] for further details.

While the transformer itself incurs most of the losses, two significant external losses occur due to parasitic elements of the transformer. First, leakage inductance results in a loss incurred in the external clamp or snubber circuit, which is necessary to keep the voltage stress on the primary switch below its  $V_{DS}$  maximum rating. Second, transformer capacitance contributes to the total parasitic capacitance of the switch node. An increase in the switching node capacitance increases the switching losses in the primary switch. We discuss the effects of leakage inductance and interwinding capacitance further in the section on EMI shielding.

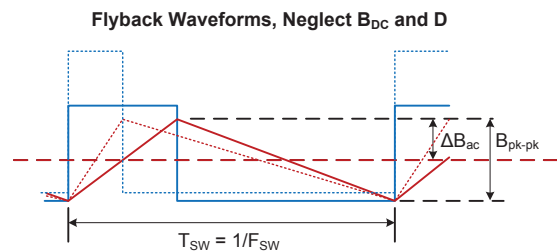
### Core loss in a flyback converter

Traditionally, designers assumed that DC flux did not affect the core losses in an inductor, and these losses are largely independent of the flux-density waveform. For example, as **Figure 4** shows, the flyback flux-density waveform is nonsinusoidal, not necessarily 50 percent duty cycle and contains a significant DC component. Yet when calculating core loss, most designers neglect the DC component and duty cycle and consider only the peak-to-peak flux swing, as shown in **Figure 5**.

Another common assumption is that all waveforms, regardless of duty cycle and DC bias, have the same core loss because they have the same  $B_{pk-pk}$  flux-density swing. Thus, designers extracted the core losses from the published sine-wave-specific loss curves using the flux-density amplitude and frequency experienced by the converter.



**Figure 4.** Flyback transformer flux-density waveform at CCM/DCM boundary.



**Figure 5.** Flyback transformer waveforms at CCM/DCM boundary, neglecting the  $B_{DC}$  component and duty-cycle variation.

A closer qualitative examination reveals that these assumptions must be incorrect. It should be apparent that the eddy currents induced in the core are higher when the rate of flux change is faster, since the induced voltage driving the eddy currents will be higher. Thus, compared to the eddy current loss generated by a sine wave of equal frequency, a low duty-cycle rectangular voltage waveform generating an equal peak-to-peak flux density must generate higher eddy current loss in the core.

Additionally, the magnetic domains theory suggests that the domain walls cause nonuniform flux density, which results in eddy current losses in excess of those related to the material's conductivity.

References [5], [6], [7] and [8] discuss in more detail the mechanisms that relate the losses to waveforms, duty cycle and DC bias, which are beyond the scope of this paper. Those authors

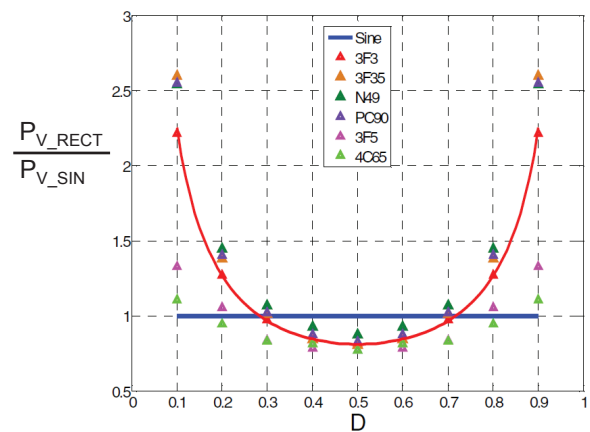
offer equations that relate manufacturer-published specific loss data for sine-wave excitation only (no DC bias) to actual losses generated with rectangular waveforms and DC bias, and provide empirical support for their theories.

### Effect of rectangular waveforms with variable duty cycle

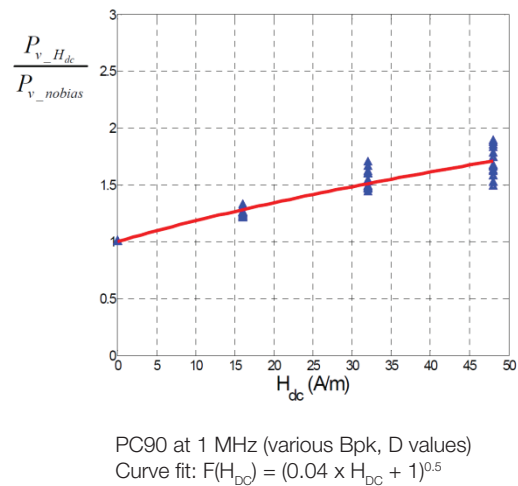
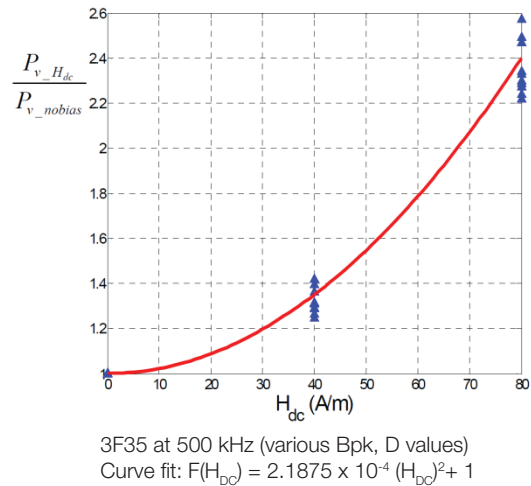
Reference [6] investigates the ratio of core loss under rectangular-wave excitation to that of a sinusoidal-wave excitation of equal flux amplitude for a number of magnetic materials (**Figure 6** reproduced from [6]). It also introduces a curve-fit equation for the core loss versus duty cycle (Equation 1):

$$\frac{P_{v\_rect}}{P_{v\_sine}} = F_{waveform} = \frac{8}{\pi^2 \cdot [4D \cdot (1-D)]^{\gamma+1}} \quad (1)$$

where  $D$  is the duty cycle and  $\gamma$  is a correction factor specific to the material, operating frequency and temperature, and has to be extracted from careful measurements. Reference [6] tabulates measured values of  $\gamma$  for several different ferrite materials.



**Figure 6.** Core-loss ratio for rectangular versus sinusoidal excitation as a function of duty cycle [6]. (Image: Courtesy of the Institute of Electrical and Electronics Engineers [IEEE], © IEEE 2014)



**Figure 7.** Core-loss ratio for DC bias versus no bias excitation. Source: Reference 5. (Images: Courtesy of Virginia Tech)

## Effect of DC bias

The author of reference [5] measured the effect on core losses when adding a DC bias,  $H_{DC}$ , for rectangular-waveform excitation and proposed a curve-fitting factor,  $F(H_{DC})$ , to account for the increase in loss due to the presence of DC bias in the core.

**Figure 7** shows curve-fitting equations for  $F(H_{DC})$  for 3F35 and PC90 ferrite materials generated from measurement data of core losses with DC bias, and rectangular-waveform excitation at different duty cycles and flux-density amplitudes.

The  $F(H_{DC})$  function represents the increase in core loss caused by DC bias; it appears that it is relatively insensitive to the amplitude and duty cycle of the excitation voltage.

## Total core loss for arbitrary waveforms

Equation 2 combines the results presented above with the core-loss equations provided by manufacturers for sine-wave excitation to calculate core loss for the rectangular-waveform excitation present in flyback (and many other PWM) converters:

$$P_{v\_total} = P_{v\_sine} \cdot F_{waveform}(\gamma, D) \cdot F_{DC}(H_{DC}) \quad (2)$$

where  $P_{V\_SINE}$  is the Steinmetz equation loss for sinusoidal excitation.

References [5] and [6] contain the information necessary to use Equation 2 for several Ferroxcube materials. We hope that magnetic materials manufacturers will consider verifying the validity of the results reported and generate the information necessary to enable users to accurately calculate core losses in PWM applications, which are far more common than sine-wave applications.

In order to put Equation 2 to practical use, manufacturers must make available the following information about magnetic materials:

- Frequency and flux-density exponents to generate the correct  $P_{V\_SINE}$  at the relevant flux density and frequency range. (Note: Ferroxcube provides an excellent spreadsheet documenting their materials, available upon request).
- The  $\gamma$  parameter and an appropriate equation with which to use it.
- The equation for  $F_{DC}(H_{DC})$ .



We must emphasize a few points:

- Duty cycle and DC-bias effects on core losses are significant, and should not be ignored.
- The substantial increase in core loss at extreme duty-cycle values is an often-neglected penalty of wide input/output-voltage-range converters.
- The increase in loss due to DC bias reduces the benefits expected from CCM operation.
- The assumption of equal core loss in single- and double-ended applications with equal AC flux excursions is probably incorrect.

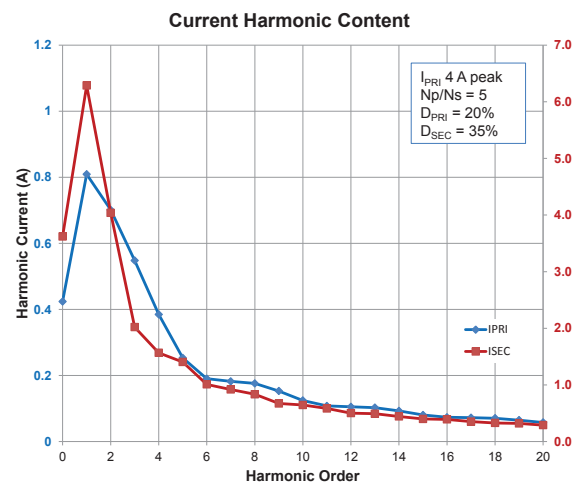
## Copper loss and AC effects in flyback transformers

Current flowing through the resistance of copper windings causes copper loss in a transformer. Losses arise because of the DC component of the current and the DCR of the windings, but also (and often more significantly) from high-frequency AC effects.

For flyback converters operating in DCM or transition mode (TM), the current flowing in both the primary and secondary windings is triangular in shape (**Figure 3**). Since the flyback converter stores energy during the primary conduction interval and then delivers energy to the load and the output capacitor during the secondary conduction interval, the duty cycle of each interval is typically less than 50 percent. The primary duty cycle will often be much less than 50 percent at high-line input voltages, where the  $di/dt$  of the current ramp is much steeper, and so the high-frequency harmonic content will also be greater. Consequently, AC loss mechanisms can become more significant. Note that in **Figure 8**, the zeroth harmonic is actually the DC component of the current waveform.

Since the flyback's primary and secondary currents have a significant DC component and significant high-frequency harmonic content (**Figure 8**), both ACR and DCR are important. The ACR-to-DCR ratio

will depend on the frequency, wire diameter and overall layer structure. The eddy currents induced inside the wires (as a result of the magnetic field inside the wires) are the main cause of AC loss and increased ACR. These eddy currents lead to skin effect and proximity effect, which we will explain further in the next sections.

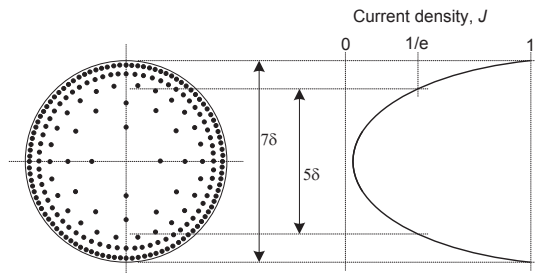


**Figure 8.** Harmonic content of typical flyback primary and secondary current.

## Skin effect

When DC current flows in a wire, the current density is uniform throughout the wire's cross-section; in other words, the current is distributed equally across the wire. But when a time-varying AC current flows, the changing current produces a changing magnetic field around the wire. This changing magnetic field is also present inside the wire. Faraday's law states that whenever there is a changing magnetic field, a voltage (or electromotive force [EMF]) is induced, so as to oppose the changing magnetic field. The induced voltage causes circulating eddy currents to flow, and since the conductivity of copper is high, these currents can be very significant. The eddy currents reduce or cancel the current flow in the center of the wire, and reinforce or increase the current flow in the outer regions of the wire cross-section, leading to current-density distribution as shown in **Figure 9**.





**Figure 9.** Nonuniform AC current distribution due to induced eddy currents. Source: Reference 9.

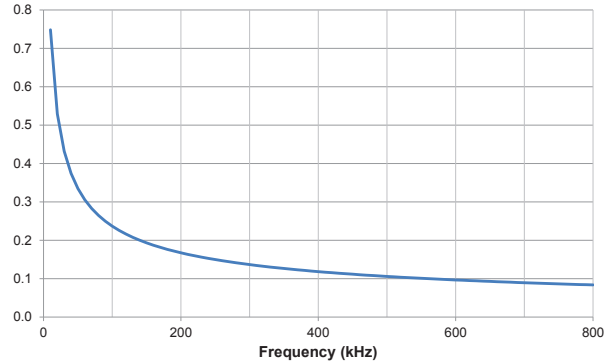
As the frequency of the AC current increases, the current becomes more concentrated near the outer edges of the wire, and the central portion of the wire will carry almost none of the current. The “skin depth” is defined as the depth inside the wire where the current density has fallen to approximately 37 percent (1/e) of the value at the surface. This depth is also where the penetrating magnetic field strength has fallen by the same 1/e ratio – hence it is also sometimes referred to as “penetration depth.” Penetration depth,  $\delta$ , depends on the resistivity of the wire material,  $\rho$ , the relative magnetic permeability of the wire material,  $\mu_r$ , and the frequency of interest,  $f$ . See Equation 3:

$$\delta = \sqrt{\frac{\rho}{(\pi \cdot \mu_0 \cdot \mu_r \cdot f)}} \quad (3)$$

Since the wire used in transformers is almost exclusively copper,  $\delta$  can be conveniently expressed as a function of only frequency. At 100°C, Equation 4 gives the  $\delta$  of copper, where  $f$  is in kilohertz (plotted in **Figure 10**):

$$\delta = \sqrt{\frac{2.3 \cdot 10^{-8}}{(\pi \cdot 4\pi \cdot 10^{-7} \cdot 1 \cdot 1k)}} \cdot \frac{1}{\sqrt{f}} = \frac{2.4 \text{ mm}}{\sqrt{f}} \quad (4)$$

Looking back at **Figure 9** as an example, the wire diameter is seven times larger than  $\delta$  at the frequency of interest. To approximate the ratio of

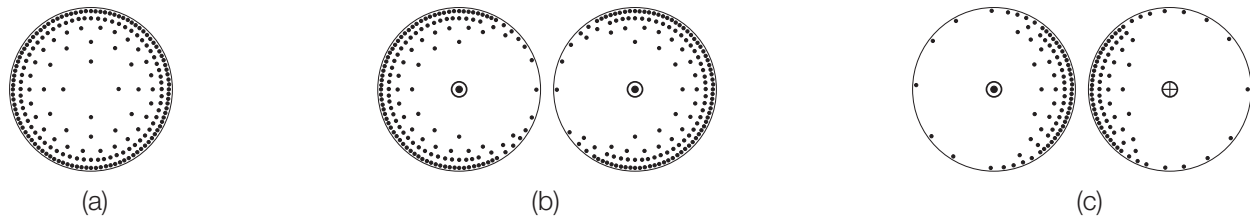


**Figure 10.** Copper skin depth (or penetration depth) in millimeters vs. frequency in kilohertz at 100°C.

ACR to DCR, assume that all of the AC current flows in an annular ring around the outside of the wire, one penetration-depth wide. Thus, Equation 5 approximates the ratio of ACR to DCR by the ratio of the total wire cross-section to the cross-section of the  $1-\delta$  wide outer annulus:

$$\frac{ACR}{DCR} = \frac{(7\delta)^2}{(7\delta)^2 - (5\delta)^2} = \frac{49}{49 - 25} = \frac{49}{24} \cong 2 \quad (5)$$

This illustrates the significance of skin effect when using large diameter wires. Using the example from **Figure 9** and Equation 5, reducing the wire diameter to  $2-\delta$  reduces the ACR to DCR ratio to approximately 1; however, the DCR will have increased twelvefold due to the significantly smaller wire diameter. Filling the space occupied by the single  $7-\delta$  wire with multiple  $2-\delta$  wires reduces DCR and consequently ACR. Replacing the single large  $7-\delta$  wire with an array of nine paralleled  $2-\delta$  wires (to fit in approximately the same total area as the original wire), DCR is now 136 percent of the original value ( $7^2/(9 \cdot 2^2)$ ). Thus ACR is now 1.36 times the original DCR, compared to twice the original DCR for the single large-diameter wire. Of course, this improvement comes at the penalty of more complicated multistranded wires – but these are kind of trade-offs that you need to consider when weighing cost/complexity against efficiency performance.



**Figure 11.** AC current distribution due to induced eddy currents for single wire (skin-effect only) (a); two adjacent wires with current in same direction (b); and two adjacent wires with current in opposite directions (c). Source: Reference 9.

## Proximity effect – single layer

In the previous section, we explained skin effect in the context of a single isolated wire. But rarely will you encounter a single isolated wire in practice. Flyback-transformer windings always consist of multiple turns, built up in multiple layers, including at least one primary winding and one secondary winding. They usually also include an auxiliary winding, and sometimes multiple secondary windings.

Skin effect alone is actually not that significant. What is far more important in the context of transformers is “proximity effect.” This is very similar to skin effect, but arises from the effect of the magnetic field that AC current flow in one wire causes on all adjacent wires. As you will see, proximity effect can build up rapidly as you add more layers of wire – to the point where the inner layers are carrying significantly more eddy current than load current.

We will first explain how proximity effect occurs in a pair of wires and then in a single layer of multiple wires. A common misconception is that proximity effect only applies to multiple-layer windings and does not occur in single-layer windings. But proximity effect does occur in single-layer windings, and its extent depends on the chosen wire diameter.

**Figure 11** shows the AC current flow in a single wire, the effect of two adjacent wires with current flow in the same direction, and the effect of currents in opposite directions. Note that for ease of illustration, the wire diameter is much greater than the penetration depth at the frequency of interest.

When current flows in two adjacent wires, the magnetic field from the AC current flow in each wire affects the current distribution of the other.

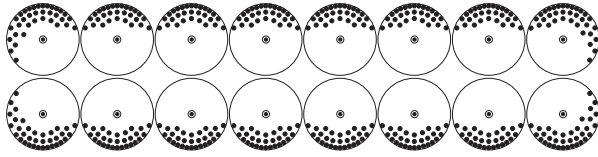
When currents flow in the same direction, the current distribution will tend toward the farther-away outer surfaces, and the current density at the facing edges drops. When currents flow in opposite directions, the current density concentrates at the inner-facing surfaces.

If you place multiple adjacent wires together in a typical single-layer transformer winding, the current flow will be in the same direction in each wire, assuming that they are connected in series. The proximity effect will reduce the current density at the adjacent-facing edges of each wire (except for the first and last wire in the layer), as shown in **Figure 12**.

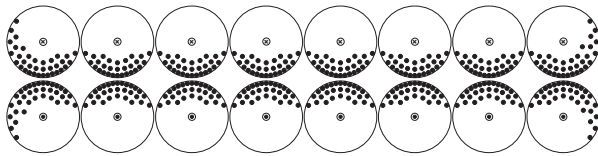
The current density is concentrated along the top and bottom surfaces of the wires in the layer, with little current flow in a central strip along the layer. This qualitatively highlights how much more significant and important proximity effect is compared to skin effect alone. Even for a single layer, if the wire diameter is too large compared to the penetration depth, proximity effect will occur.



**Figure 12.** AC current distribution due to proximity effect for a single-layer winding, with all currents flowing in the same direction.



**Figure 13.** AC current distribution due to proximity effect for a two-layer winding, with all currents flowing in the same direction.



**Figure 14.** AC current distribution due to proximity effect for a two-layer winding, with currents in each layer flowing in opposite directions.

### Proximity effect – multiple layers

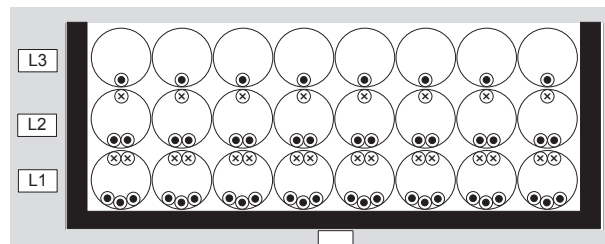
If you extend and implement the transformer winding over two layers, the proximity effect will impact the distribution within each layer as already seen – but each layer will also impact the other.

**Figure 13** illustrates how the current distribution is concentrated only along the outer surface of the wires in each layer. A two-layer flyback transformer primary or secondary winding could typically have this kind of winding structure.

Arranging a two-layer winding with currents flowing in opposite directions in each layer causes the current density to concentrate along the inner-facing surfaces of the wires in each layer, as shown in **Figure 14**. A forward-mode transformer would typically have this type of winding structure, where both primary and secondary current flows simultaneously in opposite directions. A flyback transformer with adjacent primary and secondary winding layers has this type of structure during the transition interval, when the primary current commutates to the secondary.

The illustrations in **Figure 13** and **Figure 14** are of course grossly simplified, with very large wire diameters, to illustrate proximity effect between

adjacent layers and how the resulting current concentration is worse than skin effect alone. Proximity effect becomes progressively worse with the addition of more winding layers, inducing canceling eddy currents in each layer that contribute significantly higher losses. **Figure 15** illustrates a three-layer 24-turn winding, with eight turns per layer. Current is flowing in the same direction (out of the page surface) in each winding layer. Once again, the wire diameter is much larger than the penetration depth in order to highlight the proximity effect.



**Figure 15.** AC current proximity effect for a three-layer winding, with currents in each layer flowing in the same direction.

Assuming a normalized 1-A current in the winding, with 24 turns the magnetomotive force (MMF) is 24 At. Since the wires are so large compared to the penetration depth, the magnetic field cannot penetrate far enough into any of the winding layers. A corresponding 24-At MMF on the inner surface of the first innermost winding layer (L1) cancels the 24 At of MMF of the air gap. Thus, the inner surface of each wire in layer L1 must carry 3 A each in order to generate 24 At of MMF across eight turns.

Since they are all connected in series, the net current in each wire must be 1 A. This means that a canceling 2-A current must flow in the opposite direction on the outer faces of the wires in L1 in order to get 1 A net. The magnetic field from that opposing 2-A current on the outer face of L1 will then force a canceling 2-A current to flow in the opposite direction on the inner face of L2 as shown in **Figure 15**.

Once again, since the net current in each wire in L2 must be 1 A, yet another 1-A canceling current will flow on the outer faces of L2. The magnetic field from the 1-A current on the outer face of L2 forces a corresponding canceling current in the inner face of L3. Because the wire diameter is so large that the magnetic field cannot penetrate far enough into the wire, these canceling currents develop to allow the magnetic field to propagate through the multilayer winding structure.

In the example in **Figure 15**, the initial expectation is that the conduction loss would be proportional to  $(3 * I^2)$ , since each of the three layers carries the same net current,  $I$ . Using Equation 6 to sum the contribution of the currents on all of the faces results in a loss proportional to:

$$P_{cond} \propto [I^2] + [I^2 + (2I)^2] + [(2I)^2 + (3I)^2] = 19I^2 \quad (6)$$

The total losses are more than six times higher than expected. Adding more layers with the same large wire diameter makes the situation progressively worse. For four layers, the loss would be  $(44 * I^2)$  vs.  $(4 * I^2)$ , 11 times higher. For five layers, the loss would be  $(85 * I^2)$  versus  $(5 * I^2)$ , 17 times worse; and so on for more layers.

Intuitively, you can see that by reducing the wire diameter sufficiently, the 3-A current on the inner face of L1 will eventually merge with the canceling 2-A current on the outer face of L1 to achieve both a net and an actual 1-A current flow in L1, reducing proximity effect considerably. Of course, as we noted earlier when discussing skin effect, a narrower wire diameter will have considerably higher DCR, which you must compensate for by using more paralleled strands of thinner wire.

## Proximity effect – passive layers

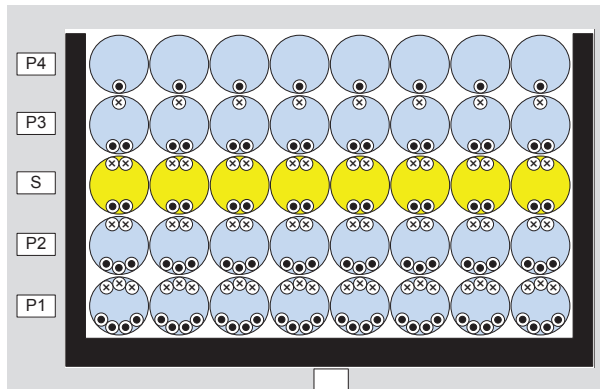
Passive layers are layers of a winding structure that do not carry any useful load current. In some cases they never carry useful current (such as an EMI shield), while in other cases they carry current only part of the time (such as a center-tapped secondary in a forward-mode push-pull converter – each half only carries current 50 percent of the cycle at most). During any interval when no load current flows, proximity effect-induced eddy currents can flow in the nonconducting winding, contributing to conduction loss even when not conducting.

A flyback transformer with interleaved primary and secondary layers is another example of a passive layer, when the nonconducting secondary is sandwiched between conducting primary layers. Even with a noninterleaved flyback transformer, the primary or secondary layer that sits closest to the core air gap will also be a passive layer when it is not conducting.

**Figure 16** illustrates this passive-layer proximity effect, where a single secondary layer, S, is sandwiched between two inner primary layers (P1, P2) and two outer primary layers (P3, P4). As before, assume that the wire diameter is much larger than the penetration depth and that a normalized 1-A net current in each wire where the total MMF is 32 At. Since the magnetic field cannot penetrate the wires, all of the required current to balance the MMF flows on the inner face of layer P1. This results in a 4-A current on the inner face of each wire in L1, with a canceling 3-A current on the outer face, and so on as before.

As shown in **Figure 16**, the secondary layer will have a 2 A of current induced along one face and a canceling 2 A of current induced on the opposite face. So while the secondary layer is in a nonconducting phase of the cycle and the net

current in the winding is zero, there are significant eddy currents induced in the layer, contributing extra conduction losses. In this case, the nonconducting secondary will exhibit losses eight times higher than the outermost primary layer, P4. Intuitively, as already noted, reducing the wire diameter sufficiently will cause the canceling eddy currents to merge and diminish greatly.



**Figure 16.** AC current proximity effect for a four-layer flyback primary winding, with a nonconducting secondary passive layer sandwiched in-between the primaries.

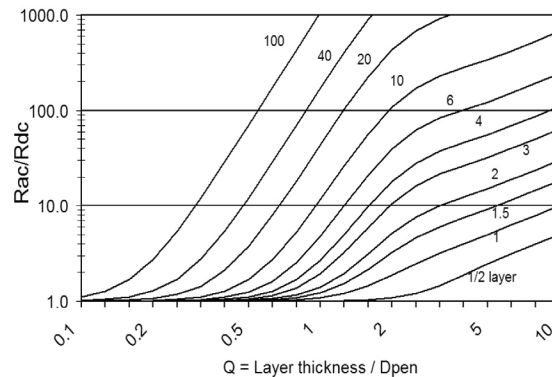
Again, these examples are gross oversimplifications to illustrate the fundamentals of proximity effect. But they do qualitatively highlight the impact of proximity effect, and the importance of carefully choosing the right wire diameter and winding construction. In many cases, adding more copper (either by increasing the wire size or adding more layers to fill the winding window) can actually be counterproductive, leading to higher transformer losses.

### ACR factor

Extensive analysis exists on the topic of ACR and proximity effect, most notably by Dowell [10]. Despite the large number of assumptions and the fact that they deal only with sinusoidal currents, Dowell's equations have proven very useful for predicting the ACR factor,  $k_p$  (the ratio of  $R_{AC}$  to  $R_{DC}$ ), as a function of layer ratio, Q (the ratio of layer thickness to penetration depth [ $D_{PEN}$  or  $\delta$ ]

at the frequency of interest), and layer count.

**Figure 17** (reproduced from [14]) illustrates the trade-off between wire size and layer count using Dowell's equations.



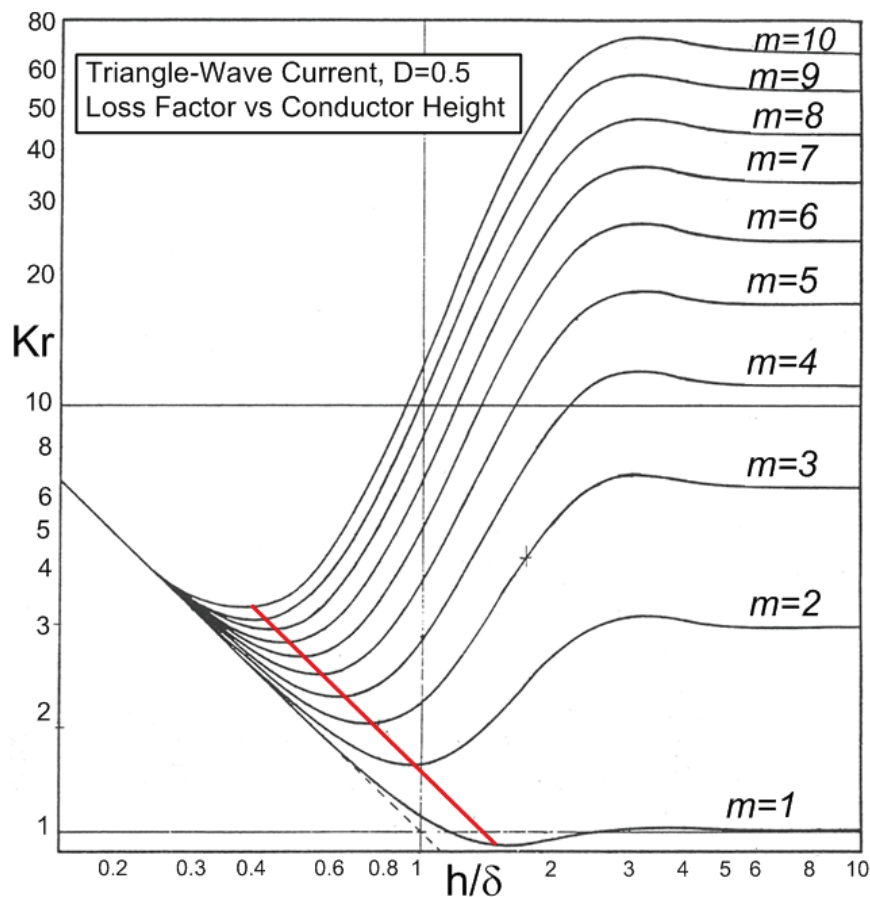
**Figure 17.** ACR factor  $R_{AC}/R_{DC}$  versus layer thickness and layer count. Source: Reference 14.

For low layer counts, you can use a larger wire size without incurring a major increase in the ACR/DCR ratio – a diameter twice the penetration depth will result in an ACR/DCR ratio of 2 for a single layer. However, even for a single-layer winding, ACR increases significantly if the wire size is much larger than the penetration depth. This highlights the significance of proximity effect, even for single-layer windings.

If you need to use a large number of layers, you must keep the wire size to a smaller fraction of the penetration depth as the layer count increases. For example, a 10-layer winding would require the layer height to be approximately half the penetration depth to keep the ACR/DCR ratio at 2.

Dowell's equations apply to sinusoidal waveforms at a single frequency. In flyback transformers, there is significant high-frequency harmonic content, particularly at smaller duty cycles (**Figure 8**). So although the ACR/DCR ratio may be acceptable when based on the penetration depth at the fundamental switching frequency, the ACR/DCR ratio will increase significantly for higher-order harmonics. This indicates that you may need to





**Figure 18.** Normalized effective resistance factor vs. layer thickness and layer count for triangular currents at a 50 percent duty cycle; reproduced from [9]. (Image courtesy of Bruce Carsten)

choose a much smaller wire diameter to reduce the losses associated with high-frequency harmonics.

Note that the graphs in **Figure 17** show the ACR/DCR ratio. When using a smaller diameter wire, DCR will increase rapidly, since it is inversely proportional to the square of the diameter. Although the ACR/DCR ratio decreases with smaller wire diameter, the absolute-value ACR will eventually increase. Moreover, since the flyback current waveforms have a significant DC component and a fundamental switching-frequency component, the DCR is significant and requires minimizing.

### Methods to choose the optimum wire size

Given the conflicting requirements to minimize both DCR and ACR, how can you choose the optimum wire diameter and strand count to minimize copper loss for a given design? We will propose two

methods here based on work published by Carsten [9] and Hurley [12].

#### Optimized wire size based on Carsten

**Figure 18** is reproduced from [9], where Carsten applied Dowell's equations to triangular currents at 50 percent duty cycle and evaluated the losses based on a Fourier expansion of the harmonics of the waveform. The "effective resistance factor,"  $K_R$ , is defined as the ratio of the effective resistance to the DCR, with the layer height,  $h$  (equivalent to the layer thickness in **Figure 17**), set equal to the penetration depth at the fundamental frequency,  $\delta_0$ . Carsten generated curves for the  $K_R$  factor versus the ratio of layer thickness to penetration depth for a range of layer counts. As you can see from the curves in **Figure 18**, for a given number of layers, there is a value of layer height where  $K_R$  is a minimum – this is the optimum layer height for that

layer count. Setting the layer height smaller than this value will result in higher losses due to increased DCR; a larger layer height will have higher ACR.

Note that although there is an optimum  $K_R$  value for each layer count, the actual  $K_R$  value will increase as the layer count increases – see the red diagonal line in **Figure 18**.

For a given transformer design and a target number of winding layers, you can use the curves in **Figure 18** to select  $h$  as a ratio of  $\delta_0$  at the fundamental frequency. Knowing the optimum value of  $h$ , you can calculate the optimum wire diameter,  $d$ . Depending on the transformer's bobbin geometry, choose the number of strands to fill the full layer widths as neatly as possible – it may be necessary to vary the chosen wire diameter up or down somewhat to achieve a good fill of the available window width. We will provide real-world examples of winding optimization later.

#### Optimized wire size based on Hurley

Hurley et al [12] propose an alternative method to choose the optimum wire size where you determine the optimum layer thickness for any arbitrary current waveform simply by evaluating the rms value of the current waveform and the rms of the derivative of the current waveform. This method gives reasonably accurate results – typically within 5 percent of the result calculable by using the first 30 harmonics of the waveform – but with significantly less computation and complexity.

Hurley generated equations for rms values of various common current waveforms, their derivatives and the corresponding optimum ratio of layer height to fundamental-frequency penetration depth. From that table [12], for a variable duty cycle triangle-wave current wave-shape (closest to the current wave-shape in a flyback transformer when operating in DCM or

TM), the ratio of the optimum wire diameter to penetration depth is given by:

$$\Delta_{OPT} = \sqrt[4]{\frac{\pi^2 \cdot D}{3 \cdot \psi}} \quad (7)$$

$$\text{where: } \psi = \frac{5p^2 - 1}{15}$$

Where  $\Delta = d/\delta_0$ ,  $d$  = wire diameter,  $D$  = duty cycle,  $p$  = number of layers.

Equation 7 can be used to estimate the optimum layer height as before. However, where the Carsten curves are available only for 50 percent duty cycle, the Hurley equations can be used for different duty cycles, and to plot the variation in optimum layer height as a function of duty cycle.

Using Equation 7 for duty cycle  $D = 0.5$ , the  $\Delta_{OPT}$  ratio ( $d/\delta_0$ ) for one-layer winding is 1.57, and for two-layer it is 1.07. These figures agree reasonably closely with the red line that highlights the minimum loss points on the various curves of **Figure 18**, approximately 1.6 and 0.95, respectively, (note that the horizontal axis of **Figure 18** is a log scale).

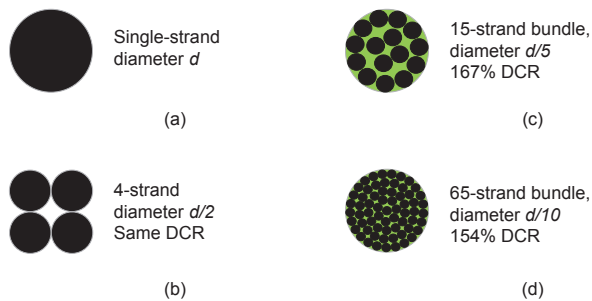
#### Wire type – solid core versus multistrand versus Litz

As we have shown, the ACR factor can be very significant due to skin and proximity effects. However, since ACR is a multiple of DCR, and the flyback currents contain a significant DC component, minimizing DCR is also important.

**Figure 19** compares a single-strand wire of diameter,  $d$ , and various combinations of smaller strand sizes that take up roughly the same space as a large single strand. (In this example, the effect of the small thickness of outer enamel insulation coating is ignored, although in practice you cannot always neglect this effect, especially for very small wire diameters where it becomes increasingly more



significant). As the number of strands of smaller wire increases, the DCR increases since the fill factor will worsen because of space lost to gaps in-between the individual strands. The fill factor for very small strands will be even worse due to the enamel insulation on each strand. However, if the frequency is high enough, the decrease in ACR factor of the



**Figure 19.** Comparison of single versus multistrand wire bundles.

stranded wire may be sufficient to justify an increase in DCR. By using a sufficient number of wire strands, an acceptable DCR may also be achieved.

For bundles with a high number of multiple strands, twisting and bundling is very important in order to ensure that all strands equally occupy all positions in the cross-section of the bundle along each turn around the core center leg. Litz wire is usually woven together from a number of sub-bundles to help achieve this goal. If a bundle is poorly twisted, such that some strands occupy central positions in the bundle for all or most of the time, the losses can actually be dramatically worse. In this case, most of the AC current will flow in the outer strands only, increasing the effective resistance. Even worse, besides not carrying any (or as much) useful current, the central strands can actually suffer large losses due to induced eddy currents from the current flow in the outer strands.

Litz wire is commonly used for very high frequencies where the ACR factor would be significant. For example, for a Litz bundle using 0.1-mm wires, the

frequency would need to be 575 kHz before the penetration depth equals the 0.1-mm diameter.

The required number of strands,  $N$ , would depend on the rms current and required DCR.

At such high frequencies, Litz construction has advantages if you choose the correct wire size and strand count for the frequency and current waveform of interest. A bundle of  $N$  strands of Litz wire is equivalent to  $\sqrt{N}$  layers. So a single physical layer of Litz wire is actually equivalent to  $\sqrt{N}$  layers when using **Figure 18** or the Hurley equations from reference [12] to determine the optimum strand diameter. A poorly chosen Litz bundle (wire diameter and strand count for the frequency of interest) might actually make losses worse.

Litz wire is rarely used and probably offers little ACR advantage for more conventional flyback switching frequencies (<150 kHz typical for EMI reasons). Moreover, Litz wire costs more, has poorer window utilization and comes with handling difficulties. Since there are many strands of small wire diameters, sometimes a small percentage of strands can break, which can impact the effective resistance, and result in induced eddy current losses in the nonconducting strands. Soldering the small wire diameters can be difficult at the transformer terminations; high soldering temperatures can actually vaporize some strands, again leading to a percentage of nonconducting strands.

## Leakage inductance

Leakage inductance is caused by the magnetic flux from one winding in a transformer that does not couple to other windings. It is due to the magnetic flux in the spaces and gaps between windings, which stores energy in those gaps, in the same way that energy is stored in the air gap of a ferrite core. The energy in the leakage inductance is typically

dissipated external to the transformer. Several of the references – [1], [11], [13], [14] – discuss the causes and consequences of leakage inductance in more detail.

For flyback transformers, minimizing leakage inductance is very important, since in most cases the leakage energy dissipates in an external snubber or clamp circuit. As you will see later, it is also important to minimize the ratio of leakage to the magnetizing inductance in order to minimize the amount of magnetizing energy lost to the clamp circuit.

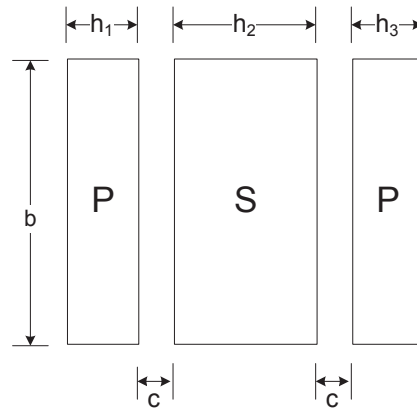
### How to estimate and minimize leakage inductance

Several published methods explain how to estimate leakage inductance based on the physical geometry of the windings and the layer structure in a transformer. **Figure 20** and Equation 8 show a method used by Carsten [9]. This method assumes that all winding layers are the same full width,  $b$ , and cannot be used with some partial-width layers. Note, that the leakage inductance to any partial-width layers will be much higher, increasing as the width of the partial layer narrows.

$$L_{LEAK} = \frac{\mu_0 \cdot N^2 \cdot MLT \cdot (\sum h + 3 \sum c)}{3b} \cdot \frac{1}{m^2} \quad (8)$$

Following are the parameters of Equation 8:

- $N$  = number of turns on the winding to which the leakage is referred
- $MLT$  = Mean length per turn of the windings
- $\sum h$  = sum of the heights of all winding layers
- $\sum c$  = sum of the heights of the spacing gaps between winding layers
- $m$  = level of interleaving (number of winding “portions”)
- $b$  = bobbin winding breadth (width of the winding layer)

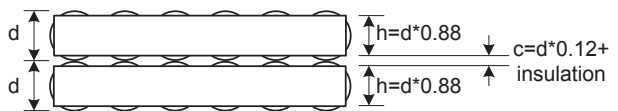


**Figure 20.** Typical interleaved flyback transformer winding layer spacing.

Per the assumptions used in Dowell’s equations [10], each winding layer of circular wire diameter  $d$  converts to an equivalent rectangular block of the same cross-section. Thus,  $h$  is not quite the same as  $d$  (Equation 9):

$$h^2 = \pi \cdot \frac{d^2}{4} \Rightarrow h = d \cdot \sqrt{\frac{\pi}{4}} = d \cdot 0.886 \quad (9)$$

As **Figure 21** shows, you can use the wire diameter and Equation 9 to calculate  $h$  for each winding layer. You can calculate the spacing,  $c$ , using the thickness of an intervening tape or insulation, plus the thickness or enamel coating or any other insulation on the wire, plus the extra gap due to the conversion of diameter  $d$  to an equivalent  $h$ .



**Figure 21.** Converting each winding-layer pair into equivalent  $h$  and  $c$  values.

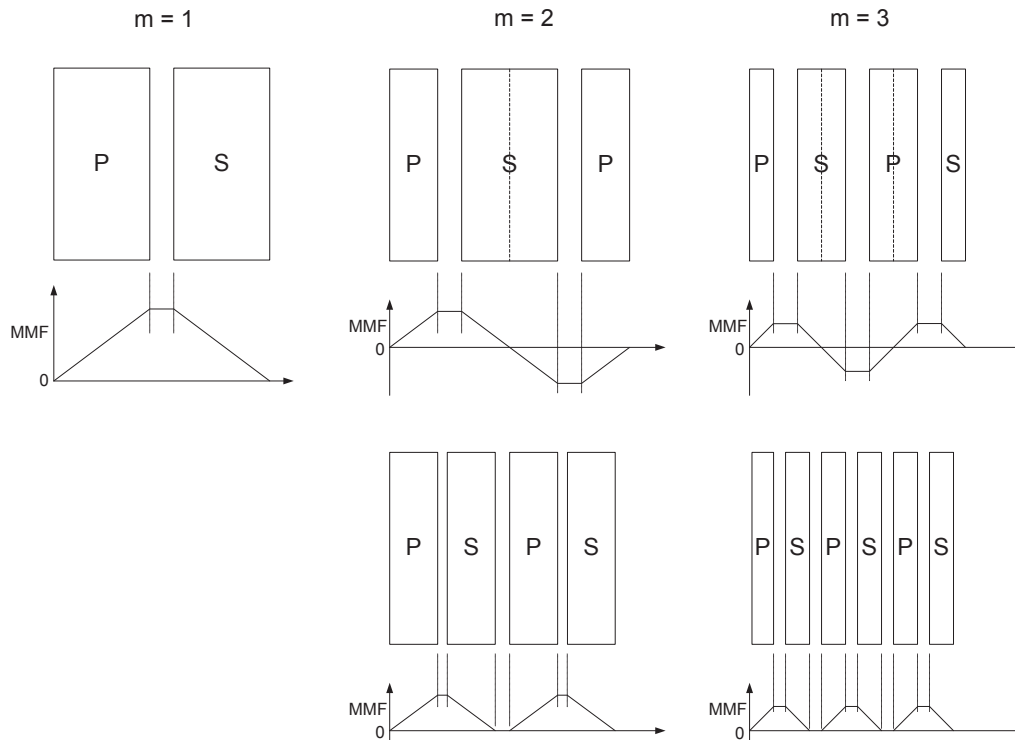


Figure 22. Different levels of interleaving to reduce leakage inductance.

## Leakage inductance reduction and minimization

Leakage inductance depends largely on the physical winding geometry; you can estimate the leakage inductance from this geometry. An inspection of Equation 8 shows that you can reduce the leakage inductance by:

- Interleaving – increasing the value of  $m$ .
- Using a wider bobbin winding width – maximizing  $b$ .
- Minimizing turns  $N$  and mean length per turn  $MLT$ .
- Minimizing the thickness and quantity of spacing gaps,  $c_n$ , between winding layers.
- Minimizing winding layer thicknesses,  $h_n$ , and the number of layers.

## Interleaving

Figure 22 shows examples of different levels of interleaving to reduce leakage inductance in the context of a conventional forward-mode transformer. But the same principles also apply

to a flyback transformer during the transition interval, when primary and secondary current flow simultaneously, and when leakage inductance is relevant.

In the first example, the primary and secondary are placed side by side with no interleaving. The corresponding MMF diagram underneath shows how the primary MMF builds up to a maximum value, and is then canceled by the secondary, back to zero. The MMF diagram shows just one portion or region of MMF build up and return to zero – so in this example with one portion,  $m = 1$ .

The primary and secondary are interleaved in the second examples. Both interleaving methods are different, but equivalent. That is because in both cases, the MMF builds to a peak and declines back to zero over two separate portions, so in both cases  $m = 2$ . Similarly, the third example shows two different interleaving methods, but as both are equivalent in terms of interleaving portions,  $m = 3$  in both cases.

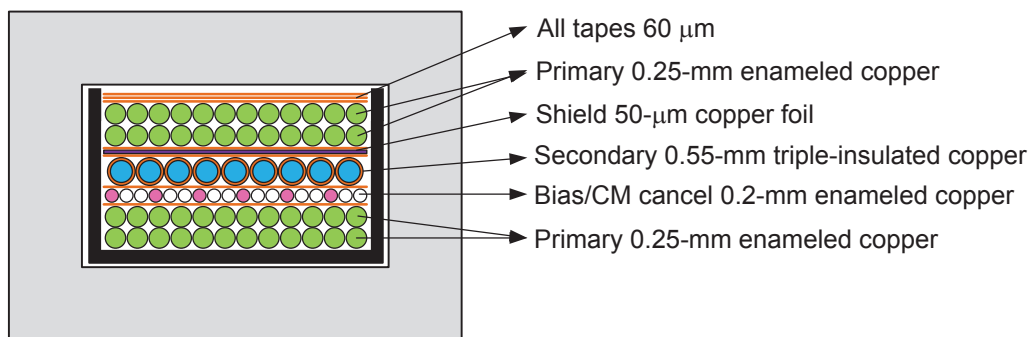
Since leakage inductance is inversely proportional to  $m^2$ , a first level of interleaving with two portions (i.e.,  $m = 2$ ) is expected to result in a four-fold decrease in leakage inductance. By changing from  $m = 1$  to  $m = 2$ , as shown in **Figure 22**, the winding structure changes from a single primary-secondary interface to two interfaces, one at each face of the secondary. In the interleaved case, there are now two interface spacing gaps,  $c$ ; both are likely to be approximately the same dimension as the single  $c$  in the noninterleaved case. So in reality, the factor  $\Sigma c/m^2$  in Equation 8 only decreases by a factor of two, and the leakage inductance will really only decrease by half. Nonetheless, this is a significant reduction and is usually very beneficial.

However, the designer should be aware that interleaving primary and secondary windings may possibly increase transformer cost, complicate EMI and safety compliance (since there are now two primary-secondary interfaces), and increase transformer interwinding capacitance.

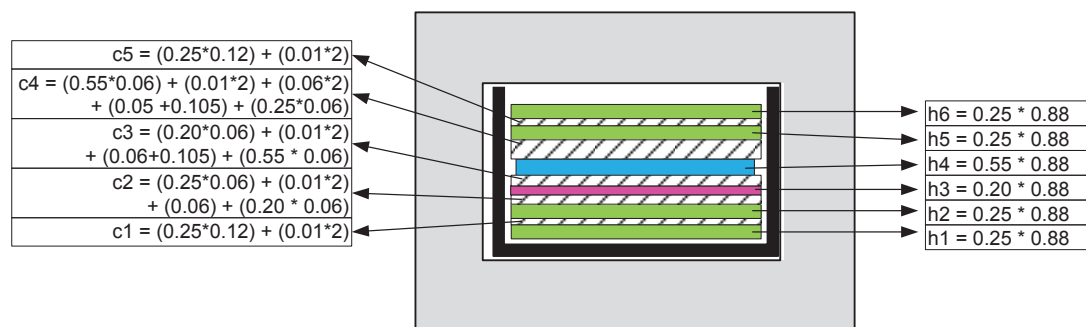
### Leakage inductance estimation – worked example

We now use Equation 8 to estimate the leakage inductance of the typical flyback transformer winding structure illustrated in **Figure 23**. This structure consists of a split primary with auxiliary bias and secondary layers sandwiched in-between. Each half primary is wound over two layers, and secondary and bias layers are wound over single layers. There is also a shield layer inserted between the secondary and outer half primary. **Figure 23** lists all of the wire sizes.

We converted all round wire diameters to an equivalent rectangular block with the same cross-section. The switching frequency of the target design was 60 kHz, with a  $\delta \sim 0.31$  mm. The shield is sufficiently thin (0.05 mm, one-sixth of  $\delta$ ), so that for simplicity, we included it as part of the insulating space between the secondary and outer half primary (**Figure 24**).



**Figure 23.** Interleaved flyback transformer winding structure.



**Figure 24.** Conversion of sample interleaved flyback transformer winding structure to layer heights  $h_n$  and spacing gaps  $c_n$ .

When you know the heights,  $h_n$ , of all of the conducting layers and the spacing gaps,  $c_n$ , of the insulating layers, you can estimate the leakage inductance using Equation 8. In this case, the primary total turns  $N = 34$ ; we used the RM10 bobbin, with  $MLT = 52$  mm. The primary is interleaved with two portions,  $m = 2$ ; the winding breadth  $b = 9$  mm. (The bobbin nominal dimension is actually 10 mm, but due to wire insulation and entry/exit wire routing, the layer fill is typically ~90 percent of the available width).

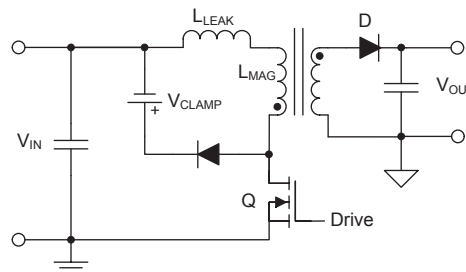
$$L_{LEAK} = \frac{\mu_0 \cdot 34^2 \cdot 52 \text{ mm} \cdot (1.54 \text{ mm} + 3 \cdot 0.78 \text{ mm})}{3 \cdot 9 \text{ mm}} \cdot \frac{1}{2^2} = 2.71 \mu\text{H} \quad (10)$$

In Equation 10, 2.71  $\mu\text{H}$  is reasonably close to the measured leakage inductance of 3.2  $\mu\text{H}$ . The difference comes down to practical nonidealities of the actual winding, such as tape creasing, entry/exit thickness and return wires. Nevertheless, we have shown how to estimate leakage inductance for a given winding structure and how to objectively compare different winding structures for leakage inductance performance. We also have shown the impact of the chosen bobbin shape/geometry on leakage inductance.

### Effect of the clamp voltage value on transformer leakage inductance losses

In a single-switch flyback converter, you typically need a clamp circuit to limit the drain voltage of the switch; the clamp circuit absorbs energy stored in the transformer's leakage inductance and, depending on the value of the clamp voltage, will also absorb a fraction of the magnetizing energy. In **Figure 25**, you can see that immediately after transistor Q turns off, all of the primary current

diverts into the clamp circuit (represented in **Figure 25** by the voltage source,  $V_{CLAMP}$ ). A voltage will develop across the leakage inductance,  $L_{LEAK}$ , that is equal to the difference between  $V_{CLAMP}$  and the reflected secondary voltage,  $V_{REFLECTED}$ . Consequently, the current in the leakage inductance (which is also the primary current) will decrease at a rate dependent on the difference between the two voltages; thus, magnetizing current will flow into the clamp circuit until the current in the primary decays to zero.

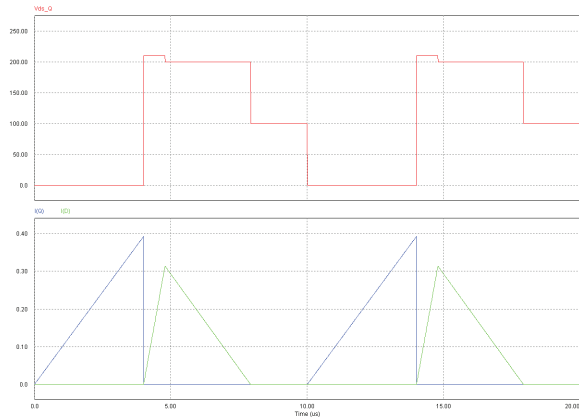


**Figure 25.** Simplified flyback schematic showing a clamp/snubber network as an ideal voltage clamp.

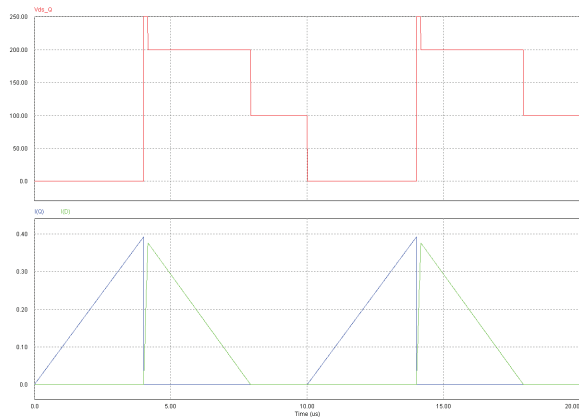
The rate at which the current decreases in the leakage inductance determines the rate at which the current transfers to the secondary. **Figure 26** illustrates this process.

In **Figure 26a**, where the clamp voltage is only 10 percent higher than the reflected secondary voltage, a considerable amount of the magnetizing energy is lost in the clamp. The current transferred to the secondary is significantly lower compared to **Figure 26b**, where the clamp voltage is 50 percent higher than the reflected secondary voltage.

In an extreme case, where the reflected secondary voltage is equal to the clamp voltage, no voltage is available to force the current in the leakage inductance to decay faster than the current in the magnetizing inductance; thus, no magnetizing current can be transferred to the secondary. The clamp circuit will absorb all magnetizing energy and leakage energy.



(a)  $V_{CLAMP} / N \cdot V_{REFLECTED} = 1.1$



(b)  $V_{CLAMP} / N \cdot V_{REFLECTED} = 1.5$

Figure 26. Comparison of current transfer to the secondary winding (a) versus the voltage-clamp level (b).

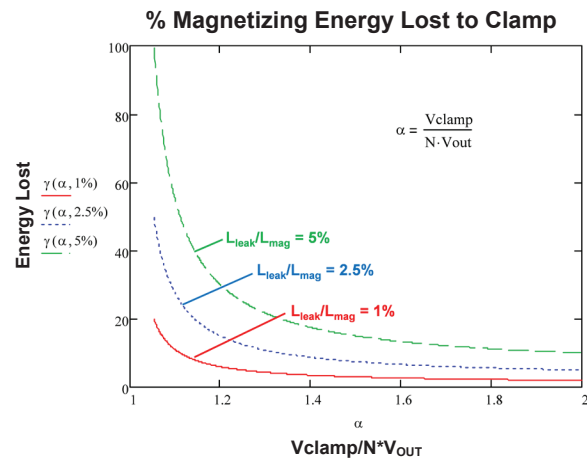


Figure 27. Graph of percentage energy lost to the clamp versus the clamp level and leakage/magnetizing inductance ratio.

Figure 27 shows the percentage of magnetizing energy lost in the clamp,  $\gamma$ , as a function of the ratio of clamp voltage to the primary reflected voltage,  $\alpha$ , and the percentage ratio of the leakage to the magnetizing inductance.

The energy lost in the clamp increases rapidly as the ratio of the clamp to the reflected voltage drops below 1.2. This loss is also very sensitive to the leakage-to-magnetizing inductance ratio.

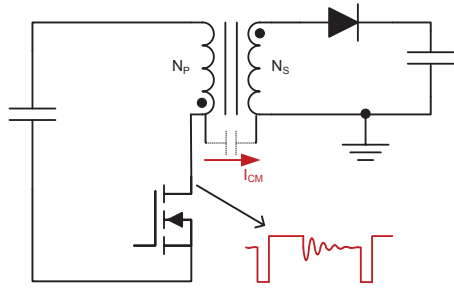
Although selecting a lower clamp voltage may allow use of a lower-voltage switching transistor with a lower  $R_{DS(on)}$ , the added clamp loss may easily outweigh the expected benefits.

## EMI shielding and cancellation techniques

### Causes of EMI

Reference [15] gives a very good and thorough explanation of EMI causes and solutions. This section will focus solely on the CM interference that occurs from flyback transformer capacitance. We will also discuss techniques to minimize CM EMI through transformer design and construction.

Figure 28 shows the CM current,  $I_{CM}$ , that flows between the primary and secondary transformer windings caused by the voltage waveform imposed across the interwinding capacitance. Since the primary voltage swing is typically much greater than the secondary voltage (for offline AC/DC applications),  $I_{CM}$  will flow from the primary to the secondary.  $I_{CM}$  will then flow to earth through the impedance from the output circuit to earth, causing a potential CM interference issue.



**Figure 28.** CM current flow from the primary to the secondary due to the switching voltage waveform across the primary-secondary interwinding capacitance.

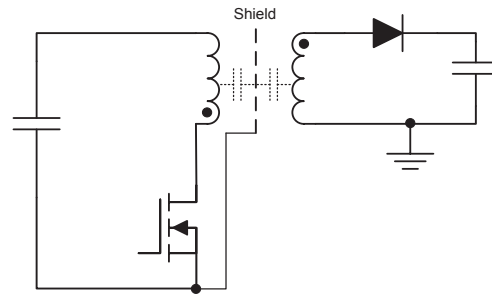
In many applications, the output return (negative  $V_{OUT}$ ) terminal is often directly connected to earth anyway – resulting in the worst-case potential CM EMI result. This CM EMI needs filtering at the power-supply input using a combination of CM filter chokes and Y-capacitors. Any steps to reduce CM EMI at the source can result in significant cost, size and power-loss reductions for the EMI filter.

In order to minimize CM EMI, you can construct the transformer to minimize the interwinding capacitance, which in turn will minimize  $I_{CM}$ . However, reducing the capacitance typically involves increasing the thickness of dielectric spacing between the primary and secondary windings (moving them further apart), and/or reducing the surface area of overlap between them. Both of these changes will lead to poorer primary to secondary coupling and increased leakage inductance. Remember that increased leakage inductance will increase losses. So there is usually a trade-off between low-leakage inductance construction for efficiency, versus low capacitance for EMI.

### EMI mitigation methods I – transformer shields

Electrostatic shields help reduce CM EMI when added to the transformer [15]. As discussed earlier, the shield should be as thin as possible in order to minimize eddy current loss in the shield due to proximity effect.

The shield typically connects back to local primary ground as shown in **Figure 29**, or sometimes connects to the input DC bulk capacitor's positive terminal – this is possible because that point is also a quiet AC ground. With the shield in place,  $I_{CM}$  will flow into the shield and back to local primary ground instead of flowing to output and from there back to earth.



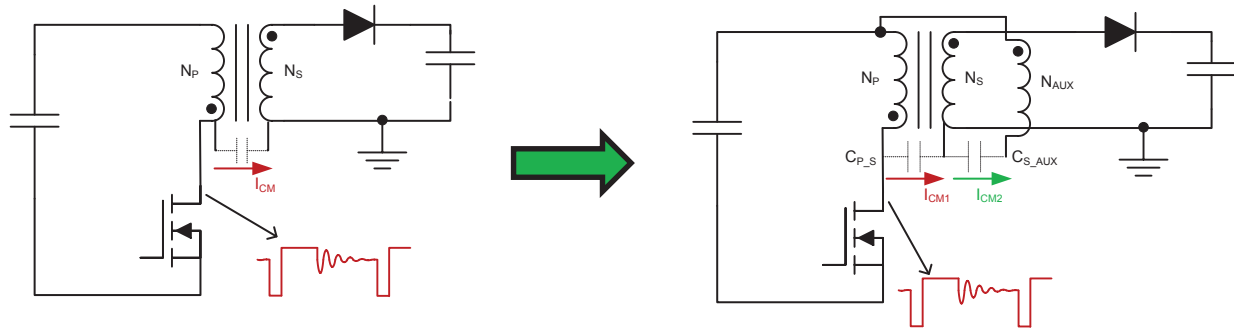
**Figure 29.** Flyback transformer with shield layer between the primary and secondary.

Even though  $I_{CM}$  is trapped by the shield and returned to local primary ground, capacitance still exists between the shield and secondary winding. Since the voltage induced in the one-turn shield is not the same as in the secondary winding (unless you are using a one-turn secondary), there is still some CM current flow between shield and secondary. Therefore, although the shield helps greatly attenuate CM EMI, the shield cannot eliminate it completely. A disadvantage with interleaved windings is that the number of primary-secondary interfaces increases – more shield layers are usually required, one at each primary-secondary interface.

### EMI mitigation methods II – CM cancellation windings and CM balance

As an alternative to shields, you can introduce a separate auxiliary cancellation winding,  $N_{AUX}$ , as shown in **Figure 30**. The polarity of the auxiliary winding is oriented to produce a canceling current of opposite polarity to the current injected from the





**Figure 30.** Flyback transformer with additional auxiliary cancellation winding.

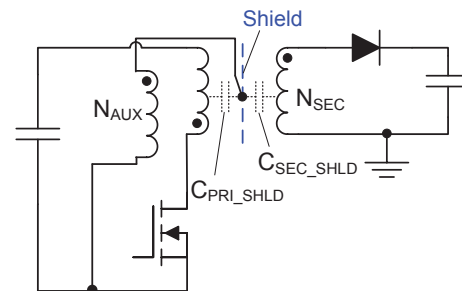
primary. By adjusting the number of turns  $N_{AUX}$  and the secondary-auxiliary capacitance,  $C_{S\_AUX}$ , you can make the magnitude of  $I_{CM2}$  equal to  $I_{CM1}$ . Thus,  $I_{CM1}$  from the primary is canceled, and close to zero net CM current will flow to the output, and from there to earth.

This approach depends on tight manufacturing controls over the value of  $C_{S\_AUX}$ . If  $C_{S\_AUX}$  varies, then the CM nulling will not be perfect. Even if the manufacturer tightly controls  $C_{S\_AUX}$  capacitance, its value will potentially vary as the ambient temperature changes and as the transformer's temperature changes due to internal self-heating. Over the power supply's lifetime, the capacitance will also change as multiple heat/cool cycles cause the insulating tapes to expand, compress and harden over time – such that the capacitor dielectric thickness can change.

As an alternative to CM cancellation, you can arrange the transformer windings to achieve CM balance. With this method, the average voltage at both ends of the interwinding capacitances are arranged to be the same amplitude and polarity, thus minimizing or nulling the CM current through the parasitic capacitance in a way that does not rely on the value of the capacitance itself.

**Figure 31** shows an example where a shield is

deployed between primary and secondary windings as before – but rather than connect the shield to an AC ground, it is instead driven by an auxiliary winding, with  $N_{AUX} = \frac{1}{2} N_{SEC}$ . This ensures that the average voltage on the shield is the same as the average voltage on the secondary winding. Since the average voltage at both ends of  $C_{SEC\_SHIELD}$  is the same, it is balanced for CM, so there will be zero average CM current flow from the shield to the secondary winding.

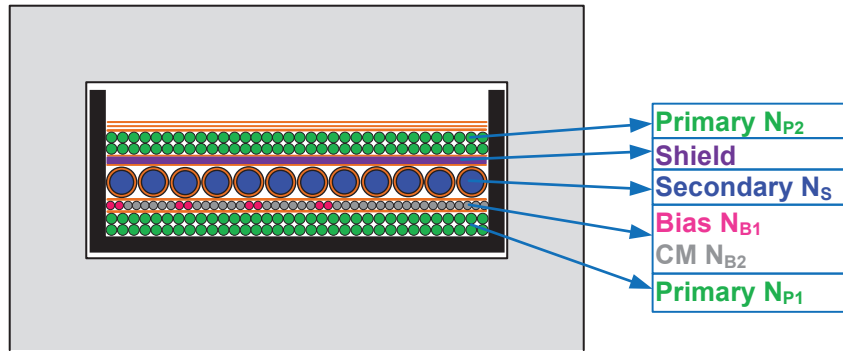


**Figure 31.** Flyback transformer with shield plus auxiliary winding for CM balance.

### CM balance – design example

**Figure 32** is an example implementation of CM balance in a flyback transformer winding structure.

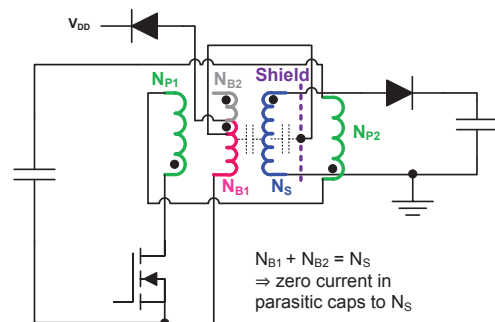
**Figure 33** shows the equivalent schematic, with the windings colored to match the equivalent physical winding. The structure is interleaved, with the primary split into two half primaries and all other windings sandwiched in-between.



**Figure 32.** Flyback transformer winding structure with CM balance.

Between the inner half primary and the secondary is an auxiliary winding that serves multiple functions. First, as the primary-side bias winding (pink strands), it supplies bias power for the primary controller. Second, it is wound with multiple parallel strands (pink and gray strands) that fill the full bobbin width and serve as a shield layer between the inner half primary and the secondary winding. Third, there are extra turns (gray strands) such that the total turns in that layer match the secondary winding turns in order to achieve CM balance between the layers.

A shield layer (purple) is placed at the other interface between secondary and outer half primary. Again, the shield in this case is not tied to an AC ground, but is instead driven by a tap on the auxiliary winding, such that the average voltage on the shield matches the average voltage on the secondary, again achieving CM balance.



**Figure 33.** Equivalent schematic of the flyback transformer shown in Figure 32.

Using the schematic in **Figure 33**, the arrangement is explained using the voltages in the circuit. The output voltage is approximately 20 V, so the average voltage for the flyback phase across the secondary will be approximately 10 V. With a 6T secondary, this is equivalent to 1.67 V/T.  $N_{B1}$  is a 4T winding to generate the required bias rail, and  $N_{B2}$  consists of a further 2T, for a total 6T of auxiliary winding to match the 6T secondary winding. Consequently, the capacitance between auxiliary and secondary has the same voltage waveform and amplitude at both sides, so it is CM-balanced.

There is a tap on the  $N_{B1}$  winding after 3T to drive the shield. Thus, the average shield voltage will also be 10 V. Once again, the same average voltage on both the secondary winding and the shield layer (10 V) achieves CM balance. The major advantage of this arrangement is that it does not rely on the value of the parasitic capacitance, or controlling it to a required value. CM balance is assured regardless of capacitance value or variations.

In practice, you will need to adapt the implementation and structure used to achieve CM balance depending on your specific application's circumstances. Very often, figuring out the best implementation for a given case involves trial and error.

It is difficult to estimate the cost/performance trade-offs between applying CM mitigation inside the transformer versus external CM EMI filtering. Shielding and CM balance layers inside the transformer will add material and labor cost to the transformer – but they can be very effective at reducing CM noise in a way that does not add significantly to the overall size or power loss. On the other hand, adding an external CM filter choke, or increasing its size/inductance is relatively straightforward. But this will incur extra cost as the external CM choke will occupy more space and incur extra losses.

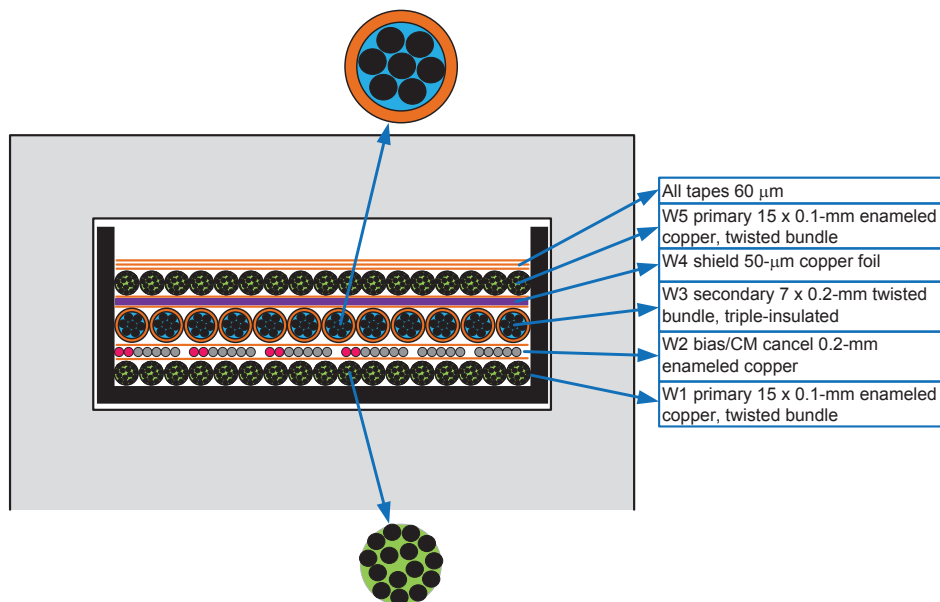
One further important point: the secondary-side rectifier in **Figure 33** is shown in the conventional high-side location. But locating the rectifier (diode or synchronous rectifier [SR]) on the low side (for gate-drive ease), will change the polarity of the secondary winding with respect to the auxiliary/bias layer. This means that a winding with opposite polarity is required to drive the shield – ideally with an inverted auxiliary winding and a bias rectifying diode placed in the return leg. This preserves all relative winding polarities and maintains CM balance.

However, if you are also using the auxiliary/bias winding for primary-side regulation (PSR), it is not possible to put the bias rectifying diode in the return leg. In this case, the shield drive winding  $N_{B2}$  must wind in the opposite direction, with appropriate turns, to provide the necessary balance versus the secondary layer. In such cases with a secondary rectifier in the return leg, it can be simpler and more cost-effective to use two shields on either side of the secondary driven by an anti-phase winding  $N_{B2} = 1/2 N_{SEC}$ .

## Real-world examples of EMI and efficiency improvements

### Transformer No. 1

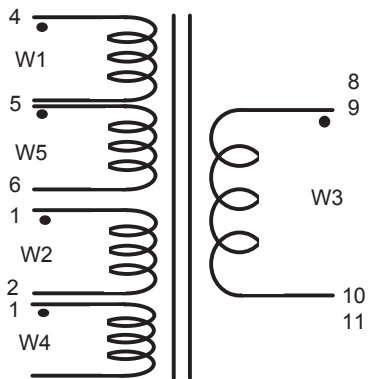
Using the TI [UCC28630EVM572](#) (EVM572) [16] as a starting point, we reviewed the structure of its transformer. We identified possible further improvements to the structure, and implemented and tested several alternative versions against the original transformer for EMI and efficiency performance. The evaluation module (EVM) demonstrates a 19.5-V output reference design



**Figure 34.** UCC28630EVM572 transformer winding construction (transformer No. 1).

using the [UCC28630](#) DCM/CCM PSR controller, and is rated for an average output power of 65 W, or up to 130 W of intermittent peak power.

**Figure 34** illustrates the structure of the original transformer, while **Figure 35** is the equivalent electrical schematic. The transformer uses a standard RM10/I core set and bobbin. The windings are interleaved – the primary split into two half primaries, with all other windings sandwiched in-between. A twisted bundle is used for each half primary, comprising 15 strands of 0.1-mm wire, with each half primary wound over a single layer.



**Figure 35.** UCC28630EVM572 transformer schematic (transformer No. 1).

Between the inner half primary and the secondary is an auxiliary winding.

The secondary uses a twisted bundle of seven strands of 0.2-mm wire; the outside of this bundle is triple-insulated for safety compliance. Using two triple-insulated bundles in parallel fills the full layer and reduces the total resistance of the secondary. A shield layer is placed between the secondary interface to the outer half primary. As noted previously, the shield in this case is not tied to an AC ground but is instead driven by the bias-rail tap on the auxiliary winding so that the average voltage on the shield is close to the average voltage on the secondary, to get close to CM balance.

We designated this standard EVM572 transformer as transformer No. 1.

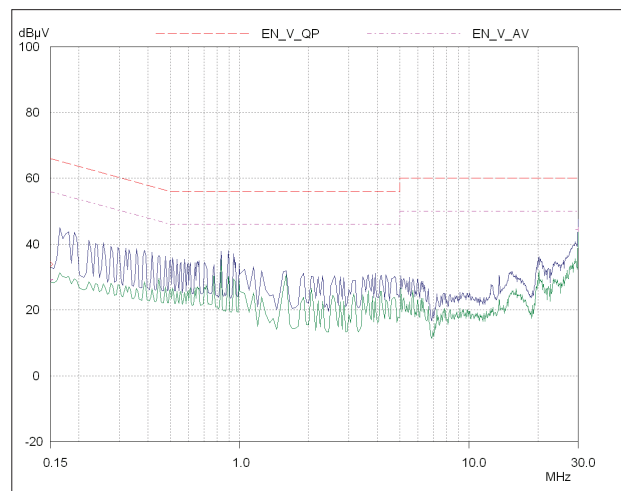
#### Analysis of transformer No. 1 performance

We measured transformer No. 1 for leakage inductance, EMI and efficiency performance in the EVM572 board. Since the EVM efficiency was typically worse at low line, the efficiency performance with all transformer variants was at 115 VAC. We tested conducted EMI at both 115 VAC and 230 VAC, and found it worse at low line, 115 VAC.

We measured the leakage inductance at  $4.51 \mu\text{H}$  across the full primary terminals, with the main secondary shorted (all other windings open).

The full load efficiency at 65-W load, 115-VAC/60-Hz input was 87.7 percent, or 9.11 W of total power loss (not including the output cable drop).

**Figure 36** shows the typical conducted EMI performance at 115 VAC, 65 W. The results show very good pass margin due to the balanced CM shielding structure of this transformer, as previously discussed.



**Figure 36.** Conducted EMI plot for the UCC28630EVM572 with transformer No. 1. Conditions: input voltage 115 VRMS, output power 65 W, output return connected to earth; quasi-peak (QP) result in blue, average (AVG) result in green.

Reviewing the construction from a loss perspective, the primary wire strand diameter is 0.1 mm. Since the EVM's full-load switching frequency is 60 kHz, the fundamental frequency  $\delta$  is approximately 0.31 mm. Thus, the 0.1-mm strand  $h/\delta$  ratio is only 0.29 – this is very low. Assuming that the 15-strand bundle is sufficiently well twisted and woven to give Litz-like performance, this construction is equivalent to almost a four-layer winding ( $N$ -strand bundle/Litz  $\Rightarrow \sqrt{N}$  layers). Even with four layers, going back to **Figure 18**, the optimum  $h/\delta$  ratio is approximately 0.7. Clearly, there is room for further optimization.

The secondary has seven strands of 0.2-mm diameter wire and is thus equivalent to a  $\sim 2.6$ -layer winding. Again looking at **Figure 18**, the optimum  $h/\delta$  ratio is approximately 0.9, but the actual  $h/\delta$  ratio is 0.57, so again there appears to be room for further optimization.

The next sections will investigate various alternate transformer constructions and compare performance. As we mentioned in the introduction, we changed only the transformer winding structure, keeping all other components on the board unchanged for all tests, including the transformer core material (Ferroxcube 3C95) and the turns count for all windings.

## Transformer No. 2

For transformer No. 2 a structure similar to transformer No. 1 is used, but with two layers for each half primary and a single layer for the secondary. For a two-layer half-primary winding, the optimum  $h/\delta$  ratio is approximately 0.9 according to **Figure 18**. At a 60-kHz switching frequency,  $\delta$  is 0.31 mm, giving  $h = 0.28$  mm. Converting from rectangular layer back to round wire, the optimum diameter is then approximately 0.32 mm.

The RM10/I bobbin winding window width is 10 mm, which allows for a target of 9 mm (90 percent) for the wires. We assumed an enamel coating thickness of 0.02 mm for all standard wires and this is added to get the actual wire outer diameter (OD). We assumed that the triple-insulation thickness was 0.2 mm, again added to the bare-copper diameter to get the actual wire OD. To choose the best wire diameter and strand count requires several iterations to find the combination that fits the available width comfortably, using complete full winding layers. Full-width layers are important to minimize leakage inductance.

Using the optimum wire diameter – 0.315 mm (SWG30) wire with OD = 0.34 mm – four strands would not fit in two layers, while three strands would not fully fill two layers. Since the curves in **Figure 18** show a reasonably flat characteristic near the optimum value, there should be little penalty in adjusting the wire diameter up or down slightly to get a better full-layer-width fill factor. For this reason, we decreased the wire size to 0.25 mm (0.27-mm OD), using four parallel strands to completely fill two layers with 17T for each half primary.

Regarding the secondary layer, for a one-layer winding, the optimum  $h/\delta$  ratio is approximately 1.6, again according to **Figure 18**. At a 60-kHz fundamental switching frequency,  $\delta$  is 0.31 mm, giving  $h = 0.5$  mm. Converting from rectangular layer back to round wire, the optimum diameter is then approximately 0.56 mm. Considering 0.55-mm triple-insulated wire, with OD = 0.75 mm, six turns of two strands will neatly fill the full available layer width.

As **Figure 34** showed, the original auxiliary bias layer is not completely full, so the shielding will not be as effective as it could be. For transformer No. 2, we added an extra strand to the auxiliary bias

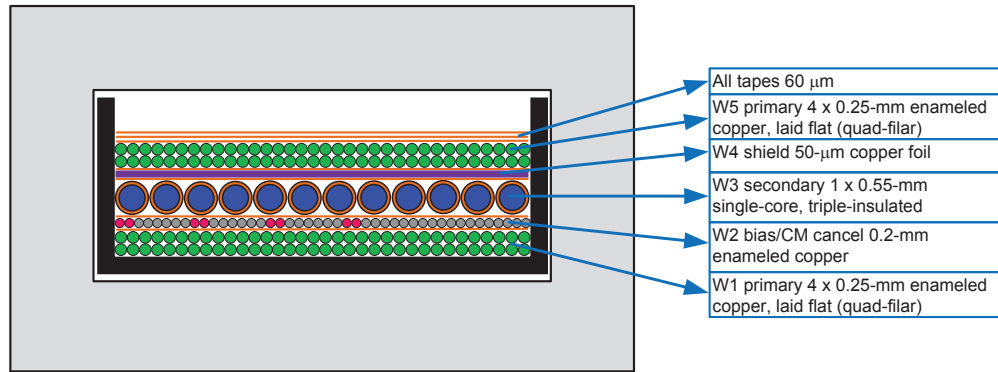


Figure 37. Transformer No. 2 winding construction.

layer for a total of eight strands. Transformer No. 2's schematic is the same as **Figure 35**. **Figure 37** illustrates the final winding cross-section and construction of transformer No. 2.

#### Analysis of transformer No. 2 performance

We checked transformer No. 2 for leakage inductance, EMI and efficiency performance in the EVM572 board.

We measured the leakage inductance at 3.24 µH across the full primary terminals, with the main secondary shorted (all other windings open). This shows a significant reduction of 30 percent compared to transformer No. 1.

The full load efficiency at 65-W load, 115-VAC/60-Hz input was 89.03 percent, or 8.01 W of total power loss (not including the output cable drop). This is a 1.3 percent efficiency improvement or a loss reduction of 1.10 W (12 percent lower total losses in the whole board) – with no other change but the transformer.

**Figure 38** shows typical conducted EMI performance at 115 VAC and 65 W. This result is similar to transformer No. 1, as expected, since we used a similar CM balance approach.

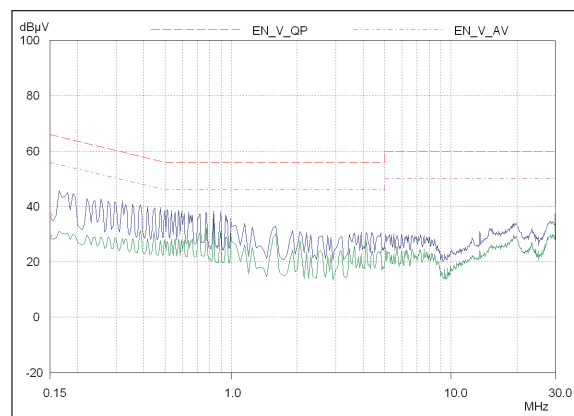


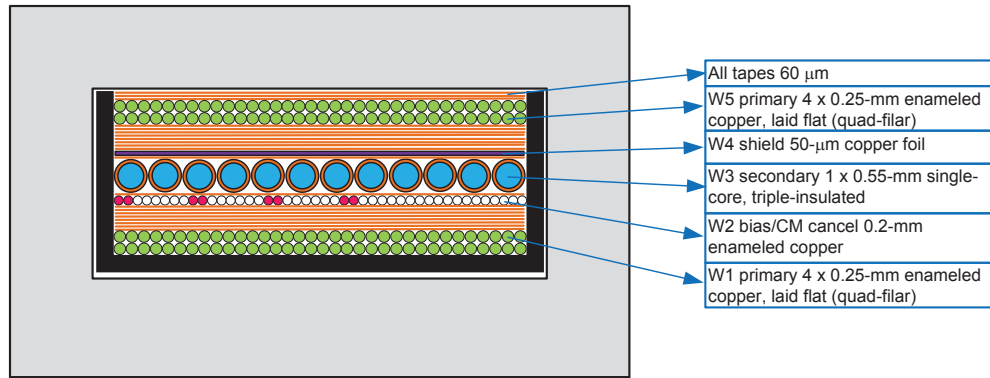
Figure 38. Conducted EMI plot for the UCC28630EVM572 with transformer No. 2. Conditions: input voltage 115 VRMS, output power 65 W, output return connected to earth; QP result in blue, AVG result in green.

### Transformer No. 3

The leakage inductance of transformer No. 2 was 30 percent lower than transformer No. 1, and the overall losses reduced by 12 percent, or 1.1 W. How much of this improvement was due to the leakage inductance reduction (less energy lost in the external clamp), and how much was due to the expected improvement in winding ACR?

To answer this question, we implemented transformer No. 3; see **Figure 39**. This is an almost identical construction to transformer No. 2, except that we added several more layers of tape to the construction on top of the first half primary and below the second half primary. This increase in separation increases the leakage inductance. We





**Figure 39.** Transformer No. 3 winding construction.

used the process described earlier for estimating leakage inductance and Equation 8 to estimate the required number of extra layers of tape to increase the leakage inductance to the same level as transformer No. 1. Based on our calculations, an extra 12 layers of tape would increase the leakage inductance by approximately 40 percent. In practice, we actually needed an extra 14 layers of tape to get the desired 40 percent increase in leakage inductance, which is very close to the estimate using Equation 8.

#### Analysis of transformer No. 3 performance

We checked transformer No. 3 for leakage inductance and efficiency performance in the EVM572 board.

We measured the leakage inductance at 4.46  $\mu\text{H}$  across the full primary terminals, with the main secondary shorted (all other windings open). This is approximately the same result as transformer No. 1, as targeted.

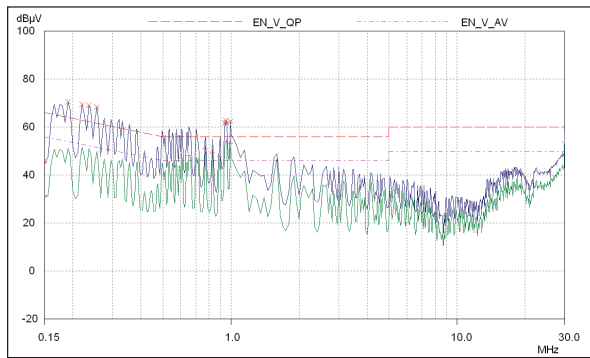
The full load efficiency at 65-W load, 115-VAC/60-Hz input was 88.39 percent, or 8.54 W of total power loss (not including the output cable drop).

This demonstrates that transformer No. 2's improvements were roughly 50 percent due to the leakage inductance reduction and 50 percent due to the improved ACR factor, thus emphasizing the importance of minimizing both leakage inductance and ACR for a flyback transformer.

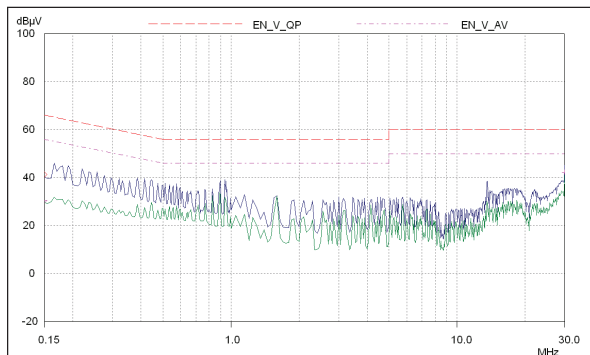
In order to highlight the benefit of the CM-balanced winding structure, we added a jumper to allow connection or disconnection of the shield and CM cancellation winding. As **Figures 40-41** show, there is a considerable difference. With the shield/CM-balanced winding connected, the conducted EMI drops as much as 26 dB on QP emissions and 20 dB on AVG.

For the conducted EMI plot of **Figure 41**, the pass margin is at least 17 dB below the Class B QP limit line (at 900-950 kHz) and at least 10 dB below the AVG limit line. This indicates that you can decrease the EMI filter size to achieve the more typical 6-8 dB pass margin, and yield significant savings in size, cost or losses.





**Figure 40.** Conducted EMI plot for UCC28630EVM572 with transformer No. 3 – shield/CM cancellation winding disconnected. Conditions: input voltage 230 VAC, output power 65 W, output return connected to earth; QP result in blue, AVG result in green.



**Figure 41.** Conducted EMI plot for UCC28630EVM572 with transformer No. 3 – shield/CM cancellation winding connected. Conditions: input voltage 230 VAC, output power 65 W, output return connected to earth; QP result in blue, AVG result in green.

For the conducted EMI plot of **Figure 41**, the pass margin is at least 17 dB below the Class B QP limit line (at 900-950 kHz) and at least 10 dB below the AVG limit line. This indicates that you can decrease

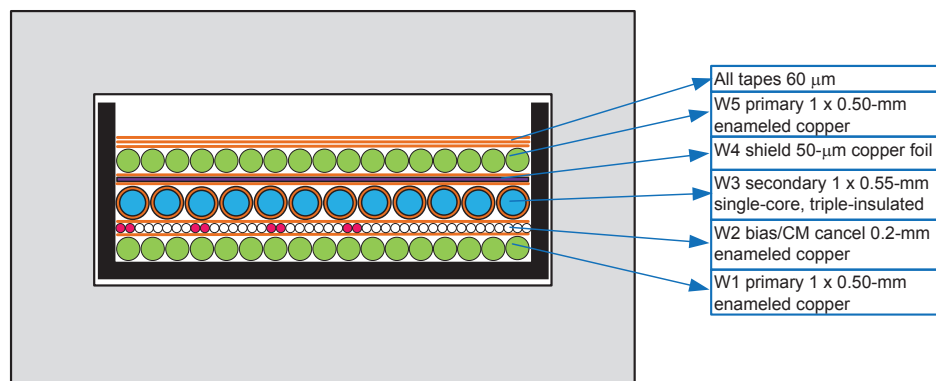
the EMI filter size to achieve the more typical 6-8 dB pass margin, and yield significant savings in size, cost or losses.

### Transformer No. 4

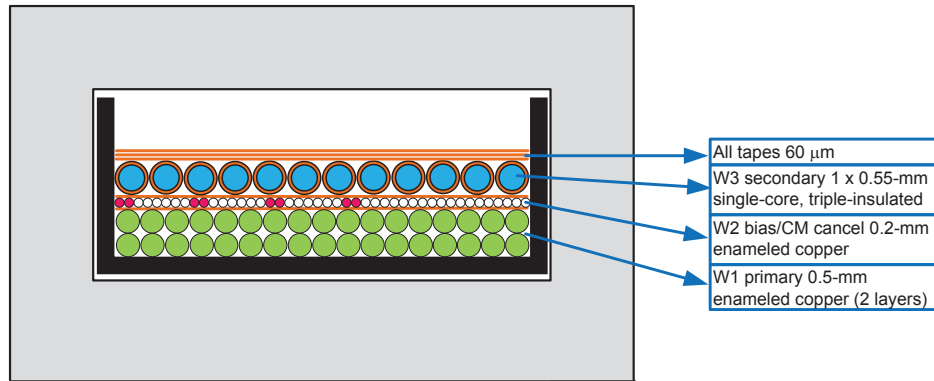
Revisiting our initial assumptions, what if each primary was wound over one layer instead of two? We calculated that the optimum wire diameter for one layer is approximately 0.55 mm. However, 17T does not quite fit in one layer in the available window width. To accommodate the full 17T in one layer, we decreased the wire diameter slightly to 0.5 mm, which almost fully fills one layer (0.53-mm wire would be ideal but was not readily available during prototyping).

Thus, we implemented transformer No. 4 with each half primary in a single layer, using a single 0.5-mm strand. All other layers were identical to transformer No. 2 (including the minimum number of tape layers). **Figure 42** illustrates the final winding cross-section and construction of transformer No. 4.

Compared to transformer No. 2, the primary winding cross-sectional area is unchanged ( $4 \times (0.25 \text{ mm})^2$  vs.  $1 \times (0.5 \text{ mm})^2$ ), so the DCR should be the same. The one-layer half-primary winding height of 0.5 mm is also the same as the two-layer 0.25-mm version, so given Equation 8, we would expect the leakage inductance to also be very similar.



**Figure 42.** Transformer No. 4 winding construction.



**Figure 43.** Transformer No. 5A winding construction.

### Analysis of transformer No. 4 performance

We checked transformer No. 4 for leakage inductance and efficiency performance in the EVM572 board.

We measured the leakage inductance at 3.29  $\mu\text{H}$  across the full primary terminals, with the main secondary short circuit (all other windings open). This is very close, as expected, to the 3.24- $\mu\text{H}$  value for transformer No. 2.

The full load efficiency at 65-W load, 115-VAC/60-Hz input was 88.58 percent, or 8.37 W of total power loss (not including the output cable drop).

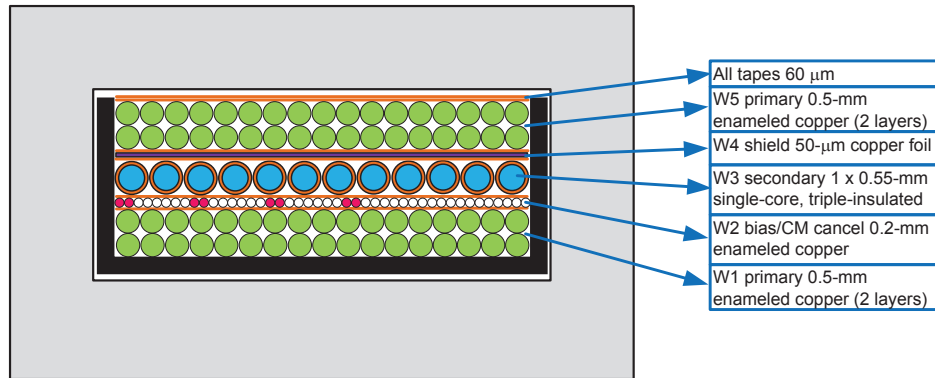
This demonstrates that although you can save ~0.5 W through the reduction in leakage inductance of both transformer No. 2 and transformer No. 4 compared to transformer No. 1, the net power loss savings of transformer No. 4 is only 0.74 W. The change in primary winding structure (to use a single, larger-diameter wire) actually increased losses by 0.34 W compared to transformer No. 2. Despite the same DCR, the ACR factor of transformer No. 4 is considerably worse than transformer No. 2.

### Transformer Nos. 5A and 5B

We wound transformer No. 5 in two versions, with and without interleaving, to demonstrate

its effectiveness. Transformer No. 5A had no interleaving, and was similar in construction to transformer No. 4. As **Figure 43** shows, the 0.5-mm half primaries are now wound together in two layers, without being interleaved as they were in the case of transformer No. 4. The auxiliary bias layer is unchanged, providing shielding and CM balance, and the secondary layer is also similarly unchanged. Since this version has no interleaving, there is no need for a shield layer on the outside of the secondary layer.

In order to show the difference between interleaved and noninterleaved implementations, we constructed transformer No. 5B as shown in **Figure 44**. This is very similar to transformer No. 5A, except that we added a shield layer outside the secondary, and another identical two-layer 0.5-mm full primary outside the shield. The shield is driven from the bias winding just as in transformer No. 2. Connecting the inner and outer full primaries in parallel achieves interleaving, just as in previous examples where two half primaries are connected in series. In the parallel configuration, the current will split approximately 50/50 between the two sets of primaries, so each one will produce half the MMF compared to the noninterleaved case.



**Figure 44.** Transformer No. 5B winding construction.

Compared to transformer No. 4, the primary winding cross-sectional area of transformer No. 5A is unchanged, so the DCR should be the same. The one-layer primary winding height of 1 mm is also the same as the two-layer 0.5-mm for transformer No. 4, so given Equation 7 we would expect that the leakage inductance would approximately double, due to the noninterleaving.

Transformer No. 5B by comparison should have half the DCR as transformer No. 4, and slightly more than half the leakage inductance due to the increase in total winding layer heights,  $\Sigma h$ , partly offsetting the 50 percent reduction due to interleaving.

#### Analysis of transformer Nos. 5A and 5B performance

We checked transformer Nos. 5A and 5B for leakage inductance and efficiency performance in the EVM572 board.

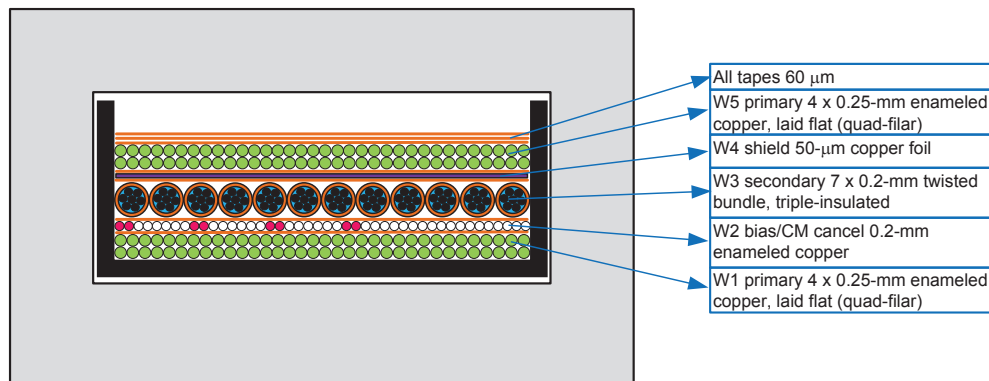
We measured the leakage inductance for transformer No. 5A at 6.41  $\mu\text{H}$ , approximately double the value of transformer No. 4, in keeping with expectations due to noninterleaving. With transformer No. 5B, the leakage inductance dropped to 3.7  $\mu\text{H}$  – again in keeping with expectations, almost half compared to transformer No. 5A due to the change to interleaving, but slightly higher than transformer No. 4 due to the increased total winding layer height.

The full load efficiency at 65-W load, 115-VAC/60-Hz input for transformer No. 5A was 86.94 percent, or 9.76 W of total power loss (not including the output cable drop). This is a huge drop in efficiency, even compared to transformer No. 1, predominantly due to the leakage inductance increase from the lack of interleaving. For transformer No. 5B, efficiency was 88.26 percent, or 8.65 W of total loss. Despite a leakage inductance similar to transformer No. 4, the total loss was almost 0.3 W worse. Using large-diameter two-layer primaries made the ACR factor worse, despite a 50 percent reduction in DCR.

#### Transformer No. 6

In the previous transformer iterations, we varied the primary between one- and two-layer constructions, with 0.5-mm and 0.25-mm wire stands. The 0.25-mm implementations resulted in better ACR factor and lower loss. But in all cases (except for transformer No. 1), the secondary implementation did not vary from the two-strand, triple-insulated, 0.55-mm one-layer implementation. Based on the findings for primary loss, maybe thinner secondary wire with more strands would also yield improvement.

To meet safety requirements, the secondary wires must be triple-insulated, or you would need a



**Figure 45.** Transformer No. 6 winding construction.

margin-wound construction. Given the significant reduction in winding-window widths for margin-wound constructions, triple-insulated wire is more common. Using a multistranded secondary winding would result in far too much window lost to the 0.2-mm triple-insulation thickness for each individual strand. Triple-insulated pre-stranded bundles (such as that used on transformer No. 1) are the most suitable option for a stranded secondary.

We implemented transformer No. 6 with the same primary, auxiliary and shield structure as transformer No. 2, combined with the stranded secondary winding of transformer No. 1. **Figure 45** shows the structure.

#### Analysis of transformer No. 6 performance

You would expect transformer No. 6's structure to have similar leakage inductance as transformer No. 2. However, we hoped that transformer No. 6 would exhibit improved secondary-winding conduction loss.

We checked transformer No. 6 for leakage inductance and efficiency performance in the EVM572 board.

We measured the leakage inductance at 3.24 µH, pretty much identical to transformer No. 2, as expected.

The full load efficiency at 65-W load, 115-VAC/60-Hz input was 89.0 percent, or 8.03 W of total power loss (not including the output cable drop). This was somewhat disappointing because compared to transformer No. 2, the results are almost identical. The multistrand triple-insulated secondary did not deliver the hoped-for conduction-loss improvement.

The total cross-section, and therefore the DCR, of transformer No. 6's secondary is 8 percent worse than transformer No. 2's secondary. Since the overall efficiency result is similar, this tells us that despite the DCR dis-improvement, there is a similar magnitude of ACR improvement – but the two effects cancel out. If we had implemented the multistrand secondary with the same total cross-section (for the same DCR), then we should have seen an improvement. However, in this case, there is not sufficient space to accommodate a triple-insulated secondary with more strands.

## Summary of transformer optimizations

**Table 2** summarizes the various results discussed in this paper. **Figures 47-48** graph the variation in efficiency of each transformer across line voltage and load.

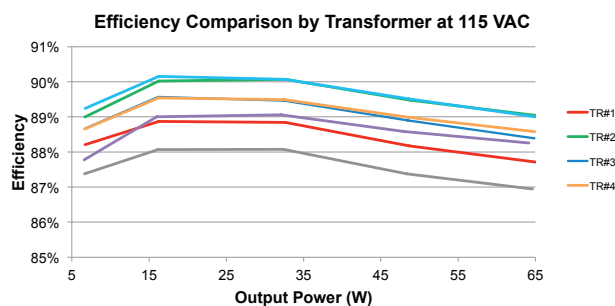
Transformer version	Leakage inductance ( $\mu\text{H}$ )	Full load efficiency at 115 VAC (percent)	$P_{\text{diss}}$ full load at 115 VAC (W)
1	4.51	87.71	9.11
2	3.24	89.03	8.01
3	4.46	88.39	8.54
4	3.29	88.58	8.37
5A	6.41	86.94	9.76
5B	3.70	88.26	8.65
6	3.24	89.00	8.03

**Table 2.** Performance comparison of various transformer constructions.

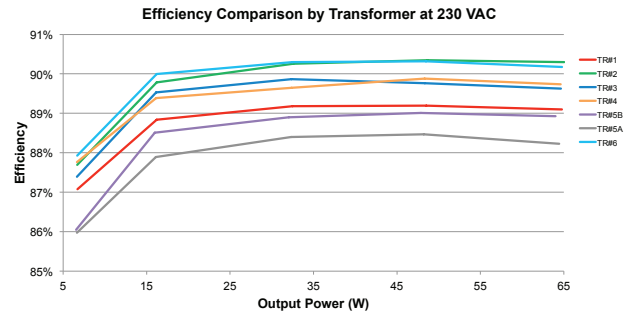
## Conclusions

This paper highlighted many important design considerations to achieve high-efficiency flyback transformers for offline AC/DC applications.

In particular, we highlighted the importance of the effects of duty cycle and DC bias on core losses. There has been (and still is) much ongoing research in this area. However, the available data from ferrite core manufacturers continues to be inadequate, and must improve so that designers can make more accurate and realistic estimates of core losses and see the genuine impact of operation at very small duty cycles.



**Figure 46.** Efficiency performance comparison of each transformer at low line (115 VAC).



**Figure 47.** Efficiency performance comparison of each transformer at high line (230 VAC).

For the transformer windings, we showed the importance of minimizing leakage inductance and ACR, and gave recommendations and approaches to improve performance. It is particularly important to choose bobbin and core styles with large breadth-to-height ratios appropriate for the required turns counts in order to minimize total layer count. Avoid partial layers and ensure that all layers are full and neatly wound.

The work of Hurley [12] and Carsten [9] serve as guides for choosing the best wire size and strand count, but multiple iterations will still be required in most cases to find a suitable compromise between cost/complexity and neat, full layers.

Finally, we showed that you can build very effective CM EMI reduction into transformer construction at the design stage, reducing system-level EMI filtering requirements and time-consuming EMI debugging later.

## Acknowledgements

Thanks to our colleagues at Texas Instruments in Cork, Ireland, for their invaluable contributions to this paper: Joe Leisten, Peter Meaney, Billy Long, John Griffin, Colin Gillmor and Seamus O'Driscoll.

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# TI Worldwide Technical Support

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