User's Guide Scalable PMIC's GUI User's Guide

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ABSTRACT

This document covers the usage and capabilities of the Scalable PMIC's graphical user interface (GUI) tool from Texas Instruments. This GUI is intended to be used with the analog EVM Control (AEVM) in order to evaluate and configure the TPS6594-Q1 and LP8764-Q1 family of devices.

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1 Introduction

This tool is based upon GUI Composer and requires the MSP432E401Y SimpleLink[™] Ethernet Microcontroller as the analog EVM controller (AEVM), which is integrated in the PMIC EVM and also available with the Launchpad[™], see 1 in the Section 11. The AEVM provides a USB interface to the host personal computer (PC) for receiving commands and then communicates with the PMIC using either an I²C or SPI protocol.

The GUI supports multiple devices with a single executable (and single AEVM), which eliminates the need to install multiple GUIs when working with more than one device. Multiple devices are configured in a master slave configuration and the AEVM communicates to each device over the selected shared medium: I²C or SPI.

2 Supported Features

The GUI supports the following features:

- Interface Multiple PMIC devices with a single GUI
- Quick-start and Register views to read and write to PMIC registers after power up
- Status Indicators for Interrupts and GPIO states
- Programming and Validation of non-volatile memory (NVM)
- Watchdog configuration and evaluation
- Multiple platforms ¹: Microsoft Windows,[®] Linux[®] 32 and 64-bit, and Mac OSX
- Web based and standalone versions available
- · Links to additional collateral, support forums, and FAQ

3 Revisions

This section details the features added with each release of the Scalable PMIC's GUI.

Release 1.0.0 is the initial pre-production release and named the Programmable Processor PMIC's GUI. This version of the tool allows for evaluation and programming but does not provide a mechanism to create NVM configurations.

Release 2.0.0 is the latest release and named the Scalable PMIC's GUI. This document reflects this latest version.

Revision	Release Date	Devices Supported	Feature Updates and Additions
1.0.0	December 2019	TPS6594-Q1 Revision 1.0 Silicon	Initial Pre-Production Release Quick-start Page Register Map Page NVM Programming
2.0.0	November 2020	 TPS6594-Q1 LP8764-Q1 TPS6593-Q1 TPS6594-Q1 Revision 1.0 Silicon 	 NVM Creation and validation NVM Templates Scripting LP8764-Q1 Device Support Improved programming speed Watchdog Evaluation Page SPI and CRC enabled serial communication

Table 3-1. GUI Revisions

¹ Please refer to dev.ti.com for version compatibility with GUI Composer.



4 Overview

Calable PMICs GUI is GUI supports evaluation, configuration, and programming of the TPS65934x, TPS6593x, and LP876x devices.			
		GET STARTED	
ase choose your device	Search Device Q.	Begin evaluating a Device Quick-start	
TPS6594x-1.0		Begin an NVM Configuration	
e TPS6594-Q1 1.0 is an integrated power-management device for automotive and industrial applications.	TP\$53246-1.6	NVM Configuration	
EAD MORE 🔸	P has some	Validate NVM Settings NVM Validation	
) TPS6594x			
he TP96594-Q1 is an integrated power-management device for automotive and industrial applications.	TP:453944		
IEAD MORE 🎍	€ Passan		
) TP\$6593x	REGISTER MAP	RESOURCES	
he TPS6593-Q1 is an integrated power-management device for automotive and industrial applications.		1 * ⊕ ₽	
EAD MORE 🄶	19440354 Diministration	Table PARC Efficiency Find More SoC E2E Forum OU User Guide Estimation Tool Power Solutions E2E Forum	
D LP8764x	REGISTER MAP		
he LP8764-Q1 is an integrated power-management device for automotive and industrial applications.	LPETRA		
EAD MORE 🔶	Participants	VALIDATED PROCESSOR-ATTACH SOLUTIONS	
▶ LP8763x	REGISTER MAP	VALIJA LED PHOLESSON-A I JACH SOLUTIONS	
he LP8763-Q1 is an integrated power-management device for automotive and industrial applications.		View NVM	
	LP3753x 49 ton	🗧 🔲 User Guide	

Figure 4-1. GUI Overview

The GUI provides pages to both evaluate and configure the PMIC. For evaluation, the quick start, register map, and watchdog pages provide an interface to monitor and control the PMIC via a SPI or I²C interface. Configuration of the PMIC NVM is done through the NVM Configuration page and the NVM validation page is provided to read the NVM content of the PMIC. More information on the Quick-start, Register Map, NVM Configuration, NVM Validation, and Watchdog Evaluation pages will be provided in the subsequent sections.

The GUI also provides templates and references to the user guides and data sheets in order to assist in the development process. It is recommended, when applicable, to use an existing template as a starting point for development. These templates not only provide a graphical representation of the PMIC operation but also generate the required NVM files to program the PMIC.

	Note	
Starting from a template is recommended.		
·		

Device Selection

The Device Selection page is the first page presented when the GUI is started. From this page a specific device can be selected by selecting the Register Map within a given device window. The other pages can also be selected without regard of a particular device. From these pages it is necessary to use the Device Interface Settings window to select which device as well as the interface.

Register Map

The Register Map page is a list view of the available user registers with the ability to read and write to those registers.

Quick-start

4

The Quick-start page is recommended as the starting point for evaluating the device. The Quick-start page provides a graphical view for interacting with the PMIC and configuring the device registers. In addition to this abstracted view is the actual register view provided from the Register Map Page.



NVM Configuration

The NVM Configuration page provides a means to both configure and program the non-volatile memory (NVM) settings. The configuration includes both the static settings as well as the pre-configured state machine (PFSM) settings.

NVM Validation

The NVM Validation page reads out the NVM content and can be used to verify the contents of the NVM match what was programmed from the NVM Configuration page.

Watchdog Evaluation

The WatchDog Evaluation page is a unique page providing a graphical interface for both configuring and exercising the Watchdog feature on select PMICs.

5 Getting Started

Getting started involves the following steps:

- 1. Find the GUI within the Gallery.
- 2. Download the required software.
 - a. GUI Composer Runtime for running the GUI from a web browser
 - b. An offline copy of the GUI
- 3. Launch the GUI.

5.1 Finding the GUI

The PMIC GUI is based upon GUI Composer which is compatible with either Chrome[™] (version 46+) or Firefox[™] (version 38+). The Chrome[™] web browser is recommended and used throughout this document for demonstration. The GUI is found through the TI Development tools at TI DevTools page. Navigating to the Gallery from the Explore tab, highlighted in red in Figure 5-1, is one way to enter the Gallery.

Stil DevTools Explore Develop Help		Chris Logout
Star Resource Explorer Star Callery No devices detected. Please connect your LaunchPad to access recommended resources for your device.	<section-header></section-header>	
		-
C	Cloud tools (show me desktop tools instead)	

Figure 5-1. GUI Composer Gallery

When in the gallery, locate the Scalable PMIC's GUI panel shown in Figure 5-2. If the panel is not visible on the main page, then use the search bar and type the term PMIC.

Note The name of the GUI has changed so panels are available for both the Programmable-Processor-PMICs-GUI and the Scalable-PMICs-GUI. The Scalable-PMICs-GUI version 2.0.0 is the latest version.



	Search Q
We've found 3 result(s) for "PMIC "	Sort by Best Match 🗸
Point Interportantial III Continue Point IIII Continue Point III Continue Point III Continue Point III Continue Point III Continue	
PMIC-Efficiency-Esti Version 0.9.0 by PMIC (Group) by PMIC (Group)	Scalable-PMICs-GUI Version 2.0.0 by PMIC (Group)
Configurable efficiency estimator Programmable Processor PMICI's tool for various Texas GUI - v1.0.0 instruments PMICI's such as TP96594-01, LP8764-01 and many more.	Configuration and Evaluation tool for use with the AEVM and the TP56594, TP56593, and LP8764 family of PMICs.
	🔂 🛃 🛈 5 Views

Figure 5-2. Locating the PMIC GUI in the Gallery

5.2 Downloading the Required Software

Both the standalone GUI and the GUI Composer Runtime are available from the PMIC panel. Again, the GUI Composer Runtime enables the GUI to be run through a web browser. This is a small download but still requires an internet connection to be able to run the GUI. By contrast the standalone GUI is much larger but does not require an internet connection.

The download options are found in the pop-up window, as shown in Figure 5-3, when the cursor is placed on the download icon. The upper three options are for a standalone download for the appropriate operating system, while the lower three are for the GUI Composer Runtime.

Ve've found 1 result(s) for " P	MI
Dushboard	
Select the platform to download	
Linux 64bits	
 Mac 	
Windows	
this software requires GUI Composer runtime v7.3.0. You can download it during the installation of this software. Alternatively, you can get the runtime here.	
Linux 64bits runtime	
Mac runtime	
Windows runtime	

Figure 5-3. GUI Software Download Options



5.3 Launching the GUI

After the appropriate software has been downloaded, the GUI can be launched locally from the PC application or from the TI Cloud using the Gallery. To use the TI Cloud version of the GUI, simply click anywhere in the panel, shown in Figure 5-4, that is not associated with the download or information icons.



Figure 5-4. GUI Panel Within the Gallery

Figure 5-5 shows an example of the PC application.

All Apps Documents Web More 🕶	م
Best match for apps	
Scalable-PMICs-GUI 2.0.0	
Apps Programmable-Processor-PMICs-GUI 1.0.0	Scalable-PMICs-GUI 2.0.0
Store PMIC - Search for apps in the Microsoft Store	 Open Run as administrator Run as different user Open file location Pin to Start Pin to taskbar Uninstall



Launching the GUI automatically loads the Device Home page, shown in Figure 5-6.

7

GUI supports evaluation, configuration, and programming of the TPB6594x, TPB6593x, and LP876x devices.		GET STARTED	
se choose your device	Search Device Q	Begin evaluating a Device	
) TP\$6594x-1.0	REGISTER MAP	Begin an NVM Configuration	
he TPS6594-Q1 1.0 is an integrated power-management device for automotive and industrial applications.	TP \$5054-1.0	NVM Configuration	
EAD MORE 🔶	P Internet	Validate NVM Settings	
• TPS6594x			
The TPS6594-Q1 is an integrated power-management device for automotive and industrial applications.			
ead more 🖕	TP SEOSA: Distances		
) TPS6593x		RESOURCES	
he TPS6593-Q1 is an integrated power-management device for automotive and industrial applications.		和 ** + 中 - 中	
EAD MORE 🔶	TP365334 4 Millionaum	GUI User Guide PMIC Efficiency Find More SoC E2E Forum	
S LP8764x			
he LP8764-Q1 is an integrated power-management device for automotive and industrial applications.	LPUTRAL		
EAD MORE →	USPAT Parameter		
€ LP8763x		VALIDATED PROCESSOR-ATTACH SOLUTIONS	
he LP8763-01 is an integrated power-management device for automotive and industrial applications.		TPSSSB4-1.0 and LP87_ View NVM	
	LP3765z	📕 User Guide	

Figure 5-6. Device Home Page

Note

The GUI will not attempt to connect to the AEVM controller unless the register map or Quick-start page is entered. The GUI will attempt to automatically detect and connect to the correct Serial Port. Once this connection is made then the GUI will attempt to connect to the default I²C address of 0x48. If the address is not acknowledged, then the GUI will provide the Device Settings window to update the interface and address. Refer to the troubleshooting section for additional tips on resolving connection issues.

5.4 Connecting to a PMIC

The GUI and AEVM support both I²C and SPI with and without CRC. As mentioned previously, when entering the Register Map and Quick-start pages, the GUI will attempt to connect to any device with a non-CRC I²C interface at address 0x48. If an alternate address or configuration is needed, then the *Device Settings* window is provided to change the settings, as shown in Figure 5-7. This window can also be accessed in the drop-down menu below *Options*.



Register Map							Auto Re	ad Off	~	IEAD REGISTER	READ ALL REGISTERS	WHITE PEOPERS
C Search Registers by name or address (0x)										Search Bitfields	Show Bits	
Re	gister Name	Address	Value	7	6	5	8i 4	19 3	2		0	FIELD VIEW DEV_REV
v User Registers - Page 0												
DEV_REV		0x01	0x00	0	0	0	0	0	0	0	0	
NVM_CODE_1		0x02	0x00	0	0	0	0	0	0	0	0	0×(00
NVM_CODE_2		0x03	0x00	0	0	0	0	0	0	0	0	
BUCK1_CTRL		0x04	0x22	0	0		0	0	0		0	
BUCK1_CONF		Dentes Dell'est						0	0		0	
BUCK2_CTRL		Device Settings				>	·	0	0		0	
BUCK2_CONF		1 Configure Serial Port Settings						0	0		0	
BUCK3_CTRL								0	0		0	
BUCK3_CONF		Select Port : COM15 (Texas Instrumen	ts, Inc.) 👻	Select Baud Rate	9600 (Recom	mended) 👻		0	0		0	
BUCK4_CTRL		2 Choose Connected Device Type	Configu	re interface set	tings			0	0		0	
BUCK4_CONF		Choose connected beriev type	i oomiga	ie internace ac	ungo			0	0		0	
BUCK5_CTRL		Select Device	Select curren	Interface	12C MODE	SPI MODE		0	0		0	
BUCK5_CONF		TROUGHT		-			_	0	0		0	
BUCK1_VOUT_1		Portanary TPS6594x V	I2C1 Addre	ss: 0x48 👻				0	0	0	0	
BUCK1_VOUT_2		······································						0	0	0	0	
BUCK2_VOUT_1			I2C1 CRC E	nabled: 🔵				0	0	0	0	
BUCK2_VOUT_2		Device Status: Disconnected 😐						0	0	0	0	
BUCK3_VOUT_1			12C2 CRC E	nabled: 🔎				0	0	0	0	
BUCK3_VOUT_2								0	0	0	0	
BUCK4_VOUT_1					CONN	ECT TO HARDWARE		0	0	0	0	
BUCK4_VOUT_2			0.00		_			0	0	0	0	
BUCK5_VOUT_1		0x16	0x00	0	0	0	0	0	0	0	0	
BUCK5_VOUT_2		0x17	0x00	0	0	0	0	0	0	0	0	
BUCK1_PG_WINDOW		0x18	0x00	0	0	0	0	0	0	0	0	
BUCK2_PG_WINDOW		0x19	0x00	0	0	0	0	0	0	0	0	
BUCK3_PG_WINDOW		0x1A	0x00	0	0	0	0	0	0	0	0	
BUCK4_PG_WINDOW		0x1B	0x00	0	0	0	0	0	0	0	0	
BUCK5_PG_WINDOW		0x1C	0x00	0	0	0	0	0	0	0	0	
LD01_CTRL		0x1D	0x00	0	0	0	0	0	0	0	0	
LD02_CTRL		0x1E	0x00	0	0	0	0	0	0	0	0	
LD03_CTRL		0x1F	0x00	0	0	0	0	0	0	0	0	
nnected to AEVM Controller, but failed to connect to devi	e TPS5594x 2n0 internal on DUTWITHI2C @0x48		0x00	0	0	0	0	0	0	0	0	

Figure 5-7. Device Settings From Options Tab

Device Settings	×
1 Configure Serial Port Settings 🤁	
Select Port : COM15 (Texas Instruments	s, Inc.) 💌 Select Baud Rate : 9600 (Recommended) 👻
2 Choose Connected Device Type	3 Configure interface settings
Select Device	Select current interface I2C MODE SPI MODE
TPS6594x TPS6594x	I2C1 Address: 0x48 👻
Device Status: Disconnected	I2C1 CRC Enabled:
	I2C2 CRC Enabled:
	CONNECT TO HARDWARE

Figure 5-8. Device Interface Settings

As shown in Figure 5-8, options are provided to select the device as well as the interface.

Select Device

The device selection will determine the register interpretation of data written to and read from the PMIC. Failure to select the correct device can result in erroneous data being written to the PMIC or data read from the PMIC to be misinterpreted.



l²C

The I²C1 address selection is limited to valid page 0 addresses of the PMIC. Once the I²C1 address is specified, the GUI will automatically determine the addresses for pages 1-4 as well as determine if the physical I²C2 interface for page 4 is to be used.

SPI

Similar to the I²C implementation, the GUI will automatically update the page information during communication.

Updating the Interface

In addition to the *Option* tab at the top of the GUI, in the Quick-start, Register Map, and Watchdog pages, there is a device settings bar that shows the current interface selection. Clicking the gear icon within the bar also opens the Device Settings window. In the NVM Configuration and NVM Validation pages, the interface selection is provided within the page. Please refer to those sections for more details.

٠	Mode	Addr	I2C CRC	WD CRC
	I2C	0x48	×	×

Figure 5-9. Device Settings Bar

Note

Connecting to a device is not required to access the GUI pages. Specifically, connecting to a device is not required to create an NVM configuration as described in section Section 8



6 Quick-start Page

From the initial Quick-start page in Figure 6-1, the *Detect Devices* box is provided to automatically detect all PMIC devices connected to the microcontroller's I²C or SPI² bus. The GUI will attempt to connect through I²C to the default address associated with the device. The *Hardware Connected* located at the bottom left of the GUI indicates that a device was found at that address. If no device can be found at the default address, then the device address (or configuration in the context of SPI) must be provided for at least one device connected to the GUI to use the *DETECT DEVICES* button. The interface connection can be changed by selecting the *Device Settings* from the *Options* drop-down menu at the top of the page.

Scala	ble PMICs GUI File Options Help	
*	Quick-start	
4		
949		
۲		
1		
®	Configure and Monitor all your Devices Settings	
		Connect your Master device to the computer using USB Port to get started DETECT DEVICES
B G	COM8115200 Herdean Connoted	Aventa de Décembre Ali Texa Normanian

Figure 6-1. Quick-start Scan Page

² To support multiple devices on the same SPI bus, dedicated Chip Select pins are required for each PMIC. The current version of the GUI does not provide multiple dedicated Chip Select pins from the AEVM, and consequently can only communicate with one PMIC with SPI.



6.1 Device Scan Results

Figure 6-2 shows, for this example, two PMICs are detected. One PMIC is configured as the master, denoted with the *M* in the blue circle, and the other as the slave. Additional information regarding the BUCK phase configuration and the $l^2C ID$ of each device is indicated. The device label is an editable field and can be updated to provide a custom naming convention. By clicking the *Proceed* button, the quick-start page will advance to the interface window where select device registers can be written or read.

Scala	ble PMICs GUI File Options Help		
*	Quick-start		
	Configure and Monitor all your Devices Settings	DETECTED DEVICES	RE-SCAN FOR DEVICES
		PROCEED Presse Re-Coan to get the latest device settings after programming	Avende de Despace**

Figure 6-2. Quick-start Scan Page Results



6.2 Configuration and Monitoring

Within the Quick-start page there are six tabs aligned horizontally for editing and four tabs aligned vertical for monitoring and accessing advanced features. These are highlighted in Figure 6-3. These tabs in the Quick-start page are described in the following sections. It is important to note that the GUI is continuously polling the PMIC to update the Interrupts, Resource Status, and GPIO Pin status. Additionally, each update or change in value results in communication to the PMIC to update the appropriate register. The device can be reset with a power cycle to restore the register settings to the NVM values.

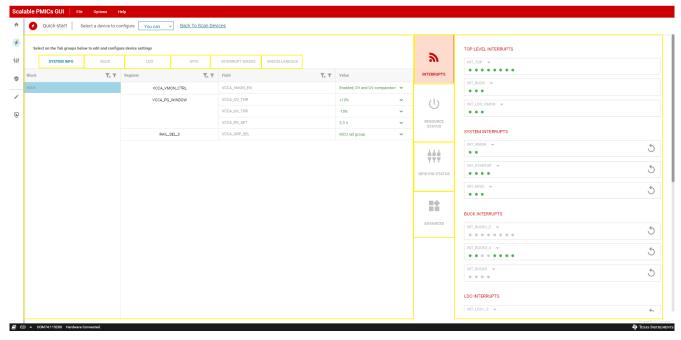


Figure 6-3. Quick-start Page Highlights

Note

At the top of the Quick-start page is a drop-down menu to select the device when multiple PMICs are connected. This label is defined in Figure 6-2.

Note

All register fields are direct references to the device specification. When values within a field are repeated or reserved, the GUI will not show these possible values in the drop-down menu options.



6.2.1 System Info

As shown in Figure 6-4, the system info tab is related to the VCCA input voltage and, when applicable, additional voltage monitors. Drop-down menus are provided to show the possible values for each field.

-	Quick-start Select a	device to configure	TPS65940 -	Back To Scan D	241065					
Selec	ct on the Tab groups below to edit	and configure device s	ettings						TOP LEVEL INTERRUPTS	
	SYSTEM INFO	BUCK	LDO	GPIO	INTERRUPT MASKS	MISCELLANEOUS		۳	INT_TOP 👻	
Block	T x T	Register	T x T	Field	T _x T	Value		INTERRUPTS		
VCCA		VCCA_VM	ON_CTRL	VCCA_VMON_EN		Enabled; OV and UV co	m 🗸			
		VCCA_PG_	WINDOW	VCCA_OV_THR		+10%	~	\bigcirc	INT_LDO_VMON 👻	
				VCCA_UV_THR		-10%	~	RESOURCE STATUS	•••	
				VCCA_PG_SET		3.3 V	~		SYSTEM INTERRUPTS	
		RAIL_S	SEL_3	VCCA_GRP_SEL		MCU rail group	~	$\frac{1}{7}\frac{1}{7}\frac{1}{7}$	INT_VMON -	5
								GPIO PIN STATUS	INT_STARTUP V	5
										5
								ADVANCED	BUCK INTERRUPTS	
									INT_BUCK1_2 💌	5
									INT_BUCK3_4	5
										5

Figure 6-4. System Information

Note

The phase configuration cannot be changed with either the Quick-start or the Register map pages. To change the phase configuration the device NVM must be reconfigured, please seeSection 8.

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6.2.2 BUCK

The phase configuration will determine which BUCKs are available for editing through the quick-start. In Figure 6-5, the BUCK2 information is not available because BUCK2 is multiphased with BUCK1. The BUCK1 is treated as the master and BUCK2 as the slave, with all of the properties of BUCK1 being applied to BUCK2. Please refer to device data sheet for a more detailed description of the fields and the associated operation.

Select on the Tab groups be	low to edit	and configure device setti	ngs					RESOURCE STATUS	
SYSTEM INFO		BUCK	LDO	GPIO	INTERRUPT MASKS	MISCELLANEOUS	INTERRUP	BUCK1_2	Disabled
ock	$\overline{\P}_{\! \times} \overline{\P}$	Register	$\overline{T}_{\!\rm X}\overline{T}$	Field	T _x T	Value	INTERROP	BUCK3	Disabled
ck1_2		BUCK1_CT	RL	BUCK1_EN		Disabled; BUCK1 regulate	<u>ں</u>		
ick3				BUCK1_FPWM		PWM operation only.	v U	BUCK4	Enabled
ick4				BUCK1_FPWM_MP		Automatic phase adding	RESOURCE STATUS	BUCK5	Disabled
ick5				BUCK1_VMON_EN		Disabled; OV and UV com	~		
				BUCK1_VSEL		BUCK1_VOUT_1	✓ 111 TTT	LD01	Enabled
				BUCK1_PLDN		Enabled; Pull-down resist			Disabled
				BUCK1_RV_SEL		Enabled	✓ STATUS		UISADIed
		BUCK1_CO	NF	BUCK1_SLEW_RATE		2.5 mV/µs	~	LD03	Disabled
				BUCK1_ILIM		5.5 A	~		
		BUCK1_VOU	T_1	BUCK1_VSET1		0.800 V	ADVANCE	LDO4	Disabled
		BUCK1_VOU	Т_2	BUCK1_VSET2		0.3 V	 	-W	
		BUCK1_PG_WI	NDOW	BUCK1_OV_THR		+4% / +40 mV	~		
				BUCK1_UV_THR		-4% / -40 mV	~		
		RAIL_SEL	.1	BUCK1_GRP_SEL		SOC rail group	~		
		(j) Buck1_2,Buck3,Bu	ck4,Buck5 are ac	tive as Masters as per cu	rrent phase configuration				

Figure 6-5. BUCK Configuration

Note

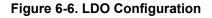
The frequency selection register FREQ_SEL is protected and cannot be changed from the quick-start page. To change this field, similar to the phase configuration, the NVM must be updated accordingly.



6.2.3 LDO

From the LDO tab, configuration of the LDOs is available. Please refer to the device data sheet for a more detailed description of the fields and the associated operation. If a PMIC does not have LDOs, then the LDO tab will be omitted.

	Quick-start Select a	device to co	nfigure TPS65940 -	Back To Scan De	vices					
	Select on the Tab groups below to edi	t and configure	e device settings					۳	TOP LEVEL INTERRUPTS	
l	SYSTEM INFO	BUCK	LDO	GPIO	INTERRUPT MASKS	MISCELLANEOUS			INT_TOP -	
I	Block T _x T	Register	T _x T	Field	T _x T	Value		INTERRUPTS	INT_BUCK 💌	
I	LD01		LD01_CTRL	LDO1_EN		Enabled; LDO1 regulator.	~	215	• • •	
I	LD02			LDO1_PLDN		125 Ohm	~	Ú	INT_LDO_VMON 👻	
l	LD03			LD01_VM0N_EN		Disable OV and UV comp	~	RESOURCE	•••	
l	LD04			LD01_RV_SEL		Enabled	~		SYSTEM INTERRUPTS	
l			LD01_VOUT	LD01_VSET		1.80 V	~	***	INT_VMON 👻	5
l				LD01_BYPASS		Linear regulator mode.	~		• •	C
l		L	D01_PG_WINDOW	LD01_0V_THR		+4% / +40 mV	~	GPIO PIN STATUS	INT_STARTUP 👻	\$
l				LD01_UV_THR		-4% / -40 mV	~		••••	
l			RAIL_SEL_2	LD01_GRP_SEL		MCU rail group	~			5
l		LDO	_RV_TIMEOUT_REG_1	LDO1_RV_TIMEOUT		16ms	~	ADVANCED		
I								ADVANOLD	BUCK INTERRUPTS	
l									INT_BUCK1_2	5
l										
									INT_BUCK3_4	Ć
									INT_BUCK5 💌	4
l										5



6.2.4 GPIO

The GUI provides the interface to configure the PMIC GPIOs. When the GPIO is configured as an input, the GUI provides an additional mechanism to drive the GPIO from an associated AEVM pin and view the state change through the GPIO Status vertical tab on the right side of the page.

The PMIC GPIO can be configured as input or output or be mapped to internal functions within the PMIC. For this example, the PMIC is using GPIO1 and GPIO2 for the second I²C instance. The GPIO PIN STATUS window pane can be used to confirm the function and the level of each pin when configured as GPIO. The CONFIGURE GPIO LEVEL box appears, see Figure 6-7, when the GPIO direction is set to input to initially set the AEVM output level. Please ensure that the hardware platform is configured to support the intended GPIO operation.

Note

When evaluating a multi-PMIC solution, the control of the AEVM outputs are only for the AEVM which is connected to the GUI (connected to the PC through the USB port).

The GPIO pin status, see Figure 6-7, indicates the function of the GPIO as well as the current state (high or low) of GPIO that are not configured for special functionality. The colors are gray, red, and green. In addition to the color, a text description to the right of each indicator is also provided.



Quick-start Page

Quick-start		device to configure	● TPS65940 ▼	Back To Scan Dev					
Select on the Tab groups i	below to edit	and configure device	e settings		GPIO PIN STATUS				
SYSTEM INFO		BUCK	LDO	GPIO	INTERRUPT MASKS	MISCELLANEOUS	2	GPI01	SCL_12C2/CS_SPI
ock	T x T	Register	T x T	Field	T x T	Value	INTERRUPTS	GPI02	SDA_12C2/SD0_SPI
210 1		GPIC	1_CONF	GPI01_0D		Open-drain output 🗸 🗸		01102	0000202000201
2010				GPI01_DIR		Input 🗸	U	GPI03	GPI03
210 3				GPI01_SEL		SCL_I2C2/CS_SPI 🗸	RESOURCE	GPI04	GP104
PIO 4				GPI01_PU_SEL		Pull-down resistor selecte 🗸 🗸		66104	C GPI04
PIO 5				GPI01_PU_PD_EN		Disabled; Pull-up/pull-dov 🗸	+++	GPI05	SCLK_SPMI
10 0				GPI01_DEGLITCH_EN		No deglitch, only synchro 🛛 🗸	GPIO PIN	GPI06	SDATA_SPMI
20.8		GPIC	0_0UT_1	GPI01_OUT		Low	STATUS	GPI06	SDATA_SPMI
9 019								GPI07	GPI07
90 10 90 11								GPI08	G P108
WRON and nRSTOUT							ADVANCED	GPI09	GP109
								GPI010	GPI010
								GPI011	O GPI011





6.2.5 Interrupts

From the interrupts tab the user can decide to mask or monitor various interrupt sources: State Machine, GPIOs, BUCKs, and so on.

The interrupt status, shown on the right side of Figure 6-8, can be used to monitor the interrupt events. The interrupts are grouped according to function and can be expanded to see each individual interrupt source. *TOP LEVEL INTERRUPTS* are read only and cannot be cleared. Other interrupts can be cleared at a register or bit level, as indicated by the reset symbol. An *ERROR* status with a red dot indicates that an interrupt has occurred while a *NORMAL* status with a green dot indicates that no interrupt has occurred or that the interrupt has been cleared. Typically, gray represents interrupts which are masked. If an interrupt has a *NORMAL* status with a gray dot, then this indicates that the interrupt is not applicable for the specified phase configuration. The GUI will ignore any attempt to unmask or generate an interrupt that is not applicable to the device phase configuration.

🤣 Quick-start	Select a	levice to configur	e TPS65940 🔻	Back To Scan D	evices					
Select on the Tab groups	below to edit	and configure devic	e settings						TOP LEVEL INTERRUPTS	
SYSTEM INFO		BUCK	LDO	GPIO	INTERRUPT MASKS	MISCELLANEOUS		۳	INT_TOP 👻	
Block	T _x T	Register	T _x T	Field	T _x T	Value		INTERRUPTS	INT_BUCK 👻	
State Machine Actions		FSM_1	TRIG_SEL_1	MCU_RAIL_TRIG		MCU power error	~	215	• • •	
GPIO				SOC_RAIL_TRIG		SOC power error	~	(INT_LD0_VMON 👻	
BUCK				OTHER_RAIL_TRIG		SOC power error	~	RESOURCE STATUS	•••	
LDO				SEVERE_ERR_TRIG		Immediate shutdown	~		SYSTEM INTERRUPTS	
System		FSM_1	TRIG_SEL_2	MODERATE_ERR_TR	IG	Orderly shutdown	~	$\frac{1}{T} \stackrel{1}{} \frac{1}{T} \stackrel{1}{}$	INT_VMON 💌	ć
Error								GPIO PIN	• •	C
								STATUS	INT_STARTUP -	٢
										ť
								ADVANCED		
									BUCK INTERRUPTS	
									INT_BUCK1_2 -	*
									INT_BUCK3_4 👻	
										Ċ
									INT_BUCK5 👻	ć
										C

Figure 6-8. Interrupt Mask and Status

6.2.6 Miscellaneous Settings

The MISCELLANEOUS tab includes settings for the power good (PGOOD), spread spectrum configuration, and additional configurations of the PMIC.

r	🖌 Quick-start Sele	ect a d	evice to configure	TPS65940 👻	Back To Scan De	vices					
	Select on the Tab groups below t	o edit a	nd configure device s	ettings					2	Read/Write Registers	
ł	SYSTEM INFO		BUCK	LDO	GPI0	INTERRUPT MASKS	MISCELLANEOUS		INTERRUPTS		
,	Block T	T	Register	T _x T	Field	T x T	Value		INTERROPTS	Register Address Enter page address followed by the	0x
	POWERGOOD		PG00D	_SEL_1	PGOOD_SEL_BUCK1		Voltage AND Current	~	215	register address	
12	Spread Spectrum				PGOOD_SEL_BUCK2		Voltage AND Current	~	Ú	Register Value	0x
9	Additional Configurations				PGOOD_SEL_BUCK3		Voltage AND Current	~	RESOURCE STATUS	Actual Register Value in Hex	
					PGOOD_SEL_BUCK4		Voltage AND Current	~			
			PG00D.	_SEL_2	PGOOD_SEL_BUCK5		Voltage AND Current	~	+++		
			PG00D	_SEL_3	PG00D_SEL_LD01		Voltage AND Current	~	GPIO PIN		
					PGOOD_SEL_LDO2		Voltage AND Current	~	STATUS		
					PGOOD_SEL_LDO3		Voltage AND Current	~			
					PGOOD_SEL_LDO4		Voltage AND Current	~			
			PG00D	_SEL_4	PGOOD_SEL_VCCA		Masked	~	ADVANCED		
					PGOOD_SEL_TDIE_W/	ARN	Masked	*			
					PGOOD_SEL_NRSTOU	Т	Masked	~			
					PGOOD_SEL_NRSTOL	IT_SOC	Masked	~			
					PGOOD_POL		PGOOD signal is high w	hi 👻			
					PGOOD_WINDOW		Both undervoltage and	ov 🗸			

Figure 6-9. Miscellaneous Settings

6.2.7 Advanced

The Advanced tab provides direct write and read access to and from the registers. The access format is 0xabc, where *a* is the page number and *bc* is the register address. Refer to the device data sheet for the page number and register address for a given device register.



7 Register Map Page

The Register Map page lists the different registers available for configuration. Unlike the Quick-start page, there is no device label to select if multiple PMICs are present. In the case of I²C, the device address should be selected in the *Device Settings* below the *Options* tab at the top of the GUI. In the case of SPI, the HW connection to the chip select pin will determine which PMIC the GUI communicates with and whose contents are displayed in the Register Map page.

The Register Map page is intended for direct read and writes to the PMIC registers. The read can be done individually or all at once. Similarly, writing to registers can also be all at once or individually. In the *Immediate Write* mode (option located at the top right of the page), only individual registers are written to immediately with each change in the Field View, change in bits, or change in hexadecimal value. In *Deferred Write* mode, the writing of a single register or all registers is deferred until the **WRITE REGISTER** or **WRITE ALL REGISTERS** button is selected.

L	٥	Mode I2C	Addr 0x48	I2C CRC ×	WD CRC ×											
	Re	gister	Мар			Auto Read	Off		~	READ) REGIS	TER	READ	ALL RE	EGISTERS	WRITE REGISTER WRITE ALL REGISTERS Immediate Write
4	Q Search	Registers b	y name or	address (0	x)					Sea	arch Bi	itfields		Sho	w Bits	
		Registe	r Name			Address	Value				В				*	Field View DEV_REV
ŀ								7	6	5	4	3	2	1	0	DEV_REV
ŀ	Ver Reg	gisters - Pa	ge O		0	0x01	0x08	0	0	0	0	1	0	0	0	User Registers - Page 0 / DEV_REV / SILICON_VERSION[2:
	NVM_C					0x01	0xF0	1	1	1	1	0	0	0	0	SILICON_VERSION 600
	NVM_C					0x02	0x07	0	0	0	0	0	1	1	1	
	BUCK1_	_				0x04	0xA2	1	0	1	0	0	0	1	0	User Registers - Page 0 / DEV_REV / DEVICE_ID[5:3]
	BUCK1	CONF				0x05	0x2C	0	0	1	0	1	1	0	0	DEVICE_ID 60
	BUCK2	CTRL				0x06	0xA2	1	0	1	0	0	0	1	0	
	BUCK2_	CONF				0x07	0x2F	0	0	1	0	1	1	1	1	
	BUCK3_	CTRL				0x08	0xA2	1	0	1	0	0	0	1	0	
	BUCK3_	CONF				0x09	0x2C	0	0	1	0	1	1	0	0	
	BUCK4_	CTRL				0x0A	0xA3	1	0	1	0	0	0	1	1	
	BUCK4_	CONF				0x0B	0x2C	0	0	1	0	1	1	0	0	
	BUCK5_	CTRL				0x0C	0xA2	1	0	1	0	0	0	1	0	
	BUCK5_	CONF				0x0D	0x1B	0	0	0	1	1	0	1	1	
	BUCK1_	VOUT_1				0x0E	0x37	0	0	1	1	0	1	1	1	
	BUCK1_	VOUT_2				0x0F	0x00	0	0	0	0	0	0	0	0	
	BUCK2_	VOUT_1				0x10	0x37	0	0	1	1	0	1	1	1	
	BUCK2_	VOUT_2				0x11	0x00	0	0	0	0	0	0	0	0	
	BUCK3_					0x12	0x41	0	1	0	0	0	0	0	1	
		VOUT_2				0x13	0x00	0	0	0	0	0	0	0	0	
	BUCK4_					0x14	0x73	0	1	1	1	0	0	1	1	
		VOUT_2				0x15	0x00	0	0	0	0	0	0	0	0	
1	BUCK5_					0x16	0xB2	1	0	1	1	0	0	1	0	
1	BUCK5_	VOUT_2				0x17	0x00	0	0	0	0	0	0	0	0 🚽	Powered By GUI Con

Figure 7-1. Register Map

Note

Although visible from the Register Map Page, not all registers can be edited from this page. Specifically, the interface configuration cannot be changed, and similar with the Quick-start page the Buck frequencies cannot be changed. No error is reported, however, with each write is an associated read. The read will update the display so that writes to protected fields will accurately reflect that the write was unsuccessful.



8 NVM Configuration Page

The NVM configuration page is the main feature of the GUI and highlights the configurability of the PMIC. The configuration is comprised of the static and dynamic (PFSM) settings which are customizable for a broad range of applications. The NVM configuration page also provides the interface to download the configuration into the NVM of a target device. The download can be done after completion of creating a custom configuration, or this can be done with an existing NVM configuration.

8.1 Creating a Custom Configuration

Starting a validated template is recommended.

The NVM Configuration page does not require hardware in order to develop an NVM configuration. Connection with an actual device is needed only when attempting to upload to a target device.

There are three mechanisms available to start development. The first is to use the *Open Configuration* feature below the File tab at the top of the screen. This would be a configuration previously saved with the *Save Configuration* feature below the same File tab. Second, standard configurations are also provided as templates and can be selected below the *Select a template to start with*. Figure 8-1 shows the initial Select view with the upload and template mechanisms selected.

Note

Scala	able PMICs GUI	File	Options Hel		
+	🛞 NVM Configura	۲	Open Configuration	SELECT ——— STATIC CONFIGURATION ———	- PFSM PROGRAM
4	Select a template to		Save Configurations	VICES	
ŶĻŶ	start with _ Generic_LP8764				
۲	TI Jacinto 7: DRA821				
/	devices you would like to configure for NVM				
۲	TP \$65594x-1.0				
	TPS6594x-1.0				
	TP \$6534x				
	TPS6594v				
				Duplicate (or) No device alias found! 🕴 Skip to Programming	
<i>∎</i> ∈	COM74:115200 Hard	lware	Connected.		Powered By GUI Composer TH TEXAS INSTRUMENTS

Figure 8-1. Open an Existing Configuration

Finally, device icons are provided on the left-hand-side which can be selected to create a single or multi-PMIC application, as shown in Figure 8-2. As devices are added the Device Name can be edited and the Master/Slave selection can be made. The GUI requires unique device names and only one master.

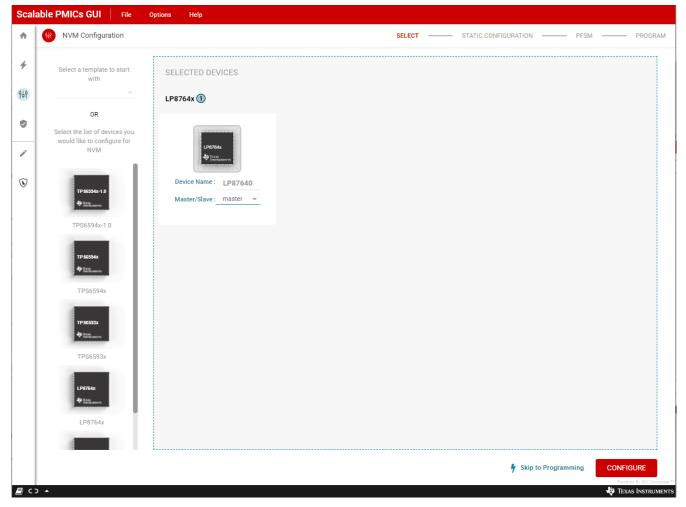


Figure 8-2. Starting from a blank template

Once the configuration is uploaded or the devices for the application selected, the development flow will move through the Static Configuration and PFSM perspectives and then finally to the Program perspective as highlighted in Figure 8-3. Section Section 8.2.1 will describe how to program an existing NVM Configuration using the *Skip to Programming* option found at the bottom of Figure 8-3.

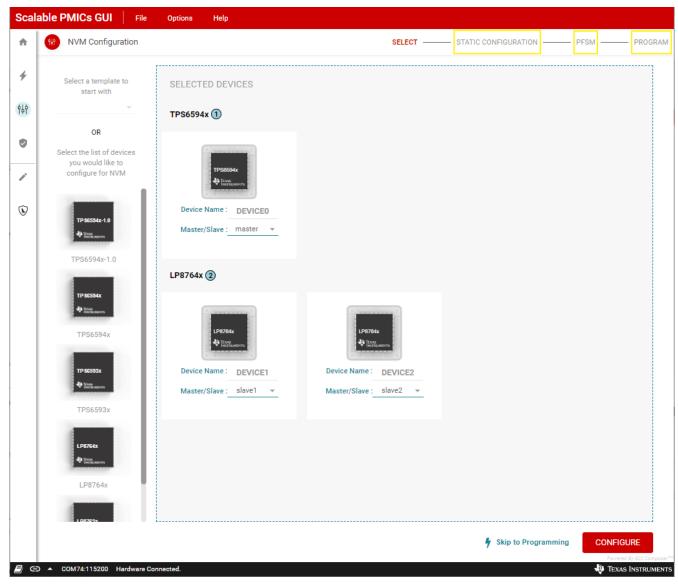


Figure 8-3. Configuration Development Flow

Note

It is not recommended to change or edit the selected devices of an existing configuration, with the exception of the device name. Doing so can break dependencies found in the PFSM. If during development it is discovered that the number or type of devices was defined in error, then a new configuration should be restarted from a blank or existing template.

8.1.1 Static Configuration

The Static Configuration perspective provides a similar interface as to what is found in the Quick-start page. The recommended flow is to start with the System Info tab on the far left, updating each block within the System Info tab and then proceeding to the next configuration tab. In a multi-device system, simply select the device to be configured from the Select a device to configure drop-down menu at the top left of the page.

Within each block are a list of registers and fields which directly match the device register and field names. It is recommended to use the data sheet specification to understand and properly set the field values for a given application. Within the BUCK blocks there is an additional graphical selection tool, see Figure 8-4, to abstract the register settings into the use cases also described in the device data sheet. The graphical selection tool will appear in the far right column of the display, providing the Configuration Use case name as well as the recommended inductor value.



NVM Configuration					SELECT	- STATIC CONFIGURATION - PFSM - PROGR
Static Configuration	Select a device to c	onfigure DEVICE0 👻 📋				
SYSTEM INFO	BUCK	LDO GPIO	INTERFACE INTERRUPT M	IASKS MISCE	LLANEOUS	
ock	T _x T	Register T _× T	Field	$\overline{\tau}_{\rm x} \overline{\tau}$	Value	How do you like to setup Buck1?
ick1	Ō	BUCK1_CTRL	BUCK1_FPWM		PFM and PWM operation (AUT0 moc $$	Is this rail used for VTT?
ack2	Ū		BUCK1_FPWM_MP		Automatic phase adding and sheddir $~~$	Yes No
uck3	Ū		BUCK1_VSEL		BUCK1_VOUT_1	What is this rail's switching frequency?
luck4	Ū		BUCK1_RV_SEL	Ø	Disabled V	
uck5	Ū	BUCK1_CONF	BUCK1_SLEW_RATE		10 mV/µs 🗸	
			BUCK1_ILIM		4.5 A 🗸	Does this rail want to be optimized for multiphase configuration?
		BUCK1_VOUT_1	BUCK1_VSET1		0.3 V ~	
		BUCK1_VOUT_2	BUCK1_VSET2			What is the output of this rail?
		BUCK1_PG_WINDOW	BUCK1_OV_THR		+3% / +30mV 🗸	
			BUCK1_UV_THR		-3% / -30mV 🗸	What is the output capacitance on this rail?
		RAIL_SEL_1	BUCK1_GRP_SEL		No group assigned V	Greater Than 100 UF Less Than 100uF
						Selected Configuration
						4.4MHz Multiphase Configuration
						Recommended Inductor Value
						220nH
						Please validate Static Configuration to proceed Validate Configuration DEFINE PF3

Figure 8-4. BUCK Static Configuration

Note Only one device is visible at a time. Be sure that all devices in the application are defined.

Within the Static Configuration perspective, the GUI is monitoring the validity of the configuration. Specifically, for multi-device solutions the GUI is making sure that both the power (VCCA and nPWRON) and interface selections match. By clicking on the *Validation Failed* text at the bottom of the perspective a pop-up window, as shown in Figure 8-5, will describe all of the issues which are invalid and preventing the next stage of the development.

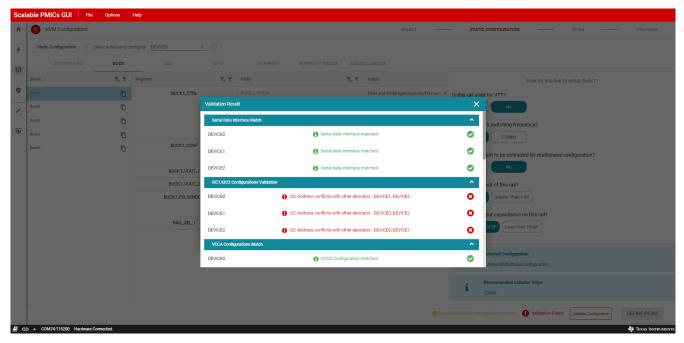


Figure 8-5. Static Configuration, Failed Verification

In this example, all three devices have the same I²C address(es). After updating each device to a unique address, the GUI now shows Validation Success and the Define PFSM button is now active.



Scale	able PMICs GUI File Options	Help						
A	NVM Configuration					STATIC CONFIGURATI	ON PFSM	
+	Static Configuration Select a device to c	onfigure DEVICE2	_ 0					
949			INTERFACE					
	Block T _× T	Register	T x T	Field T _x T	Value			
0		SERIAL_IF_CONFIC				v V		
1			Validation Resu			×		
•		I2C1_ID_REG	Serial Data Inf	f) Serial data interface ma	tobast			
		I2C2_ID_REG		_				
			DEVICE1	Serial data interface ma		•		
			DEVICE2	Serial data interface ma	.tches!	•		
				nfigurations Validation		^		
			DEVICE0	Valid I2C1/I2C2 Addres	sses!	•		
			DEVICE1	Valid I2C1/I2C2 Addres	ssest	•		
			DEVICE2	Valid I2C1/I2C2 Addres	sses!	•		
			VCCA Configu	arations Match		^		
			DEVICE0	Ø VCCA Configuration ma	itches!	•		
							Validation Success	DEFINE PFSM
<i>E</i> e	COM74:115200 Hardware Connected.							👋 Texas Instruments

Figure 8-6. Static Configuration, Passing Verification

In addition to the check of the static settings, in devices which support functional safety, there is an additional check of the safety related features. By clicking on the *Functional Safety Assumptions not met* text, a pop-up window, as shown in Figure 8-7, displays. The window lists the parameters related to the device's functional safety assumptions. Refer to the device's functional safety manual and the application's functional safety goals, in order to confirm that the selected settings meet their functional safety target.

NVM Configuration						ST.	ATIC CONFIGURATION		
Static Configuration	Select a device to c	onfigure DEVICE2	_ 0						
			INTERFACE INTERRUPT MASKS						
Block	Τ × Τ	Register	T _x T Field	τ, τ	Value				
	Ö	SERIAL_IF_CONFIG				v			
			Functional Safety Warnings			>	×		
			DEVICEO			^			
		I2C1_ID_REG	VCCA			Warning			
		I2C2_ID_REG	VCCA_VMON_EN	VCCA_VMON_EN selection may n	not meet safety assumption	0			
			Buck			Warning			
			BUCK1_RV_SEL	BUCK1_RV_SEL selection may no	t meet safety assumption	0			
			BUCK2_RV_SEL	BUCK2_RV_SEL selection may no	t meet safety assumption	0			
			BUCK3_RV_SEL	BUCK3_RV_SEL selection may no	t meet safety assumption	0			
			BUCK4_RV_SEL	BUCK4_RV_SEL selection may no	t meet safety assumption	0			
			BUCK5_RV_SEL	BUCK5_RV_SEL selection may no	t meet safety assumption	0			
			LDO						
			LD01_RV_SEL	LDO1_RV_SEL selection may not i	meet safety assumption	0			
			LD02_RV_SEL	LDO2_RV_SEL selection may not	meet safety assumption	0			
							umptions not met 🛛 🚫 Validation	Success Validate Configuration	DEFINE PFSM

Figure 8-7. Function Safety Assumptions Check

When transitioning to the PFSM perspective from the static settings if any values were not updated, then a warning message will appear. Values that are not updated will appear with a yellow highlight around the value. In this example, only the I²C addresses have been updated. Texas Instruments recommends that all settings that are highlighted as unchanged should be reviewed and confirmed.

	A Configuration	ı						SELECT		STATIC CONFIGURATION		PFSM	- PROGRAM
Static Co	onfiguration	Select a device to c	onfigure DEVI	CE2	- D								
	SYSTEM INFO	BUCK		GPIO	INTERFACE	INTERRUPT MASKS MIS	CELLANEOUS						
Block		T × T	Register		₹. ₹	Field	T × T	Value					
Serial Interfac	c	Ū		SERIAL_IF_CON	IFIG	I2C_SPI_SEL		120	~				
						I2C1_SPI_CRC_EN	0	CRC disabled	~				
						I2C2_CRC_EN	0	CRC disabled	~				
				I2C1_ID_REG		I2C1_ID		0x50	~				
				I2C2_ID_REG	3	12C2_ID		0x14	~				
									• Functional	Safety Assumptions not met	Validation Success	Validate Configuration	DEFINE PFSM

Figure 8-8. Example of non-updated Static Configuration Values

Note

The GUI does not provide an auto-save feature. Save often using the Save Configurations below the File tab shown in Figure 8-9.



Figure 8-9. Save Often

8.1.2 Pre-Configurable Mission States (PFSM)

While the static configuration was done on a per device basis, the perspective of the PFSM is that of all devices working together. Individual commands are created for each device, but they are grouped in the context of states and transitions of the system solution.

When entering the *PFSM* perspective and no template was chosen from the *SELECT* perspective, template options will be presented to aid in the development of the PFSM. Figure 8-10 shows the two templates available.



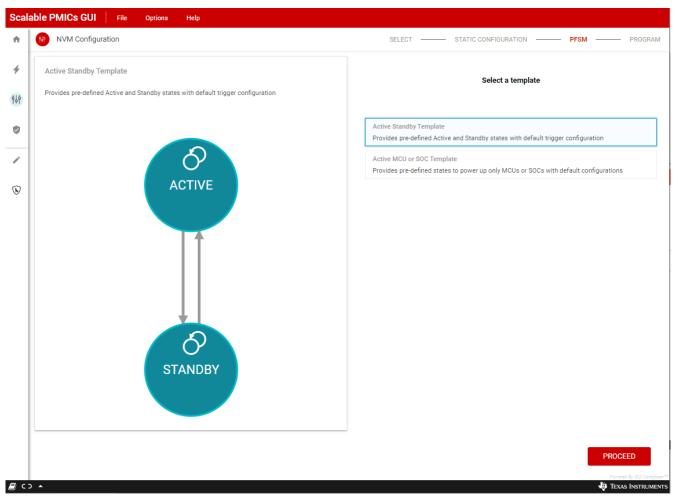


Figure 8-10. PFSM Starting Templates

Once the template is selected, then the GUI transitions into the PFSM perspective.

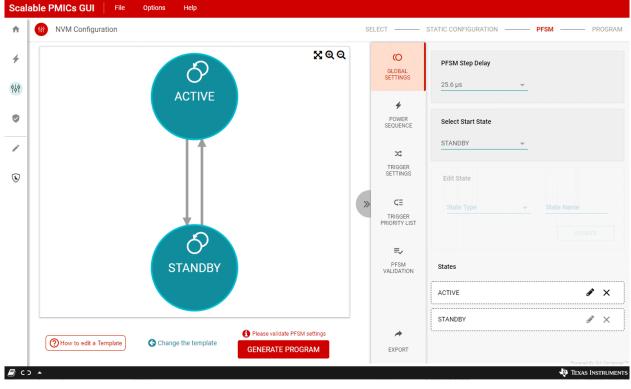


Figure 8-11. PFSM Configuration

The PFSM perspective provides a work space on the left-hand-side to draw the PFSM. How to add and remove states and transitions is described in Table 8-1 as well as within the *How to edit a Template* pop-up window, located in the bottom left corner.

Action	Interface
Create a new state	Shift+left mouse click
Create a transition	Shift+left mouse click+drag from within the source state to the destination state
Create a loop	Left mouse click on the loop icon within the state
Move a state	Left mouse click within the state and drag
Delete	Left mouse click on the state, transition, or loop and then press the backspace(delete)
Zoom	Place mouse within the drawing space and scroll
Pan	Left mouse click + drag from any blank space within the work space

Table 8-1. Actions to Edit the State Machine

Note

The GUI does not provide an auto-save feature. Save often using the *Save Configurations* below the File tab shown in Figure 8-9.

Developing the PFSM can be an iterative and non-linear process. The linear process listed here is only intended to show functionality and a basic work flow. It is possible to return to earlier steps (steps 1-5) at any time and make changes.

- 1. Create a state diagram
 - a. Adding States
 - b. Adding Transitions (Triggers)
- 2. Global Settings
- 3. Power Sequences
- 4. Trigger Settings
- 5. Trigger Priority List

6. PFSM Validation

8.1.2.1 Creating a State Diagram

The state diagram which is developed in the PFSM panel includes the user defined mission states and three hardware states, **SAFE_RECOVERY**, **LP_STANDBY**, and **RUNTIME_BIST**. The user defined mission state **STANDBY** is required in order to bridge between the hardware states and the missions states. The **SAFE** state is required as the transition between mission states and the hardware state **SAFE_RECOVERY**. As shown in Figure 8-12, the panel focuses on the mission states and the **SAFE_RECOVERY**, **LP_STANDBY**, and **RUNTIME_BIST** hardware states which can be accessed from the mission state via the PFSM.

WARNING

STANDBY, SAFE, and SAFE RECOVERY states are required, as defined in the data sheet, in order to meet device specifications.

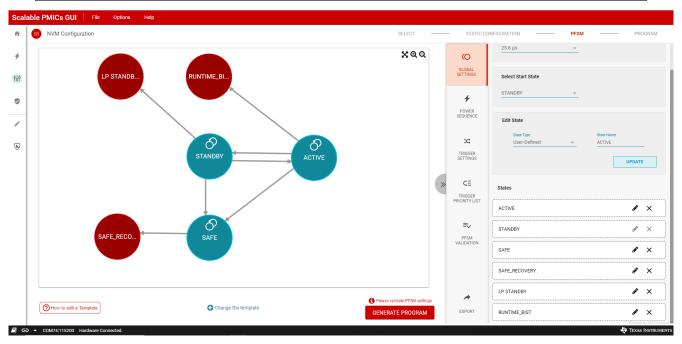


Figure 8-12. PFSM State Diagram Panel

Figure 8-13 shows the complete state machine with the additional transitions associated between the hardware and mission states. The complete state machine can be viewed by selecting the export icon (next to GENERATE PROGRAM) in the lower right corner. Please refer to the device specification for a more detailed description of the states and the transitions.



Scalable PMICs GUI File Options Help	
Preview	×
	X&Q
	EXPORT
■ C3 ▲ C0M74:115200 Hardware Connected.	🐺 Texas Instruments

Figure 8-13. Complete State Diagram

8.1.2.2 Global Settings

As states are added they will appear in the *GLOBAL SETTINGS* panel, as shown in Figure 8-14. The names of the states are configurable but the type of state is limited to either a user definition or a Hardware State. Hardware states are already defined within the finite state machine within the PMIC and by definition there is no power sequence associated with transitions to hardware states and no transitions can be defined from Hardware states.

CO GLOBAL SETTINGS	PFSM Step Delay 25.6 µs ~
P OWER SEQUENCE	Select Start State
TRIGGER SETTINGS	Edit State State Type State Name User Defined ~ ACTIVE
CE TRIGGER PRIORITY LIST	UPDATE
=,	States
PFSM VALIDATION	ACTIVE & X
	STANDBY I X
	SAFE 🖋 🗙
*	SAFE_RECOVERY X
EXPORT	LP STANDBY

Figure 8-14. Global Settings

In addition to the states, from the *GLOBAL SETTINGS* the user can select which state the PFSM will start from. This effectively determines which triggers will be unmasked once the device leaves the hardware finite state machine and transitions to the user PFSM, mission state.

The *PFSM Step Delay* setting is also part of the *GLOBAL SETTINGS*. The PFSM Step Delay setting will determine which time interval the GUI will use to attempt to meet the required delays found throughout the power sequences. The actual delays are a function of the desired delay, instruction being used, as well as the PFSM Step Delay. Instruction delays are limited to either 6 or 8-bit multiples of the step delay. In the event that the GUI cannot reach the desired delay time with the existing step delay, then the GUI will add an instruction to change the step delay temporarily to reach the desired delay time. If the step size is actually larger than the desired



delay, then the GUI inserts a command to change the step delay to support the delay time, and after the delay is complete, the GUI will insert another command to change the step delay back to the original value. Whenever the GUI makes an adjustment, the smallest step size is chosen which can still provide the desired delay. Table 8-2 is provided to exemplify the actual delay versus requested delay times as a function of the PFSM Step Delay.

Note

Choosing a PFSM Step Delay which is a common factor of the majority of the delays needed in power sequencing will optimize the memory usage in the device.

PFSM Step Delay (us)	Delay Requested(us)	Delay Instruction	Actual Delay ³ (us)
25.6	2500	DELAY_IMM (8-bit)	2483.2
		REG_WRITE_VCTRL_IMM(6-bit)	2457.6
204.8	40000	DELAY_IMM (8-bit)	39936
		REG_WRITE_VCTRL_IMM(6-bit)	39321
409.6	300000	DELAY_IMM (8-bit)	299827
		REG_WRITE_VCTRL_IMM(6-bit)	294912

Table 8-2. Examples of Requested and Actual Delay times

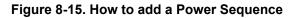
8.1.2.3 Power Sequence

Power sequences are dependent upon the target state definition, and therefore it is required to define the state in the global settings before creating a power sequence. In addition to the target state, there are options to select the sequence type. The sequence types *Power Up*, *Power Down*, and *Reset* come pre-populated with ACTIVATE and or DEACTIVATE commands based upon the sequence type. All sequence types have the TRIG_MASK pre-populated. These commands are described in Section 8.1.2.3.1.

Once a new sequence has been created, then the sequence name is added to the list of sequences (see Figure 8-15), and the sequence can be edited (lightning bolt), updated (pencil), or deleted ('X'). The update simply allows the name of the sequence to be updated as well as the target state. Using the edit icon will open a new window as shown in Figure 8-16.



GLOBAL SETTINGS	ADD SEQUENCE Sequence Name Ex: anv2active	Target State Select state ▼	
+ POWER SEQUENCE	Sequence Type Power Up Power Down	Reset Others	
TRIGGER SETTINGS	SEQUENCES STANDBY2ACTIVE		<i>i</i> ×
CE TRIGGER PRIORITY LIST			
PFSM VALIDATION			
EXPORT			ed By GUI Composer™ S INSTRUMENTS



8	SEQUENC standby:		TARGET STATE: ACTIVE			
		ADD ACTION				
		Device	v	Resource/Commands	Ŧ	
				ADD		
Power Sequ	ence Comm	ands				X 🗋 🖄 🏌
DEVICE0		ACTIVATE			Rail Conr	nection
DEVICE1		ACTIVATE				× 0 0 📋
DEVICE2		ACTIVATE				/ 0 0 📋
DEVICE0	1	TRIG_MASK				🖍 🖸 🔘 🧻
DEVICE1	1	TRIG_MASK				/00 📋
DEVICE2	1	TRIG_MASK				100
						Powered By GUI Composer*

Figure 8-16. Power Sequence Command Window

From this window, commands for each PMIC can be added and the timing relationship between each command is represented. Arrows are provided to move commands within the sequence.

Note

Delays in the *ADD ACTION* or *UPDATE ACTION* windows are relative to the previous action. Delays shown in the Power Sequence Commands list are relative to the start of the sequence.

There is a distinction between commands which have Rail Connections and commands which do not. The commands with Rail Connections are typically representative of physical outputs from the device and voltage monitors. The Rail Connections are what will appear in the power sequence diagram as described in section Section 8.1.2.3.3. The names of the Rail Connections are editable and can be updated to more meaningful names related to the application.

Initially, the trigger masks for each device are provided. As additional commands are added, they will always be placed above the trigger masks. The trigger masks can be moved in the sequence order, but typically these are the last commands in the sequence. The trigger mask at the end of the power sequence is automatically generated based upon the available triggers of the destination state. This mask can be edited to mask triggers from triggering a power sequence and a state change. Before editing the mask. it is recommended to define the triggers as described in the Section 8.1.2.4.

8.1.2.3.1 Power Sequence Resources and Commands

This section lists the different commands and resources available. The description is provided with reference to the PMIC instruction set which is described in the device data sheet.

Resources and Commands

Not all commands are available on all devices. Refer to the device data sheet.

1. BUCKx

The BUCK resource is an abstraction of the assembly instructions REG_WRITE_VCTRL_IMM and REG_WRITE_VOUT_IMM. Selecting either the VCTRL or the VOUT tab in the update action window will determine which instruction is applied. Within each tab are the various parameters of each instruction.

BUCKx commands are available for each available BUCK. If BUCKs are multi-phased then the grouping is reflected in the resource name, for example BUCK1_2_3_4, but only the master BUCK information is shown in the parameter window. In the resulting program, the master buck will be the only one reflected in the instruction.

2. BUCKx Monitor

The BUCK monitors are a special subset of the REG_WRITE_VCTRL_IMM and REG_WRITE_VOUT_IMM instructions. The parameters which are not used for this resource are not selectable. The VIN tab is the same but represents the monitor voltage setting.

3. LDOx

Similar to the BUCK and BUCK Monitor Resources, this is an abstraction of the assembly instructions REG_WRITE_VCTRL_IMM and REG_WRITE_VOUT_IMM. Selecting either the VCTRL or the VOUT tab in the update action window will determine which instruction is applied. Within each tab are the parameters of each instruction.

4. nRSTOUT

The nRSTOUT command writes or clears the nRSTOUT bit found in the MISC_CTRL register. The command is an abstraction of the REG_WRITE_MASK_IMM assembly instruction to the address 0x81, register MISC_CTRL. The data and mask are determined by the selection of unchanged, high, or low. The use of the *unchanged* selection has no impact and only serves as a delay of one instruction cycle.

5. WAIT

The wait command provides a conditional branch in the instruction set, similar to an *if* or *while* statement. When the timeout is provided, the wait condition is effectively an *if statement* continuing to the next instruction if the condition is true and jumping to the destination if the condition is false. If the timeout is non-zero, then the PMIC will wait until the condition is true and then execute the next instruction or until the timeout is



reached and then jump to the destination. The destination must always be after the wait command because the skip count of the wait instruction is always positive.

Note

Using a timeout is not recommended with multiple devices as the other devices have no information of how long the wait took if the condition was met before the timeout.

6. JUMP

The jump command is special implementation of a wait command which has a timeout of *0* and a condition which is always false. The destination must be after the jump command.

7. RESET_BUCKs

The RESET_BUCKs command is a direct write to the BUCK_RESET_REG register at address 0x87. In this command the resets are per BUCK and each BUCK must be configured even when the BUCKs are multiphased. The RESET_BUCKs command is translated into a REG_WRITE_MASK_IMM command to address 0x87 to either clear or set bits 0 through 4, representing BUCKS 1-5.

CAUTION

The RESET_BUCK command will stop the BUCK switching. This command should only be used in power down sequences.

8. GO_TO_LP_STANDBY

The GO_TO_LP_STANDBY command is a direct write of *1* to the LDOINT disable bit found in the LDOINT_CTRL register, address 0x21. LDOINT is a self-clearing bit. The GO_TO_LP_STANDBY command is a translated into a REG_WRITE_MASK_IMM command to address 0x21, with a data value of 0x01 and a mask of 0xFE.

9. SET_WD_LONGWINDOW

The SET_WD_LONGWINDOW command is a direct write to the WD_LONGWIN field found in the WD_LONGWIN_CFG register, address 0x405. This field is for programming the duration of the Watchdog Long Window. The SET_WD_LONGWINDOW command is a translated into a REG_WRITE_MASK_IMM command to address 0x405, with a data value range from 0x00 to 0xFF, and a mask of 0x00. A value of 0x00 is approximately 100ms while a value of 0xFF is approximately 12 minutes.

10.GO_TO_LONGWIN

The GO_TO_LONGWIN command is a direct write of *1* to the WD_RETURN_LONGWIN bit found in the WD_MODE_REG register, address 0x406. This command will cause the watchdog to return to the Long-Window after completion of the current watchdog-sequence. The GO_TO_LONGWIN command is a translated into a REG_WRITE_MASK_IMM command to address 0x406, with a data value of 0x01 and a mask of 0xFE.

11.FIRST_STARTUP_DONE

The FIRST_STARTUP_DONE command is a direct write of *1* to the FIRST_STARTUP_DONE bit found in the RTC_CTRL_2 register, address 0xC3. The FIRST_STARTUP_DONE command is a translated into a REG_WRITE_MASK_IMM command to address 0xC3, with a data value of 0x80 and a mask of 0x7F.

12.INCREASE_RECOVERY_COUNT

The INCREASE_RECOVERY_COUNT command is a direct write of *1* to the INCREASE_RECOVERY_COUNT bit found in the RECOV_CNT_PFSM_INCR, address 0xA5. This bit is self-clearing, so each command increments the recovery counter. The INCREASE_RECOVERY_COUNT command is a translated into a REG_WRITE_MASK_IMM instruction to address 0xA5, with a data value of 0x01 and a mask of 0xFE.

13.ACTIVATE

The ACTIVATE command is a composite of several commands associated with a power up sequence. These commands include the following:

a. REG_WRITE_MASK_IMM to ENABLE_DRV_STAT to clear SPMI_LPM_EN.

- b. REG_WRITE_MASK_IMM to VCCA_VMON_CTRL to either clear or set VCCA_VMON_EN, depending upon the value selected from the ACTIVATE command window.
- c. REG_WRITE_MASK_IMM to MISC_CTRL to either clear or set AMUXOUT_EN/REFOUT_EN and CLKMON_EN, depending upon the value selected from the ACTIVATE command window. Included in this instruction is the clearing of LPM_EN.

14.DEACTIVATE

The DEACTIVATE command is a composite of several commands associated with a power up sequence. These commands include the following:

- a. REG_WRITE_MASK_IMM to ENABLE_DRV_STAT to set SPMI_LPM_EN.
- b. REG_WRITE_MASK_IMM to VCCA_VMON_CTRL to either clear or set VCCA_VMON_EN, depending upon the value selected from the DEACTIVATE command window.
- c. REG_WRITE_MASK_IMM to MISC_CTRL to either clear or set AMUXOUT_EN/REFOUT_EN, depending upon the value selected from the ACTIVATE command window. Included in this instruction is the setting of LPM_EN.

15.ENDRV

The ENDRV command is a direct write to the FORCE_EN_DRV_LOW bit found in the ENABLE_DRV_STAT register, address 0x82. The ENDRV command is a translated into a REG_WRITE_MASK_IMM command to address 0x82, with a data value of 0x08 or 0x00, and a mask of 0xF7.

16.DELAY_IMM

The DELAY_IMM command is a direct representation of the DELAY_IMM instruction. The delay specified in this command is applied to all devices.

Note

The assembler will optimize DELAY_IMM instructions and combine with the following instruction if that instruction includes a timing parameter.

17.REG_WRITE_MASK_IMM

The REG_WRITE_MASK_IMM command is a direct representation of the REG_WRITE_MASK_IMM instruction. The REG_WRITE_MASK_IMM command includes a mask to write or clear specific bits without impacting other bits within the register.

18.TRIG_MASK

The TRIG_MASK command is a direct representation of the TRIG_MASK instruction. The trigger mask will determine which interrupts are enabled and disabled. Using the Automatic trigger will set the trigger based upon the trigger settings from the TARGET STATE.

19.REG_WRITE_IMM

The REG_WRITE_IMM command is a direct representation of the REG_WRITE_IMM instruction. The REG_WRITE_IMM command overwrites all bits within the register specified.

20.REG_WRITE_MASK_SREG

The REG_WRITE_MASK_SREG command is a direct representation of the REG_WRITE_MASK_SREG instruction. The REG_WRITE_MASK_SREG command includes a mask to write or clear specific bits without impacting other bits within the register. The data is sourced from the specified scratch register.

21.SREG_READ_REG

The SREG_READ_REG command is a direct representation of the SREG_READ_REG instruction. This command copies the contents of the register to the specified scratch register.

22.SREG_WRITE_IMM

The SREG_WRITE_IMM command is a direct representation of the SREG_WRITE_IMM instruction. 23.DELAY_SREG

The DELAY_SREG command is a direct representation of the DELAY_SREG instruction. This delay is different than the other delays found in the resources and commands. The delay is only applied to the device specified.

8.1.2.3.2 Sub-sequences

Sub-sequences are groups of commands within the power sequence and are associated with the JUMP or WAIT instructions. Functionally, the sub-sequence is simply a destination label for the JUMP or the WAIT statements to *jump* to. Graphically, the sub-sequence can be used to group commands and then the entire group can be moved within the power sequence. In Figure 8-17, the WAIT instruction is used to test GPIO1, if GPIO1 is high, then the timeout occurs and the execution jumps to the SKIPBUCK5 label and continues execution. Specifically, if GPIO1 is low then BUCK5 is enabled, if GPIO1 is high, then the regulator is not enabled. Figure 8-18 shows that there are no instructions within the sub-sequence. Instructions placed within or after the sub-sequence will be chronologically equivalent. Again, the main benefit of placing instructions within the sub-sequence is to logically group the commands and then to move them as a group when needed.

LECT	STATIC (CONFIGURATION	PFSM	PROGRAM
\otimes	SEQUENCE NAME standby2active	Target State ACTIVE	UPDATE	
	UPDATE ACTION Device TPSMSTR	·	Resource/Commands	v.
	Condition GPI01 Unit	▼ Type LOW Destination	▼ 0	-
	US 🔻	SKIPBUC	•	DATE
Power	Sequence Commands			X 🗋 🗂 † 4
TPSMS.	BUCK1_2		Rail Connec	tion 🔮 🕐 🧻
LPSLV1	BUCK1_2_3_4		Rail2	- 🗸 🖸 🔨 盲
LPSLV2	BUCK1_2_3_4		Rail3	- 🗸 📀 💿 🔳
TPSMS	TR nRSTOUT		Rail4	- 🗸 🖸 🔮 🔳
TPSMS	TR WAIT			Texas Instruments

Figure 8-17. WAIT Command Action



SE	LECT —	STATIC CONFIGURATION	PFSM	PROGRAM
\otimes	SEQUENCE NAME: standby2active	TARGET STATE: ACTIVE		
	ADD ACTION			
	Device	*	Resource/Commands	•
			ADD	
Power Sequ	uence Commands			Rail Connection
DEVICE0	ACTIVATE			
DEVICE1	ACTIVATE			/ O O 📋
DEVICE2	ACTIVATE			🖍 📀 💿 🥫
DEVICE0	BUCK1			Rail1 🧪 🕢 🕚 📋
DEVICE1	BUCK1_2_3_4			Rail2 🖍 🚱 🕚 📋
DEVICE2	BUCK1_2_3_4			Rail3 🧪 🐼 🔮 🧵
DEVICE0	WAIT			🖍 😳 🙂 🧵
DEVICE0	BUCK5			Rail5 🖍 🚱 🔮 🧵
D0_B5_SKIP				+ += += 🔋
		Add actions to sub seq	uence using + button	
DEVICE0	TRIG_MASK			🖍 📀 💿 🧵
DEVICE1	TRIG_MASK			🗸 📀 😋 🧵
DEVICE2	TRIG_MASK			100
				🐺 Texas Instruments

Figure 8-18. Empty Sub-Sequence

Note

WAIT and JUMP statements can only jump forwards in the sequence of commands. The destination can never be placed before the JUMP or WAIT statement.

8.1.2.3.3 Power Sequence Editing Tools

In addition to the four editing tools for each individual command (update, move up, move down, delete), there are four tools available for editing the power sequence in its entirety. From left-to-right, the tools are export power sequence, copy sequence, paste sequence, and reverse sequence (see Figure 8-19). The copy, paste, and reverse sequence tools create a convenient way to copy a power sequence, for example, a power-on sequence, and to paste in a new sequence, then reverse in order to create a power-off sequence.

Note

The reversal is not applied to the TRIG_MASKS as these are always intended to be at the end of the sequence. The reversal is only of the order of the commands and not the timing relationship or polarity; enable does not become disable.



LECT	STATIC	CONFIGURATION	PFSM	- PROGRAM
\otimes	SEQUENCE NAME standby2active	Target State	UPDATE	
	ADD ACTION			
	Device	~	Resource/Commands	<u> </u>
			ADD	
Power	Sequence Commands			X 🗋 🕯 🕯
TPSMS	BUCK1_2		Rail Connection	🖍 📀 🙂 🥫

Figure 8-19. Power Sequence Tools

The export power sequence provides a more complete graphical view which can be exported. From this view the user has the ability to provide inputs for the conditional WAIT command and generate timing diagrams for different conditions. As shown in Figure 8-20, either the true condition of the timeout can be selected and the timing diagram is updated appropriately.

Note

Texas Instruments recommends exporting power sequences to confirm that the timing aligns with system requirements.

EXPORT POWER SEQUE	EXPORT POWER SEQUENCES											
CONTROL RESOURCE	S EXPORT PREVIEW											
	TPSMSTR GPI01: TIMEOUT LOW											
GPI01: TIMEOUT	LOW											
DEVICE	SEQUENCE NAME	DELAY VIEW	TOTAL DELAY	RAIL CONNECTION								
TPSMSTR	BUCK1_2_3_4		0 us	Rail1								
LPSLV1	BUCK1_2_3_4		1000 us	Rail2								
LPSLV2	BUCK1_2_3_4		2000 us	Rail3								
TPSMSTR	nRSTOUT		5000 us	Rail4								
TPSMSTR	WAIT	GPI01 = LOW										
TPSMSTR	BUCK5		5000 us	Rail6								

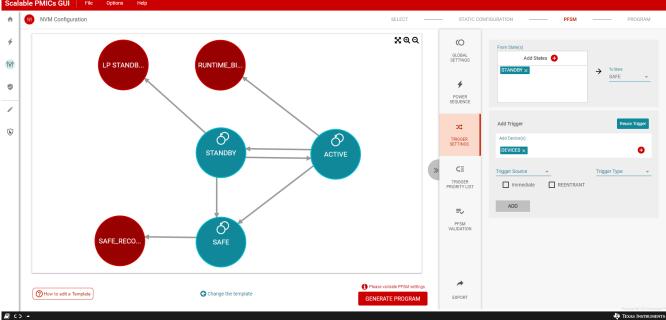
Figure 8-20. Exported Sequence with Variable Conditions

8.1.2.4 Trigger Settings

The maximum number of triggers available is 28. Please refer to the device specification for the usage of reserved triggers. The GUI will ensure that the maximum number of triggers is not exceeded and manage the usage of triggers across devices in a multiple PMIC application.



The trigger settings identify what triggers will move the PMIC operation from one state to another. In the context of the GUI, the arrows between states (or arrows looping back to the same state) must have at least one trigger definition. An example is used to outline the steps configuring the trigger settings. For this example, the *IMMEDIATE_SHUTDOWN* going high on any device will trigger all devices to execute a power down sequence and then transition to the **SAFE** state, which in turn will automatically transition all devices, without power sequence, to the hardware state **SAFE_RECOVERY**, to reset the devices. The following steps are how to setup this example.



1. Select the transition between the **STANDBY** and **SAFE** states, by clicking on the transition in the diagram.

Figure 8-21. Trigger: STANDBY to SAFE

- 2. In the From States add ACTIVE, so that both the ACTIVE and STANDBY states are selected.⁴
- 3. In the 'Add Devices' select Any, so that all devices appear in the window⁵.
- 4. From the Trigger Source drop-down menu, select IMMEDIATE_SHUTDOWN.
- 5. From the Trigger Type drop-down menu, select HIGH.
- 6. Select the *Immediate* check box. This means that the trigger can happen immediately and does not wait for the current sequence to finish.

⁴ The Reuse Trigger button is an alternative option. This would mean that step 2 would be omitted. After step 7, the ACTIVE to SAFE transition would be selected. At this point the 'Reuse Trigger' button would be selected and then the same trigger used for the STANDBY to SAFE would be selected.

⁵ While an example, Texas Instruments recommends that the IMMEDIATE_SHUTDOWN trigger be present in all devices. For other triggers, it is acceptable that the trigger is present in only one device.

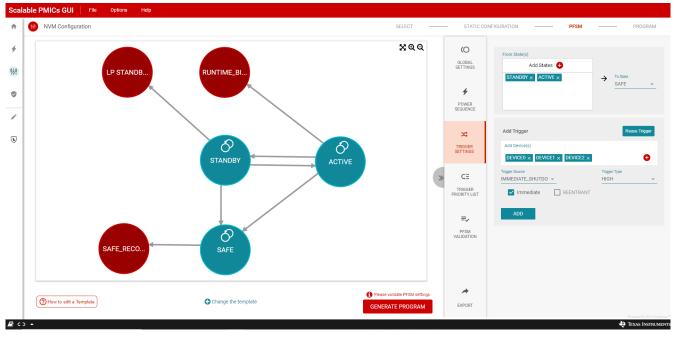


Figure 8-22. Trigger: STANDBY to SAFE (continued)

- 7. Click ADD
- 8. Now click on the transition between **SAFE** and **SAFE_RECOVERY**.
- 9. In the Add Devices window, select Any
- 10. From the *Trigger Source* drop-down menu, select 1, and from the *Trigger Type* select *High*. This combination is always true and will result in a trigger.

CAUTION

A *Trigger Source* of 1 and a *Trigger Type* of *High* will always result in a trigger.

Note

Since **SAFE_RECOVERY** is a hardware state the trigger will not have an associated power sequence. This is indicated by the EXT attribute in the trigger description. Similarly, the **RUNTIME_BIST** will also have the EXT attribute.

11. Click ADD



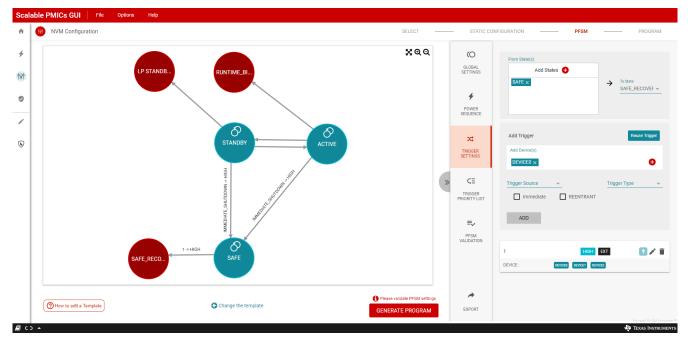


Figure 8-23. Trigger: SAFE to SAFE_RECOVERY

At the bottom of the TRIGGER SETTINGS, highlighted in Figure 8-23, is a summary of the trigger(s) associated with a transition. A scroll bar is provided to see the bottom of the pane. The last step is to associate a power sequence with the transition. Since SAFE_RECOVERY is a hardware state, the EXTERNAL flag is set and no sequence is needed in the transition to SAFE_RECOVERY. The transitions to SAFE, however, do require a sequence. Making the association between the trigger and the sequence is listed in the following instructions.

- 1. Click on the transition between **STANDBY** and **SAFE** (or **ACTIVE** and **SAFE**).
- 2. Click the lightning bolt icon. This will bring up a window showing all of the sequences which have the same destination or target state. In this case there is only one, *any2safe*.

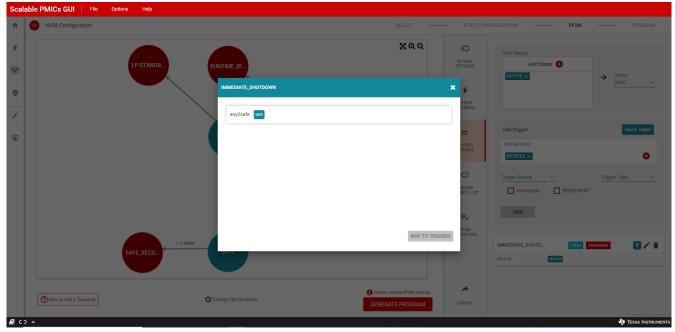


Figure 8-24. Mapping a Sequence to a Trigger

3. Select the sequence and then click *MAP TO TRIGGER*. The Trigger Setting for the transition is now complete.



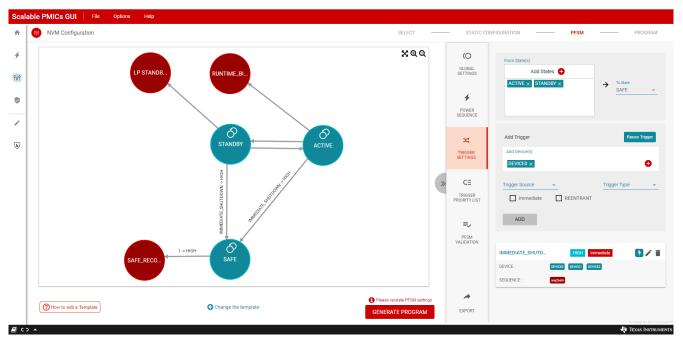


Figure 8-25. Completed Trigger Settings

Once all of the transitions have been assigned triggers and all of the triggers have been associated with power sequences, then the default TRIGGER MASKS within the power sequences will be updated. Please note the various components and relationships discussed to this point:

1. States

The states are either hardware or mission states.

2. Transitions

Transitions have a source and target state. Transitions can have multiple triggers but require at least one. Transitions to the same target state can share the same trigger.

3. Triggers

Available triggers are defined in the device specification. Each trigger can have only one power sequence associated with it. Multiple triggers can share the same power sequence. In the special case that the transition target state is a hardware state, the trigger type is EXT and there is no power sequence.

4. Power Sequences

Power sequences are defined in terms of the target state and therefor can potentially be associated with multiple triggers or transitions. Within the power sequence is the trigger mask. The automatic trigger mask is defined by all transitions from the target state and the triggers defined in those transitions. Manual trigger masks can be used to create custom trigger masks. In the TRIG_MASK command there is an option to select either an automatic or a manual trigger mask.

8.1.2.5 Trigger Priority List

Triggers are initially prioritized based upon the TRIG_SEL value for each trigger as defined in the data sheet. Lower values have higher priority. It is important to confirm that the priority within the TRIGGER PRIORITY LIST matches the desired priority of the application. Figure 8-26 shows the priority list from the simple example in the previous section. Click the arrows within the list to move triggers up and down in priority.



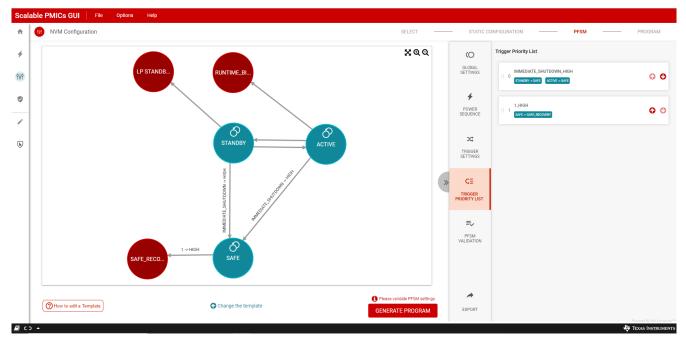
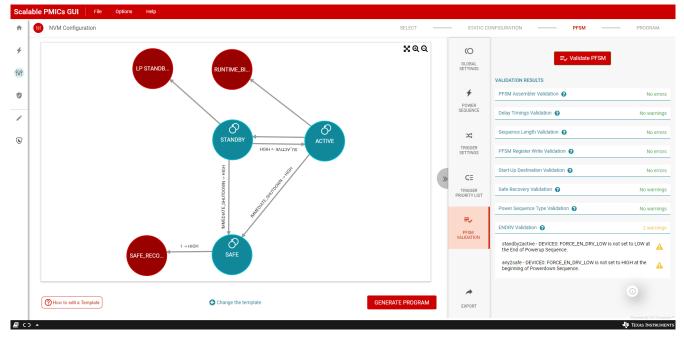


Figure 8-26. Trigger Priority List

8.1.2.6 PFSM Validation

The TRIGGER PRIORITY LIST is the last component to building a PFSM configuration. When the configuration is complete, the PFSM validation should be run in order to check and validate the PFSM content. Within the PFSM Validation view, click the *Validate PFSM* button.

Within the PFSM view, a list of results will be displayed. Any errors or warning will be accompanied by instructions and recommendations. Errors and warnings will not prevent program generation but indicate a potential risk in device performance within the application. It is recommended to address all errors as this can prevent proper compilation or file generation. Once all errors have been addressed, click the *GENERATE PROGRAM* button to move to the PROGRAM perspective.







8.2 Program

Note

Before programming is another good place to save the configuration, see Figure 8-9

The program page shows the results of the generated program in the *Generated Program* tab, as shown on the left side of Figure 8-28. This is a text format file and a scroll bar is available to view the entire content. On the right side are the control mechanisms for programming.

Scal	able PMICs GUI File Options Help	
ħ	NVM Configuration	SELECT STATIC CONFIGURATION PFSM PROGRAM
4	Generated Program Upload Program File	Choose a device to program
	1 CUSTOMER_NVM_ID=0x0	
ŶĻŶ	2 VMON_DEGLITCH_SEL=0x0	Select current interface
	3 VCCA_VMON_EN=0x0	I2C Mode SPI Mode
•	4 VCCA_OV_THR=0x0	Select Device I2C1 Address: 0x48
-	5 VCCA_UV_THR=0x0	TP\$6694x
	6 VCCA_PG_SET=0x0	PESBORX DEVICE0 I2C1 CRC Enabled: DEVICE0
	7 VCCA_GRP_SEL=0x0	I2C2 CRC Enabled:
~	8 MP_CONFIG=0x1	TPS6594x
\odot	9 BUCK1_EN=0x0 10 BUCK1_FPWM=0x0	CONNECT TO HARDWARE
	10 BUCK1_FPWM=0x0 11 BUCK1_FPWM_MP=0x0	The above settings corresponds to current device configuration.
	12 BUCK1_VMON_EN=0x0	
	13 BUCK1_VSEL=0x0	Program DEVICE0 Device
	14 BUCK1_PLDN=0x1	Save Program
	15 BUCK1_RV_SEL=0x0	
	16 BUCK1_SLEW_RATE=0x2	1 Save As Assembly Code
	17 BUCK1_ILIM=0x4	Save as assembly file to skip NVM Configuration in future programming of these
	18 BUCK1_VSET1=0x0	settings
	19 BUCK1_VSET2=0x0	
	20 BUCK1_OV_THR=0x0	Verify Connection to All Page Addresses
	21 BUCK1_UV_THR=0x0	2 Verify Connection
	22 BUCK1_GRP_SEL=0x0	
	23 BUCK1_RESET=0x0	Verify Address Conflict for Current Program
	24 BUCK1_FREQ_SEL=0x1	3 Verify Address Conflict
	25 BUCK1_SEL_NEG_OCP_HYST=0x0	M verily Audress connict
	26 BUCK1_SEL_POS_OCP_HYST=0x1	Write Configuration to Device
	27 BUCK1_SEL_ISENSE_SLOPE_COMPENSATION=0x3	
	28 BUCK1_SEL_VOUT_ADC_LEVEL=0x0 29 BUCK1_SEL_PHASE_SHEDD=0x0	4 Program Device
	29 BUCK1_SEL_PHASE_SHEDD=0x0 30 BUCK1_SEL_PHASE_ADD=0x1	
	31 EN_LOAD_COMP_BLANK=0x1	
	37 BUCK1_SEL_OUTPUT_CAPS=0x1	
/ с	> *	🐺 Texas Instruments

Figure 8-28. NVM Programming

The *Select Device* drop-down menu is provided when multiple PMICs have been configured. The associated program appears in the Generated Program tab when a device is selected. This will also determine which program will be saved and programmed.

The Select current interface will determine which physical address is used to verify the connection and program.

Two options are provided for saving the program, *Save as Assembly Code* and *Save as Binary Code*. The *Save as Assembly Code* is the same format as what is shown in the *Generate Program* tab. The *Save as Binary Code* format is of the register addresses and the hexadecimal values at those addresses. Both of these formats can be uploaded to the program page and programmed into the selected device without the use of the configuration steps, as discussed in Section 8.2.1. The *binary* format can also be used in the NVM Validation page to validate the NVM contents of a device. Once the physical connection is verified, then the device can be programmed.

Note Texas Instruments recommends saving all three file types: Configuration, Assembly, and Binary.

WARNING

Texas Instruments will not support manually edited assembly or binary files.

8.2.1 Program an Existing NVM Configuration

The NVM Configuration page can also be used to program a device with an existing NVM Configuration in the assembly or binary format. The process is simply to start at the beginning of the page and choose which type of device to program by clicking the device icon, as shown in Figure 8-29. Once a device is chosen, click the *Skip to Programming* button to go directly to the programming page.

Sca	able PMICs GUI File 0	ptions Help				
A	WVM Configuration		SELECT ———	STATIC CONFIGURATION	PFSM PROGRAM	
4	Select a template to start with	SELECTED DEVICES	 			
ŶĻŶ	· · · · · · · · · · · · · · · · · · ·	LP8764x 1				
۲	OR Select the list of devices you					
1	would like to configure for NVM	LP8764x				
\$	TP 55554x-1.0	Device Name: LP87640 Master/Slave: master 👻				
	TPS6594x-1.0					
	TP 56554x					
	TPS6594x					
	TP 86533X					
	TPS6593x					
	LP8764x					
	LP8764x					
				🕴 Skip to Programm	ning CONFIGURE	car ⁷¹
/ с	⊃ ▲				🔱 Texas Instrumen	NTS

Figure 8-29. Skip to Programming with an existing NVM Configuration

The programming perspective has changed slightly from what was described in Section 8.2. As shown in Figure 8-30, only the *Uploaded Program File* tab is available, the save options are disabled, and the *Select Device* reflects the device selection at the beginning. The interface selection should match the device being programmed. If the interface is not setup correctly the connection indicator at the bottom of the screen will reflect that the *Hardware not Connected*. *Failed to connect* and any attempt to *Verify Connection* will fail. Once the correct⁶ device is connected and the file to program selected, click *Verify Connection* and then *Program Device*.

⁶ When multiple devices are connected to the AEVM, ensure that for I²C that the address is that of the device to be programmed. In the case of SPI, make sure that the chip select is connected to the device to be programmed.



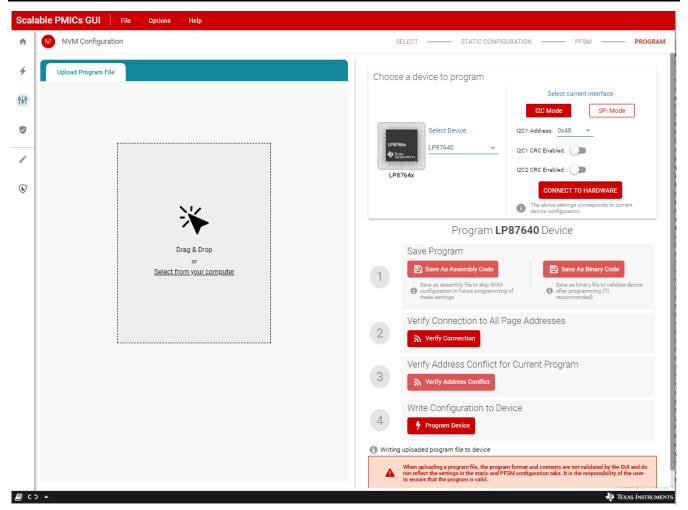


Figure 8-30. Program with an Existing Configuration

8.2.2 NVM Configuration Special Use Case: Changing the Communication Interface

The GUI tool writes the register settings using the identified interface and then uses the bulk programming method to transfer the register settings to the NVM. In the event that the NVM image uses a different interface, then it is important that the device being programmed supports both interfaces. When the GUI writes to the register settings to change the interface (SPI to I^2C or I^2C to SPI), the GUI will pause and display a prompt, see Figure 8-31, to change the hardware configuration to enable the new interface. This message specifically refers to the EVM, but can be generalized to any hardware configuration where changes are made to transition from I^2C to SPI or SPI to I^2C .



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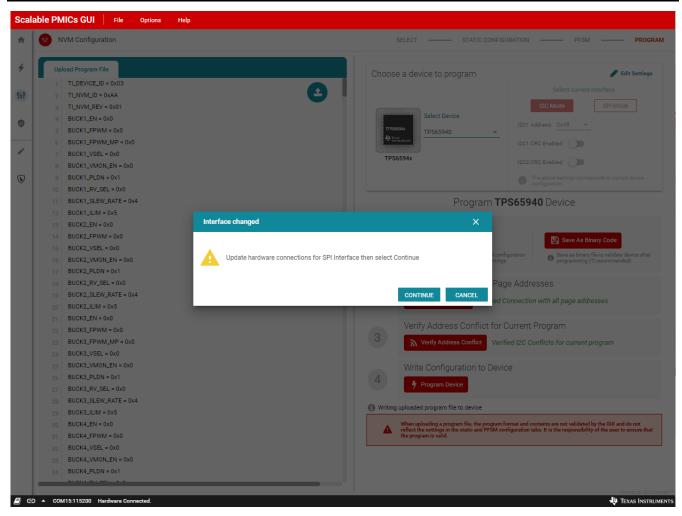


Figure 8-31. Interface Change during Programming

8.2.3 Lock Option During NVM Programming

The PMIC NVM can be permanently locked, preventing any changes to the NVM configuration. While this is not recommended during development, the feature is supported by the GUI. During the programming, a dialog window appears, see Figure 8-32, with the option to lock the NVM. Once this is done, then the PMIC NVM cannot be changed.



Scalab	IE PMICS GUI File Options	telp	
*	W NVM Configuration	SELECT STATIC CONF	FIGURATION PFSM PROGRAM
* †4†	Upload Program File 1 TI_DEVICE_ID = 0x03 2 TI_NVM_ID = 0xAA	Choose a device to program	Edit Settings
•	3 TI_NVM_REV = 0x01 4 BUCK1_EN = 0x0 5 BUCK1_FPWM = 0x0 6 BUCK1_FPWM_MP = 0x0	Select Device TP86594x De Device TPS65940	I2C Mode SPI Mode I2C1 Address: 0x48 v I2C1 CRC Enabled:
•	7 BUCK1_VSEL = 0x0 8 BUCK1_VM0N_EN = 0x0 9 BUCK1_PLDN = 0x1 10 BUCK1_RV_SEL = 0x0	TPS6594x	12C2 CRC Enabled:
	ID BUCK1_RV_SEL = 0x0 11 BUCK1_SLEW_RATE = 0x4 12 BUCK1_ILIM = 0x5 13 BUCK2_EN = 0x0 14 BUCK2_FPWM = 0x0	Do you wish to lock the device ?	ode Bave As Binary Code
	15 BUCK2_VSEL = 0x0 16 BUCK2_VMON_EN = 0x0 17 BUCK2_PLDN = 0x1 18 BUCK2_RV_SEL = 0x0	Cannot make changes to EEPROM settings on the programmed device once locked	kip NVM gramming Save as binary file to validate device after programming (Ti recommended)
	10 BUCK2_SLEW_RATE = 0x4 20 BUCK2_JLIM = 0x5 21 BUCK3_EN = 0x0 22 BUCK3_FPWM = 0x0	No Yes	Verified Connection with all page addresses flict for Current Program
	22 BUCK3_FPWM = 0x0 23 BUCK3_FPWM_MP = 0x0 24 BUCK3_VSEL = 0x0 25 BUCK3_VMON_EN = 0x0 26 BUCK3_PLDN = 0x1	3 الم Verify Address Confl 4 Write Configuration 4 Program Device	program
	27 BUCK3_RV_SEL = 0x0 28 BUCK3_SLEW_RATE = 0x4 29 BUCK3_ILIM = 0x5 30 BUCK4_EN = 0x0	Writing uploaded program file to dev	ice he program format and contents are not validated by tings in the static and PFSM configuration tabs. It is now that the program is valid.
	31 BUCK4_FPWM = 0x0 32 BUCK4_VSEL = 0x0 33 BUCK4_VMON_EN = 0x0 34 BUCK4_PLDN = 0x1	ute responsibility of the user to e	
ළ ල	COM15:115200 Hardware Connected.		🐺 Texas Instruments

Figure 8-32. NVM Lock Option

CAUTION

Locking a device is permanent.



9 NVM Validation Page

Note

Texas Instruments recommends as best practice to always use the NVM validation to confirm the correct configuration of the device following programming from the NVM Configuration page.

The NVM Validation page is used to download the current register or NVM settings to the host PC or compare the settings to a file from the host PC. One of the important aspects of this page is that the NVM settings are accessed by overwriting the current register settings. If the *NVM Settings* button is selected, as shown in Figure 9-1, when the *DOWNLOAD CONFIGURATION* button is selected, then the GUI immediately issues a set of commands to the PMIC to overwrite all existing register settings with the contents from NVM. This will overwrite any settings or configuration to the device made through the Quick-start or Register Map pages. After the overwrite is complete, then the register contents are read out through the communication interface.

Scala	able PMICs GUI	File	Options	Help	
+	NVM Validat	ion			Select Configuration to Read NVM Settings Current Settings
* + + + + + + + + - * *	Compare Configura			Drag & Drop or Select from your computer	Select Configuration 0 Real VM Settings Current Settings Select Configuration Save Configurations Select Configuration (Consequence) Image: Configuration (Consequence) Select Device Type Image: Configuration (Consequence) Select Device Type Select Device Type Select Device Select Device Select Device Device CRC Registers is recommended for downloading configuration of devices only, it is not recommended for device comparison to program files.
					DOWNLOAD CONFIGURATION
				COMPARE	DUVICUAL CONFIGURATION
<i>∎</i> ∈) ▲ COM15:115200 Ha	ardware Con	nected.		Per send by GAI Compare for 🖓 TEXAS INSTRUMENTS

Figure 9-1. NVM Validation

The top right of the page indicates which of the *Current Settings* or the *NVM Settings*, are being read. On the left side of the page is an interface to select a known file to compare the read contents to. This provides a quick visual pass/fail response to evaluate the content read. The *DOWNLOAD CONFIGURATION* option is found on the right side of the page.

Compare the Current or NVM Settings with an existing binary file

- 1. Confirm that the correct device is connected.
 - a. Select the correct Device Type.
 - b. Select the correct Communication Interface.
- 2. Select the binary file from the host PC to compare the device NVM with.



- a. Use the Drag and Drop feature or the file navigator.
- b. When a valid file is selected, the COMPARE button will become active.
- 3. Press the COMPARE button.

Download the Current or NVM Settings to a binary file.

- 1. Confirm that the correct device is connected.
 - a. Select the correct Device Type.
 - b. Select the correct Communication Interface.
- 2. Select the Current Settings or NVM Settings button
- 3. Press the DOWNLOAD CONFIGURATION button.



10 Watchdog Page

The Watchdog page is an interactive evaluation tool for exercising the watchdog functionality in both TRIGGER and Q&A modes. This tool uses the MSP432E microcontroller on the AEVM to create the watchdog stimulus for both correct and incorrect use cases. Status monitoring is provided to show the PMIC response.

Scal	Iable PMICs GUI File Option	ons Help									
ŧ	Watchdog				٥	Mode I2C	Addr 12C CRC 0x48 ×	► ST/	ART SEQUENCE		
4	CONFIGURATION			Edit Enable					STATUS MONITORING		
¢Ļ¢	Window Configurations Window-1	Reset Threshold	Threshold Configurations					Error Count			
٢		74 ms 7	ENABLE DRV					ERROR STATUS			
/	Window-2	74 ms	POWER H	DLD				Timeout	Ç		
	Long Window	ENABL	RETURN T	O LONG	WINDOW			Reset	Q		
$\overline{\mathbf{b}}$	•	803250 ms						Fail	Q		
									Long Window Tim	eout C	
	WATCHDOG SEQUENCE			Window 1 4 Correct answer		Window - 0 Incor	2 rect answer		Answer Error	C	
	Question		Answer					0	Answer Early	S	
	MCU reads question	MCU reads answer					Sequence Error	õ			
	Read register WD_QUESTION I2C2/SPI ANSW_CNT	Write to Write to Write to Write to	Wite to WD_ANSWER_REG ANSW_CNT	Wite to Wite t			Write to		STATUS		
	I2C2/SPI ANSW_CNT I Commands	ÄNSW_CNT ÄNSW_CNT	ANSW_CNT		L	ANSW_CNT		WD FIRST OK			
									Bad Event		
		WINDOW 1			W	INDOW	2				
						Uns	afe Window Time ()			
E G	COM15:115200 Hardware Connected.									Powered By GUI Composer Devered By GUI Composer	

Figure 10-1. Watchdog Page

To exercise the watchdog module please make sure the following conditions are met in the PMIC:

- 1. The device supports the watchdog feature
- 2. The PMIC is in a mission state. A hardware state, like **SAFE RECOVERY**, will prevent the watchdog from operating.
- 3. NRSTOUT (found in the register MISC_CTRL) must be 1
- 4. WD_EN (register WD_THR_CFG) must be 1
- 5. If applicable to the device, any GPIO configured as DISABLE_WDOG should be logic low
- 6. WD_PWRHOLD must be 0
- 7. For evaluation purposes it is recommended to set WD_RST_EN to 0 so that the device does not enter *WARM RESET* during the evaluation.

Trigger Mode

The watchdog page will reflect the settings in the controls section. In order to change from QA to *TRIGGER* mode, the *Edit/Enable* indicator, as highlighted in yellow in Figure 10-1, should be switched to *Enable*. Once in the trigger mode, switch back to *Edit*, and adjust the default *Window-1* and *Window-2* values to a time frame that does not exceed the limits of the AEVM.

With valid timing windows, the watchdog can be re-enabled and the watchdog sequence started.

Start Sequence:

- 1. Enable the watchdog, select 'Enable'
- 2. Select the mode, 'TRIGGER' or 'Q&A'
- 3. Edit the AEVM trigger waveform, select 'Edit'



- 4. Adjust 'Window-1' and 'Window-2'
- 5. Select the 'Sequence Configuration'
- 6. Enable the watchdog, select 'Enable'
- 7. Select 'START SEQUENCE'

In the EVENT STATUS view, the WD FIRST OK is illuminated and green, see Figure 10-2, indicating that the first watchdog trigger sequence was received correctly. The PMIC is continuously polled during operation and the ERROR STATUS view is updated.

Scal	able PMICs GUI File O	ptions Help								
÷	Watchdog					٥	Mode 12C	Addr I2C CRC 0x48 X	STOP SEQUENCE	TRIGGER Q&A
4	CONFIGURATION			🕄 Disabl	e Watchdog to update Con	figurations	Ed	it Enable	STATUS MONITORING	
ŶĻŶ			Threshold Configurations Controls Deset Threshold Configurations ENABLE DRV					Error Count		
۲		13 ms			ENABLE DRV				ERROR STATUS	Clear All
_		12 ms			D POWER	HOLD			Early Trigger	C
		12 ms	ENABLE RESET			TO LONG	WINDOW		Timeout	0
۲		803250 ms							Reset	0
	MSP432 supports maximum win								Fail	0
	WATCHDOG SEQUENCE		Se	equence Configuration: Correc		Preset	Mode 🕻	Advanced Mod	e Long Window Timeou	. <i>C</i>
									EVENT STATUS	
	Watchdog-Trigger on GPIO pin				1				WD FIRST OK	
	Internally Generated	ter,an		ter, en		ton, or	-		Bad Event	
	Watchdog Windows	Long Window	Window 1(Bad Event)	Window 2(Good Event)	Window 1(Bad Event)	Wind	dow 2			
			~	Watchdog Trigger Sequenc	e Started Successfully	×				
							Uns	afe Window Time 🕻)	
										Powered By GUI Composer**
	COM15:115200 Hardware Connecte	ed.								🐺 Texas Instruments

Figure 10-2. Watchdog Trigger Mode

To stop the evaluation, first use the control to set the RETURN TO LONGWINDOW, second switch from *Enable* to *Edit* mode, and then click *STOP SEQUENCE*.

Stop Sequence:

- 1. Select RETURN TO LONGWINDOW
- 2. Select Edit
- 3. Select STOP SEQUENCE

The sequence configuration can be modified to intentionally provide an incorrect sequence, using the drop down menu 'Sequence Configuration'. The incorrect timing and the consequent bad event is shown in Figure 10-3. To evaluate this configuration, first, switch from *Edit* to *Enable* mode, second, disable the *RETURN TO LONGWINDOW*, and then click *START SEQUENCE*.



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	ble PMICs GUI File Opt	tions Help									
÷	Watchdog					٥	Mode 12C	Addr 12C CRC 0x48 X	STOP SEQUENC	E	Q&A
4	CONFIGURATION			1 Disa	able Watchdog to update Conf	figurations	Edit	Enable	STATUS MONITORIN	G	
ŶĻŶ			Controls	DRV		Error Count 15					
•		13 ms Window-2 Pall Threshold 7 POWER HOLD						ERROR STATUS Early Trigger		Clear All	
6	12 ms ENABLE RESET ENABLE RESET ENABLE RESET ENABLE RESET							TimeoutReset		C2 C2	
	MSP432 supports maximum wind								• Fail		C
	WATCHDOG SEQUENCE		S	equence Configuration: Wat		Preset	Mode 🚺	Advanced Mo	de Long Window	v Timeout	Q
									EVENT STATUS		
	Watchdog-Trigger on GPIO pin			4 → 1	L	1	H-+	L	WD FIRST OF	(
	Internally Generated Triggered Pulse	Longon	1	to an			las, en		Bad Event		
	Watchdog Windows	Long Window	Window 1(Bad Event)	Window 2(Good Event)	Window 1(Bad Event)	Window	1(Bad Event)			
R. CO	COM15:115200 Hardware Connected						Unsa 🖉	fe Window Time (D		red By GUI Composer"'' AS INSTRUMENTS

Figure 10-3. Invalid Trigger Watchdog Input

The errors can be cleared using the icons to the right of each error, or by clicking Clear All.

Q&A Mode

As previously stated, the Q&A mode can be selected when the *Edit/Enable* indicator is moved to *Enable*.



Scal	able PMICs	GUI File Opt	tions Help											
÷	0	Watchdog					٥	Mode I2C	Addr 0x48	I2C CRC ×	► ST	TART SEQUENCE		
4	CONFIGUE	RATION						E	dit	Enable	STATUS MONITORING			
ŶĻŶ	Window-1			Threshold Configurations Reset Threshold 0		Controls					Error Count			
۲	Window-2		1 ms	Fail Threshold		POWER HOL	D					R STATUS	Clear All	
/				0	0					0	Timeout	Q		
0	Long Wine	dow		ENABLE RESET		RETURN TO	_ONGWIN	IDOW			0	Reset	Q	
•	-		105 ms								0	Fail	0	
												Long Window Timeout	C	
											0	Answer Error	C	
	WATCHDOO	G SEQUENCE		Window 1 Window 2 4 Correct answer v 0 Incorrect answer				ver -	0	Answer Early	Q			
		Question		Answer								Sequence Error	Q	
		MCU reads question	MCU reads an	swer							EVENT STATUS			
		Read register	Write to	Write to G WD_ANSWER_REG	Write to WD_ANSWER_REG	Write to WD_ANSWER_REG						WD FIRST OK		
	I2C2/SPI Commands	ANSW_CNT	ANSW_CNT	ĀNSW_CNT ĀNSW_CNT		ANSW_CNT				CNT		Bad Event		
			1											
			WI	NDOW 1	WINDOW 2									
					🔳 Unsafe Window Time					ow Time (
													Powered By GUI Composer**	
/ с	> ^												🔱 Texas Instruments	

Figure 10-4. Watchdog Q&A

Once the Window configuration is updated for the Q&A a similar process can be employed to evaluate the Q&A mode. Figure 10-5 shows a correct sequence of answers to the questions while Figure 10-6 shows an incorrect answer.

Watchdog	1				Mode 120		STOP SEQUENCE TRIGGER	Q&A
ODNFIGURATION Conductions to update Configurations to the Configuration to the Configur								
					Controls		Error Count	
		20 ms			ENABLE DRV		ERROR STATUS	Clear
					Dever Hold		Timeout	
		20 ms			RETURN TO LONGWINDOW		Reset	
		803250 ms					0 Fail	;
							Long Window Timeout	ć
							Answer Error	ź
ATCHDOG SEQUE	NCE						Answer Early	ć
	Question			Answer			Sequence Error	í
	quotatin			7.1101/01			EVENT STATUS	
	MCU reads question	MCU reads an	swer				WD FIRST OK	
I2C2/SPI Commands	Read register	Write to WD_ANSWER_RE ANSW_CNT	Write to G WD_ANSWER_REG ANSW_CNT	Write to WD_ANSWER_REG ANSW_CNT		ite to WER_REG N_CNT	Bad Event	
	1 1 1 1	WI	JDOW 1	Vistchdog Q & A Sequence Started Successfully.	- × WINDOW 2			
						nsafe Window Time 🛈		

Figure 10-5. Watchdog Q&A Valid Response



Watchdog					Mode Addr I2C CRC I2C 0x48 X	STOP SEQUENCE	TRIGGER
CONFIGURATION			🕄 Disable W	Vatchdog to update Configu	rations Edit Enable	STATUS MONITORING	
			Controls			Error Count 15	
	20 ms		ENABLE DRV			I D	
			POWER HOLD			Timeout	
	20 ms		RETURN TO LONGWINDO	w		Reset	
	803250 ms					• Fail	
						Long Window Time	eout
						Answer Error	
						Answer Early	
						Sequence Error	
VATCHDOG SEQUENCE						EVENT STATUS	
						WD FIRST OK	
						Bad Event	
		Vatchdog Q & A Sequence Started Successfully	V		Unsafe Window Time ()		

Figure 10-6. Watchdog Q&A Invalid Response



11 Additional Resources

- 1. SimpleLink[™] Ethernet MSP432E401Y MCU Launchpad[™] Development Kit
- 2. GUI Composer User's Guide.
- 3. E2E Support Forum.

12 Appendix A: Troubleshooting

12.1 Hardware Platform Not Recognized

Scal	able PMICs GUI File Options Help			
ń	Guick-start			
۲				
¢∔¢				
0	Configure and Monitor all your	Device Settings 1 Configure Serial Port Settings 2	×	
1	Devices Settings	Select Port :	▼ Select Baud Rate : 9600 (Recommended) ▼	
S	Tree Treasure in the second se	TPS5594x-1.0 TPS5594x-1.0 I2C1 Addr Device Status: Disconnected •		ng USB Port to get started
P c	Mode Addr. I2C CRC WD CRC I2C 0x48 I2C CRC WD CRC X I2C I2C CRC WD CRC I2C CRC X I2C I2C CRC WD CRC I2C CRC I2C CRC X I2C CRC I2C CRC I2C CRC I2C CRC I2C CRC X I2C CRC I2C CRC I2C CRC I2C CRC I2C CRC X I2C CRC	to your computer's USB port and click the Connec	12C2 CRC Enabled:	TEXAS INSTRUMENTS

Figure 12-1. Hardware Platform Error

The GUI will automatically connect to the AEVM (micro controller with the analog evm controller firmware) and then to the PMIC. Typically, if the GUI cannot find the hardware platform this is due to either a faulty USB connection or the GUI is attempting to connect to the wrong communication (COM) port. The hardware platform will enumerate as three devices; two CDC classes and one DFU class. From another program, like the device manager in windows, the user can verify which COM port is the ACCtrl and which is the ACCtrl Console. From the GUI option, the user should select the COM port number of the ACCtrl and **not** the ACCtrl Console. The AEVM supports a baud rate of 115200.

Other devices connected to the PC, may also enumerate at CDC class devices and the GUI may attempt to communicate with these devices. If no response is made from the device, then it is possible that the GUI will not attempt to connect to other devices until the current device responds.

Only one AEVM should be connected to a host (MAC of PC) at one time. The GUI does not support the ability to handle and respond to multiple AEVM devices connected to the host.



12.2 PMIC Device not found

Sca	Scalable PMICs GUI File Options Help									
ń	Quick-start									
•										
ήĻή										
0	Configure and Monitor all your Devices Settings	Device Settings ×								
-		Select Port : COM15 (Texas Instruments, Inc.) Select Baud Rate : 9600 (Recommended) 2) Choose Connected Device Type 3 Configure interface settings								
¢	TTPS504x ++ 40 2 ↓ Research	Select Device Select current interface I2C MODE ng USB Port to get started TPS6594x-1.0 I2C1 Address: 0x48 Device Status: Disconnected I								
	Device Settings	IZC2 CRC Enabled:								
(Mode Addr IZC CRC WD CR IZC 0:43 X X	CONNECT TO HARDWARE								
<i>_</i> c	> Mardware not Connected. Failed to connect.		🐙 Texas Instruments							



If the hardware platform is connected but the PMIC device is not found, then the GUI will report an error regarding the address: *Connected to AEVM Controller, but failed to connect to device TPS6594x_external on I2C @xx*. In the case of I²C this means that the address was not acknowledged (NACKed). Perform appropriate I²C bus checks: appropriate pull-up resistors, verify that no device is holding the clock low (clock-stretching), and so forth. Verify that the correct I²C address is being sent. The default address which the GUI uses may not be correct and it is necessary to update the address using the *Device Settings* below the *Options* tab.

Similarly with SPI, ensure that the hardware connection is correct and that the chip select is connected to the appropriate PMIC when multiple PMICs are in use.

13 Appendix B: Advanced Topics 13.1 Scripting Window

Scripting is a convenient way to send a sequence of commands (reads or writes) to the PMIC device registers as opposed to the individual commands associated with an update to a parameter in either the quick-start or Register page views. *Scripting* is found below the Options tab located at the top of the GUI. Opening the scripting window will open a new window while the GUI window will still be active as shown in the following paragraph.

pp_sc	riptjs	✓ ± ± = ► = ⊙ ○ #
1	/**	
2	* TODO: Additional scripts can be added to the 'scripts' folder.	
з	•	
4	* To view the scripting widget properties in the Designer's Property editor, select the ti-widget-scripting widget	
5	* in the TREE view. You can then modify the 'script-dir' property if you would like to	
6	* change which folder the scripts are stored in, and can make additional scripts available to the user by	
7	* adding them to the comma-separated list of script file names in the 'scripts' property.	
8	*/	
9		
10	/**	
11	* Entry point for the script, which will be executed when the user presses the PLAY button in the Scripting Dialog.	
12	*/	
13	function main() {	
14	/* TODO: application-specific script commands go here */	
15 16	//let acc_en = read('acc_en'); //write('acc_en', acc en == 8x6? 0x80; 0x86);	
10	//write(acc_en , acc_en == exet r exee : exet ;	
17	1	

Figure 13-1. Default Scripting Window

Figure 13-1 shows the initial scripting window and the default text provided. This file can be edited to provide a desired sequence of commands. One quick way to start using the scripting window is to use the record feature to capture a sequence of commands. In the upper right hand corner is the record icon. Hovering the cursor over the icon will reveal a *Start Recording* help box. In the example shown in Figure 13-2 and Figure 13-3, the recording is started and then when returning to the GUI window the Register Page is used to read DEV_REV and NVM_CODE_2 and then write to the BUCK1_CTRL register. Once these sequence of actions are completed, then returning to the scripting window will reveal the recorded commands. At this point, the recording can be stopped and these commands can be expanded and repeated for the various registers. Once the sequence is complete, then click the *Run* icon to execute the sequence.

Scal	able PMICs GUI File Options Help												
ŧ	Mode Addr I2C CRC WD CRC I2C 0x48 X X												
4	Register Map			Auto Re	ed Off		~	READ	REGISTER	READ AL	L REGISTE	ERS	white recession white ALL recossions Immediate Write 🗸
<i>,</i>	Q Search Registers by name or address (0x)							_	ch Bitfield	ds 🔽 S	Show Bite	ts	
ęΫ	Register Name	Address	Value	7	6	5	8 4	ts 3	2	1	0	Î	BUCK1_CTRL
۲	▼ User Registers - Page 0 DEV_REV	0x01	0x03	0	0	0	0	0	0	1	1		PFM and PWM operation (AUTO mode).
	NVM_CODE_1	0x02	0xAA	1	0	1	0	1	0	1	0		User Registers - Page 0 / BUCK1_CTRL /
-	NVM_CODE_2 BUCK1_CTRL	0x03 0x04	0x01 0x29	0	0	0	0	0	0	0	1		BUCK1_FPWM_MP[2] BUCK1_FPWM_MP
	BUCK1_CONF	0x05	0x2C	0	0	1	0	1	1	0	0		Automatic phase adding and shedding. \checkmark
D	BUCK2_CTRL BUCK2_CONF	0x06 0x07	0x20 0x2C	0	0	1 1	0	0	0	0	0		User Registers - Page 0 / BUCK1_CTRL / BUCK1_VMON_EN[4] Present for GUI Common
/ G	D ▲ COM15:9600 Hardware Connected.												BUCK1_VMON_EN[4] Powered By GUI Compde TEXAS INSTRUMEN

Figure 13-2. Scripting, Recording Register Read and Writes



Scripting - Sc	alable PM	ICs Gl	File						
	er] recorded [11/4/2020, 11:22:09 AM]								
3 read(main() { 'DEV_REV'); 'NVM_CODE_2' ('BUCK1_CTRL								
Logs					Ø	×			
Wed Nov 04 2020	11:23:11	0	write(BUCK1_CTRL, 41) => void						
Wed Nov 04 2020	11:23:10	0	read(NVM_CODE_2) => 1						
Wed Nov 04 2020	11:23:09	0	read(DEV_REV) => 3						

Figure 13-3. Scripting, Running a recorded sequence



14 Appendix C: Known Limitations

This section contains known limitations of the GUI. Please use the support forums to report any issues or limitations found that are not on the following list.

Number	Description	Workaround
1	CRC_15 and CRC_16 are included for comparison of NVM Validation but these registers cannot be edited	None. The GUI will report that the NVM files do not match. Inspect the registers and disregard errors associated with CRC_15 and CRC_16, registers 0x00FE and 0x00FF respectively.
2	Modifying Device Type and its configuration (for example, Master/Slave, Phase Configuration etc) is not recommended after creating PFSM as it may not produce expected results	In the case of modifying the phase configuration, remove all references in the PFSM before attempting to change the phase configuration. Changing the device type will require starting from a new or blank template.
3	SPI Hardware connection status displayed in the status bar can be detected incorrectly.	Use the register map page to confirm that values other than 0x00 and 0xFF can be read from the device.
4	The GUI does not provide control for multiple SPI Chip Select outputs.	None. In multi-device SPI configurations the Chip Select signal from the AEVM would need to be manually moved to each PMIC individually.
5	USB Connections issues with COM ports associated with Bluetooth devices.	Disable or remove devices which enumerate as COM ports on the host pc.
6	Enumeration (connecting the USB cable to the AEVM) will attempt to connect to the device with the previous or default settings and may fail to connect.	Use the Device Settings and click the <i>Connect to Hardware</i> to update the GUI to the correct connection settings.

Table	14-1.	GUI	Limitations
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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cł	nanges from Revision * (December 2019) to Revision A (November 2020)	Page
•	Updated for release v2.0.0 throughout entire document	3

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