Programmer's Guide

TPS65219 NVM Programming Guide

ABSTRACT

The TPS65219 family of power management integrated circuits (PMICs) includes a configurable non-volatile memory (NVM) space. This programmer's guide details the step by step instructions to define the PMIC default configuration and how to reprogram the NVM.

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1 Introduction

The configuration process described in this document writes to the NVM space and is intended to be used in a production line or prototype board. This mechanism is not intended to be used in final applications because the process impacts the regulator outputs and the function of digital pins. The TPS6521905 is an orderable part number, part of the TPS65219 family, created specifically to support custom NVM configuration. Table 1-1 shows the user-programmable variants and the supported package size, temperature, and switching mode. Figure 1-1 describes the supply options for pre-configured and custom NVMs based on volume. Design resources are available not only for pre-configured and high volume NVMs, but also for low volume custom NVMs. These resources can include application notes, user's guides, technical reference manuals, and NVM configuration files ready to be loaded into the PMIC NVM. Visit the TPS6521905 product page on ti.com or use our PMIC E2E forum to ask about available resources.

Note

To support NVM programming, TI offers two socketed EVMs, one for each package size. **TPS65219EVM-SKT** is the orderable part number for the 5x5 socketed EVM and **TPS65219EVM-RSM** is the orderable part number for the 4x4 socketed EVM.

Table 1-1. TPS65219 User-Programmable variants

OPN	Package	Temperature	Switching Frequency Supported
TPS6521905RHBR	RHB - 5x5 (0.5mm pitch)	Ta = -40C to 105C Tj = -40C to 125C	Quasi-Fixed Frequency (auto-PFM and forced-PWM)
TPS6521905RSMR	RSM - 4x4 (0.4mm pitch)	Ta = -40C to 105C Tj = -40C to 125C	Quasi-Fixed Frequency (auto-PFM and forced-PWM)
TPS6521905WRHBRQ1	RHB - 5x5 (0.5mm pitch) Wettable Flank	Ta = -40C to 125C Tj = -40C to 150C	Quasi-Fixed Frequency (auto-PFM and forced-PWM)
Available Upon Request	RHB - 5x5 (0.5mm pitch) Wettable Flank	Ta = -40C to 125C Tj = -40C to 150C	Fixed Frequency (recommended for applications that require best EMI control. Spread spectrum and out-of-phase switching are available)

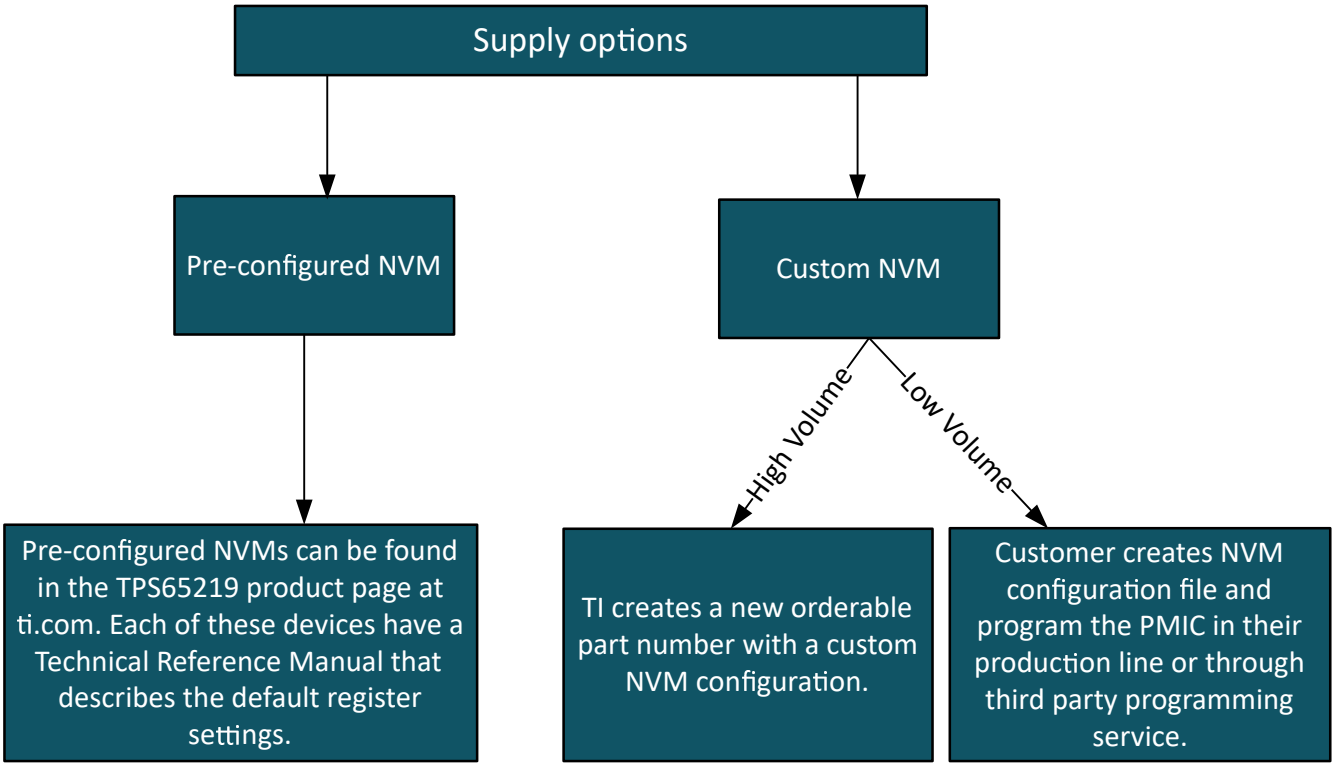

Figure 1-1. Supply Options

2 Hardware Requirements for NVM Programming

The PMIC has two memory spaces, the register map space and the NVM space. Re-programming the NVM is done by first writing to the register map through the serial interface (I2C) and then saving the register settings into the NVM. Because the configuration first involves writing to the register map, which controls the regulator and digital pins, there must be no dependency or need to use the PMIC resources. For example, an external power supply must be used to supply the pull-up resistors of the I2C pins instead of using one of the PMIC power resources while reprogramming the NVM. Table 2-1 and Figure 2-1 show the minimum hardware requirements for the hardware setup between the PMIC and the programming device.

Note

Other external components like inductors, capacitors, and so on are not needed to re-program the NVM in Initialize state. However, those components are needed for the PMIC operation in Active state and to validate NVM settings.

Table 2-1. Minimum Hardware Requirements for NVM Programming

Device pin	Required Connections
VSYS	VSYS voltage must be 3.3V or higher without exceeding the maximum recommended voltage in the spec.
	VSYS must have a minimum of 2.2uF capacitance.
VDD1P8	VDD1P8 must have a 2.2uF capacitance
I2C pins	Pull-up resistors on I2C pins (SDA/SCL) must be supplied by external 3.3V supply.
	I2C pins of the PMIC must be driven by an external I2C device that can communicate with the PMIC and write to the registers.
EN/PB/VSENSE	EN/PB/VSENSE pin must be connected to VSYS with a pull-up resistor.
AGND	AGND (pin# 15) must be connected to the PCB ground planes through a VIA . Keep the trace from the AGDN pin to the VIA short.
Thermal Pad	The package thermal pad must be connected to the PCB ground plane with a minimum of nine VIAS.

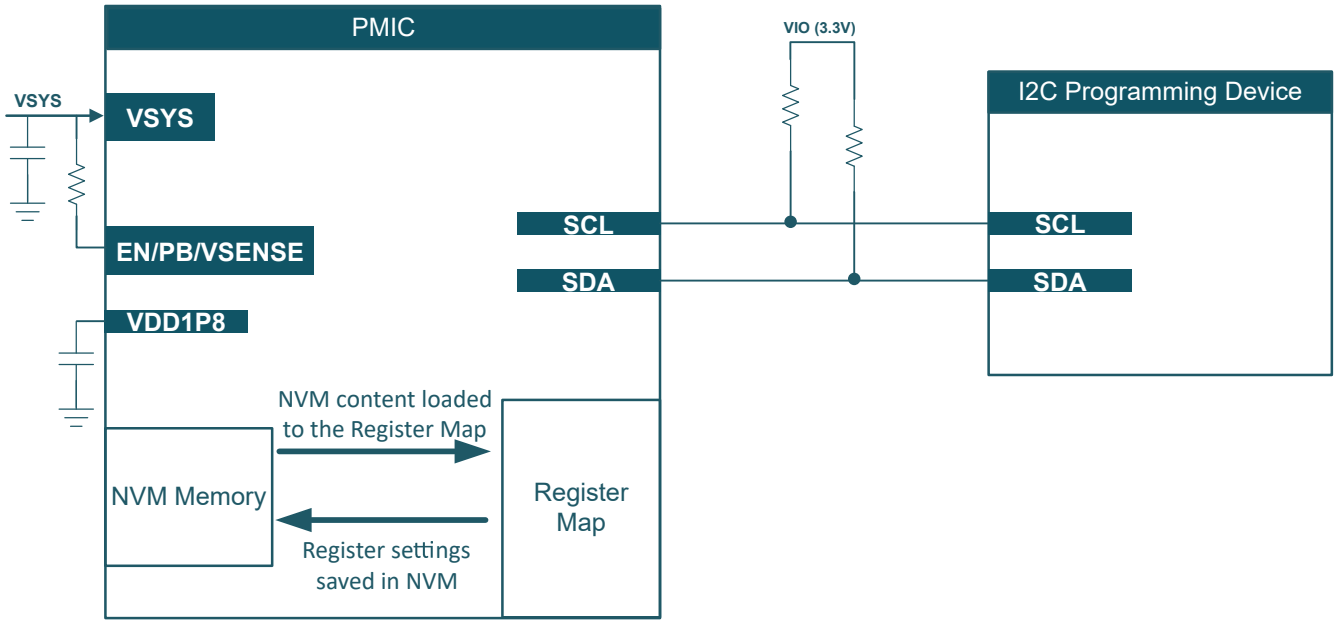

Figure 2-1. Hardware Setup for NVM Programming

3 Typical NVM Flow

This section describes the typical NVM definition flow which consists of the following steps: System requirements, Hardware setup, NVM programming and Test/Validation.

1. **System Requirements**

   Identify the system requirements and build a power distribution network (PDN). Voltage/Current, power-up/power-down sequence, low power modes, and load transient are typical requirements from processors, SoCs and peripherals.

2. **Hardware Setup**

   The TPS65219 can be programmed using the PMIC socketed EVM, a customer prototype board (in-circuit programming), or production line.

   - **Socketed EVM**: The PMIC socketed EVM comes with an onboard MSP340 that can communicate with the PMIC through I2C to re-program the NVM memory. This hardware also integrates a discrete 3.3V LDO that can supply the I2C pull-up resistors while the PMIC rails are OFF in Initialize state.

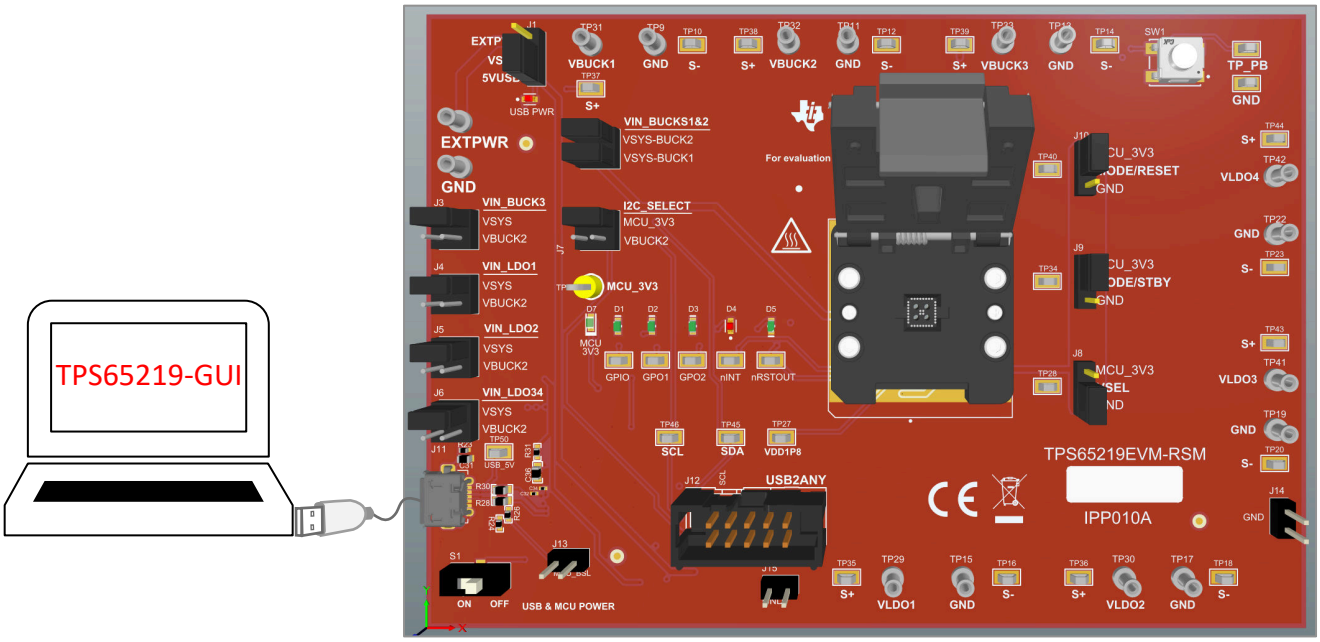

Figure 3-1. Socketed EVM

   - **Prototype board**: The user-programmable TPS6521*905* NVM comes with all the power resources inactive by default and the EN/PB/VSENSE pin configured as push-button with without FSD (PU_ON_FSD = 0x0). If this pin is pulled up to VSYS, PMIC stays OFF (Initialize state) when a valid supply is connected to VSYS. This configuration allows the reprogramming of the NVM before the power-up sequence is executed. Figure 3-2 shows what customers need to include in the prototype board to re-program the PMIC NVM. The components required include three test points on GND, SCL, SDA, and a 1x3 single row header connector that selects the pull-up supply between the external 3.3V and the PMIC rail that supplies the I2C pins in the normal application. The USB2ANY (available at ti.com) can be used to communicate with the PMIC and re-program the NVM settings.

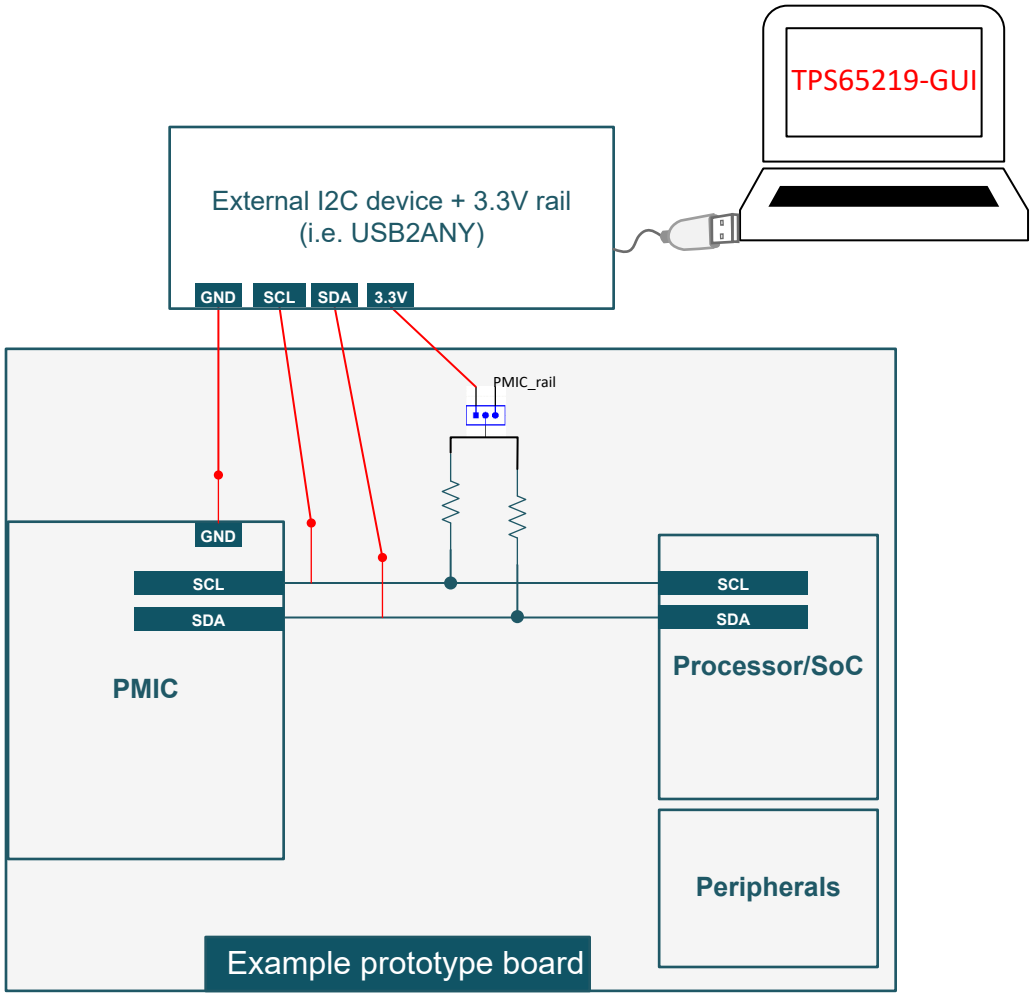

Figure 3-2. Prototype Example

Note

See section "Specifications" and "Detailed Design Procedure" in the data sheet for information about recommended external components like inductors, output capacitance, and so on.

- **Production line**: PMIC NVM can also be re-programmed in a production line following the Figure 2-1 before soldering the device into the final PCB.

3. **NVM Programming**

   Follow the programming instructions in Section 4 to change the register settings and save the new values into the NVM memory. The TPS65219-GUI can be used with the socketed EVM (or a prototype board plus an external USB2ANY). Alternatively, customers can use their preferred I2C debugger tool to write to each of the NVM registers without using the TPS65219-GUI. Once the NVM is re-programmed, it is recommended to perform a power cycle to confirm the new register settings were saved into the NVM memory.

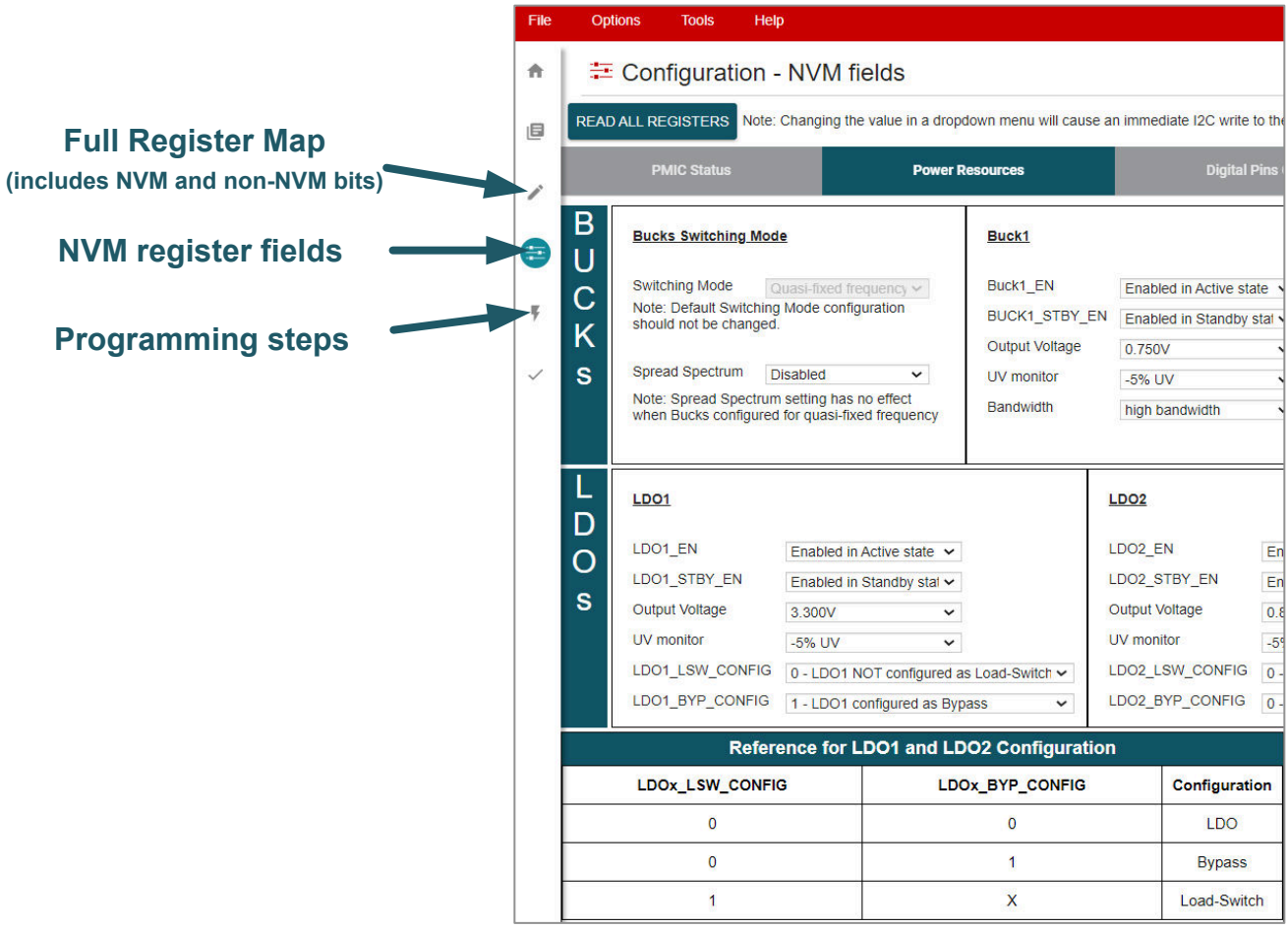

Figure 3-3. TPS65219-GUI

4. **NVM Testing**

   NVM settings must be tested to confirm expected PMIC behavior. The list below shows the minimum recommended tests. These tests can be performed in the socketed EVM or prototype board. If the socketed EVM was used to re-program the PMIC, the devices can be soldered down into the customer prototype board to test and validate system level functionality. Alternatively, the PMIC on the soldered down TPS65219EVM can be replaced to test a custom NVM configuration.

   - Measure all output voltages
   - Collect scope waveform for power-up sequence (include GPIOs if enabled and nRSTOUT)
   - Collect scope waveform for power-down sequence (include GPIOs if enabled and nRSTOUT)
   - Test EN/PB/VSENSE pin function and polarity to trigger ON and OFF request.
   - Test each multi-function pin (VSEL, MODE/STBY, MODE/RESET) configuration and polarity. Pull this pin high or low and verify if PMIC behavior changes according to the configured pin function.

   Note

   The socketed EVM can be used for re-programming and basic tests (For example: measuring output voltages, colleting power-up sequence waveforms, and so on) but must not be used to test specific performance parameters like load transient and efficiency because the socket pogo pins and layout placement introduce higher parasitic that do not represent the design of a real application.

4 Programming Instructions

This section describes the steps required to program the PMIC NVM. The programming process consists of two primarily steps; changing the register settings and saving the new values into the NVM memory. TI recommends programming the NVM in Initialize state, where VSYS is supplied but all of the PMIC outputs and monitors are OFF.

Figure 4-1 shows the steps to reprogram the device. The first command consists of an I2C OFF request to send the device to Initialize state. This command is only needed if the device is not in Initialize state. The second I2C command enables an internal oscillator for I2C communication and disables the rails discharge. The third step requires updating register settings to match specific application requirements following the programming instructions. After the register settings are updated, the new values can be saved into the NVM by writing 0x0A to register address 0x34. The last step "Validation" is optional and consists of an I2C command that compares register settings with NVM content.

Note

The first I2C command (I2C OFF request) is only needed if the PMIC is not in Initialize state. The user programmable OPN TPS6521905 comes with the EN/PB/VSENSE pin configured as "push-button" with the FSD feature disabled by default. When configured as PB, the device detects an ON-request when the pin is pulled low. If this pin has a pull-up to VSYS, then PMIC stays in Initialize state after VSYS is supplied. To verify if I2C communication is available in Initialize state, it is recommended to read the NVM ID register on address 0x01. The read back matches the two digits after the "TPS65219" in the part number. For example, when using TPS6521905, register 0x01 reads *05*.

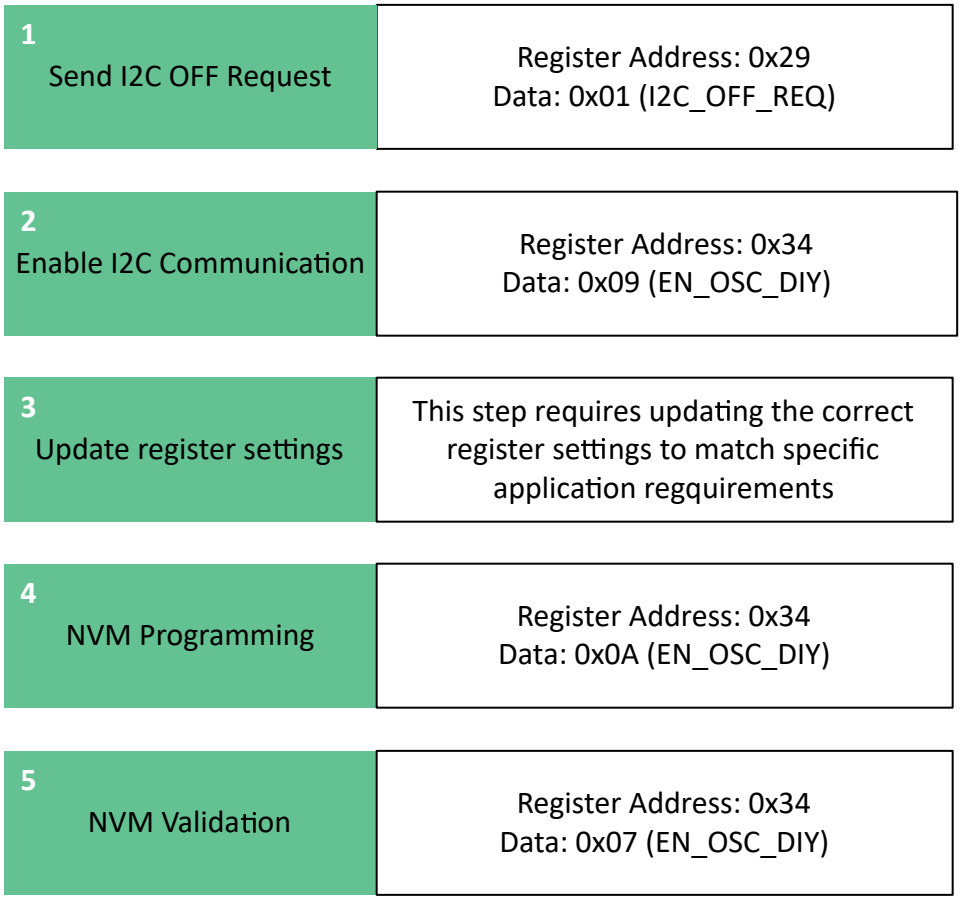

Figure 4-1. NVM Programming

4.1 Configuring Enable Settings

The PMIC has an Active and Standby state where rails can be enabled or disabled. The state change can be triggered by the MODE/STBY pin when configured as STBY.

- Figure 4-2 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-1 show the register fields to be written when NOT using the TPS65219-GUI.

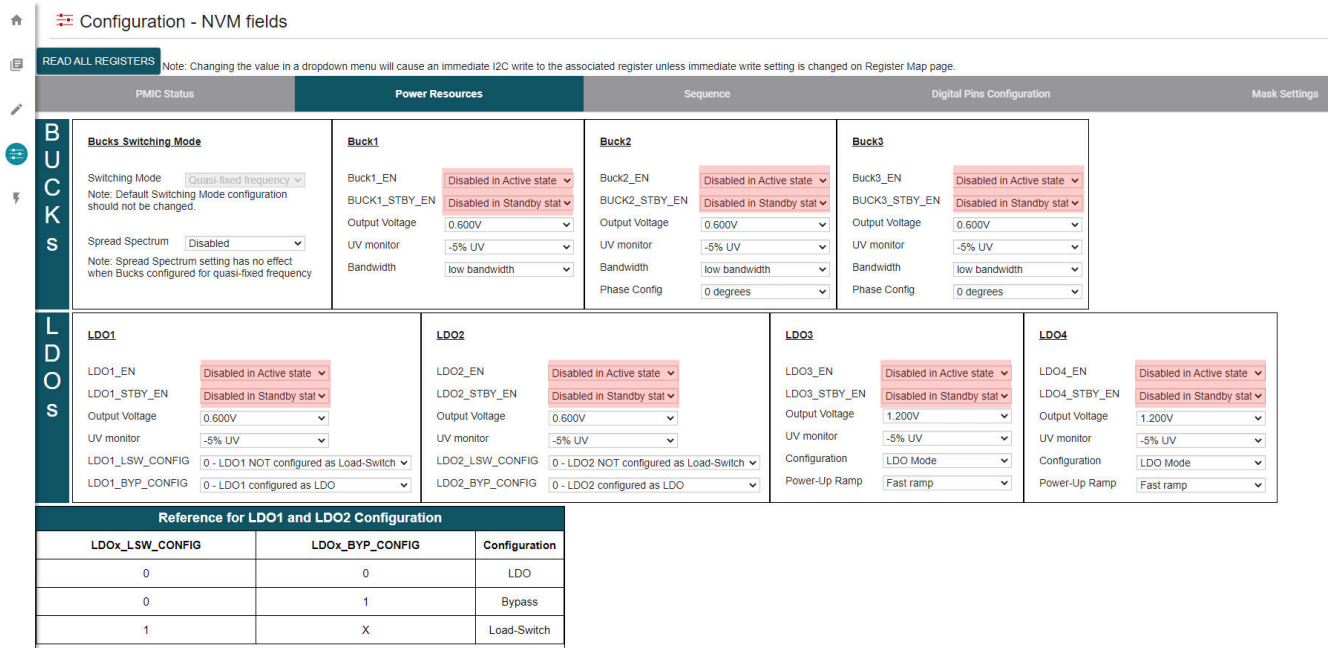

Figure 4-2. Enable Settings Using the TPS65219-GUI

Table 4-1. NVM Registers for Enable Settings

	Register Address	Bit		Settings
		Bit #	Field Name	
Enable rails in Active state	0x02	6	LDO4_EN	0h = Disabled 1h = Enabled
		5	LDO3_EN	0h = Disabled 1h = Enabled
		4	LDO2_EN	0h = Disabled 1h = Enabled
		3	LDO1_EN	0h = Disabled 1h = Enabled
		2	BUCK3_EN	0h = Disabled 1h = Enabled
		1	BUCK2_EN	0h = Disabled 1h = Enabled
		0	BUCK1_EN	0h = Disabled 1h = Enabled

Table 4-1. NVM Registers for Enable Settings (continued)

	Register Address	Bit		Settings
		Bit #	Field Name	
Enable rails in Standby state	0x21	6	LDO4_STBY_EN	0h = Disabled 1h = Enabled
		5	LDO3_STBY_EN	0h = Disabled 1h = Enabled
		4	LDO2_STBY_EN	0h = Disabled 1h = Enabled
		3	LDO1_STBY_EN	0h = Disabled 1h = Enabled
		2	BUCK3_STBY_EN	0h = Disabled 1h = Enabled
		1	BUCK2_STBY_EN	0h = Disabled 1h = Enabled
		0	BUCK1_STBY_EN	0h = Disabled 1h = Enabled

4.2 Configuring the Bucks

There are several settings that can be programmed for the Buck converters. These include the output voltages, under voltage (UV) monitoring, and bandwidth among others.

- Figure 4-3 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-2, Table 4-3, Table 4-4 and Table 4-5 show the register fields to be written when NOT using the TPS65219-GUI.

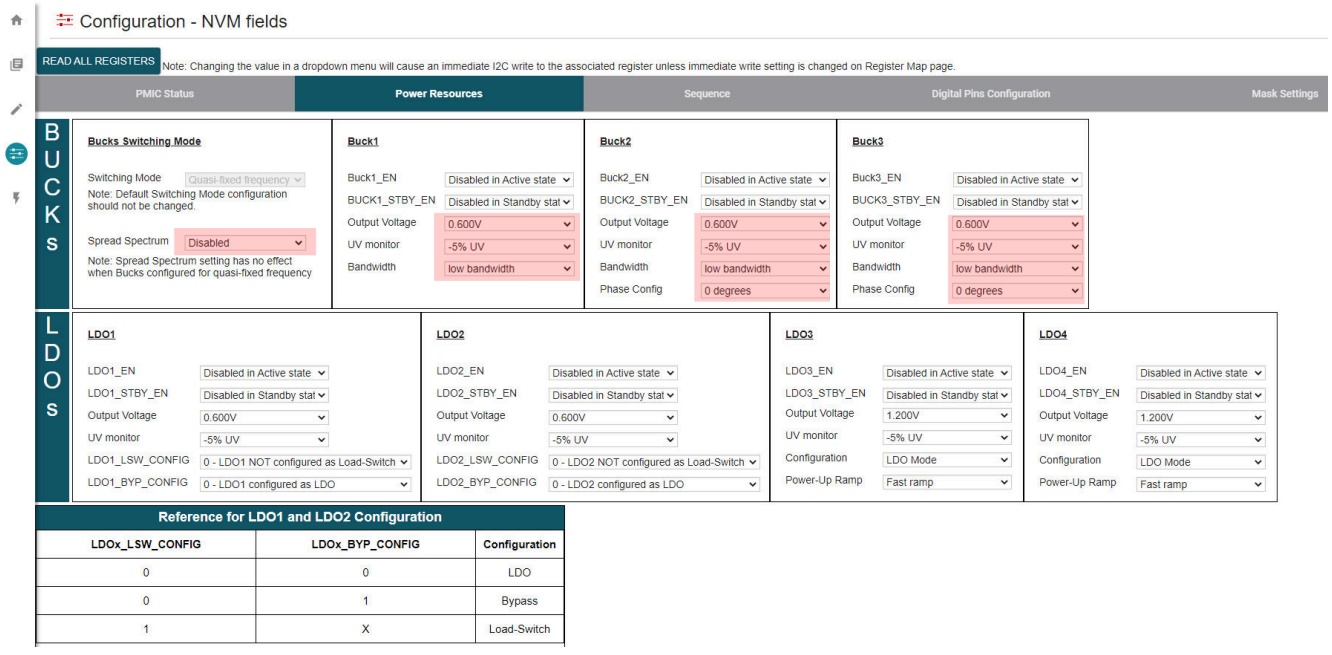

Figure 4-3. Bucks Settings Using the TPS65219-GUI

Table 4-2. NVM Registers for Buck1 Configuration

	Register Address	Bit		Settings
		Bit #	Field Name	
Bandwidth	0x0A	7	BUCK1_BW_SEL	0h = low bandwidth 1h = high bandwidth
UV monitoring		6	BUCK1_UV_THR_SEL	0h = -5% UV detection level 1h = -10% UV detection level
Output Voltage		5-0	BUCK1_VSET	see register map on data sheet

Table 4-3. NVM Registers for Buck2 Configuration

	Register Address	Bit		Settings
		Bit #	Field Name	
Bandwidth	0x09	7	BUCK2_BW_SEL	0h = low bandwidth 1h = high bandwidth
UV monitoring		6	BUCK2_UV_THR_SEL	0h = -5% UV detection level 1h = -10% UV detection level
Output Voltage		5-0	BUCK2_VSET	see register map on data sheet

Table 4-4. NVM Registers for Buck3 Configuration

	Register Address	Bit		Settings
		Bit #	Field Name	
Bandwidth	0x08	7	BUCK3_BW_SEL	0h = low bandwidth 1h = high bandwidth
UV monitoring		6	BUCK3_UV_THR_SEL	0h = -5% UV detection level 1h = -10% UV detection level
Output Voltage		5-0	BUCK3_VSET	see register map on data sheet

Table 4-5. NVM Registers for Switching Mode (Only Applicable if BUCK_FF_ENABLE = 1h)

	Register Address	Bit		Settings
		Bit #	Field Name	
Spread Spectrum	0x03	5	BUCK_SS_ENABLE	0h = Spread spectrum disabled 1h = Spread spectrum enabled
Switching Mode		4	BUCK_FF_ENABLE	DO NOT CHANGE THIS BIT
Buck2/Buck3 phase config		3-2	BUCK3_PHASE_CONFIG	0h = 0 degrees 1h = 90 degrees 2h = 180 degrees 3h = 270 degrees
		1-0	BUCK2_PHASE_CONFIG	0h = 0 degrees 1h = 90 degrees 2h = 180 degrees 3h = 270 degrees

4.3 Configuring LDOs

There are several settings that can be programmed for the LDO regulators. These include the output voltages, and under voltage (UV) monitoring among others.

- Figure 4-4 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-6, Table 4-7, Table 4-8 and Table 4-9 show the register fields to be written when NOT using the TPS65219-GUI.

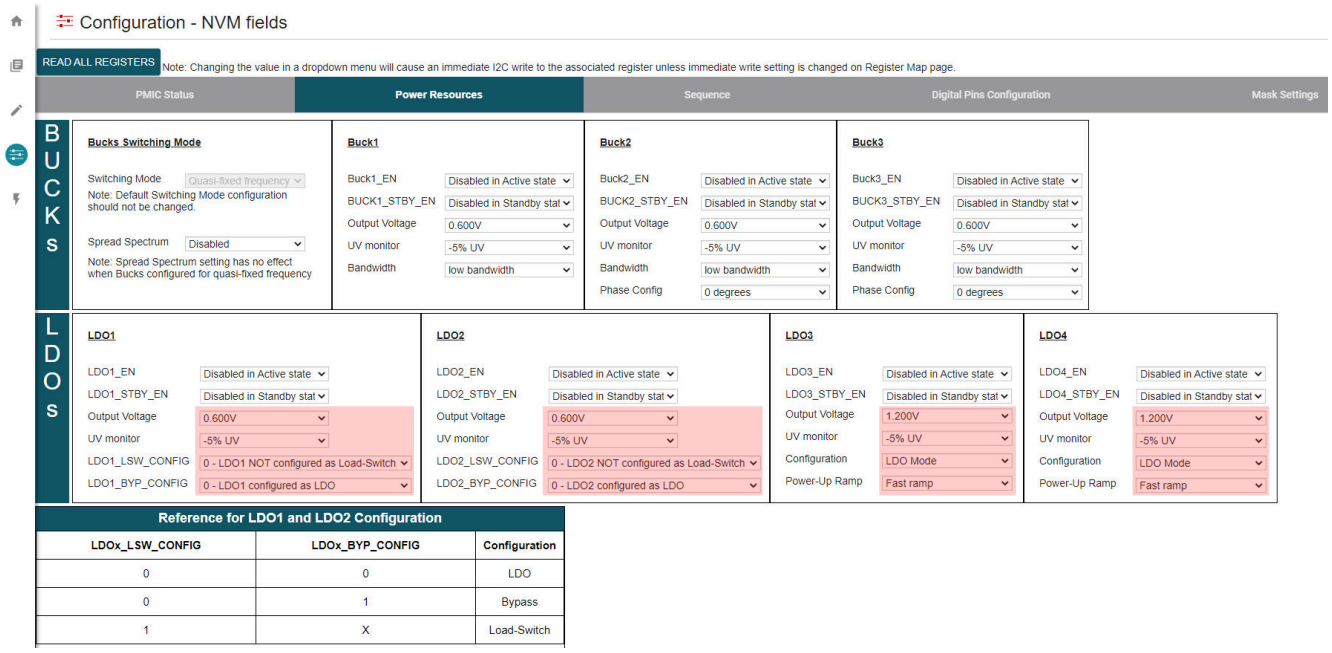

Figure 4-4. LDOs Settings Using the TPS65219-GUI

Table 4-6. NVM Registers for LDO1 Settings

	Register Address	Bit		Settings
		Bit #	Field Name	
Output Voltage	0x07	5-0	LDO1_VSET	see register map on data sheet
Configuration		7	LDO1_LSW_CONFIG	0h = LDO1 NOT configured as load-switch 1h = LDO1 configured as Load-switch
		6	LDO1_BYP_CONFIG	0h = LDO1 configured as LDO 1h = LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG 0x0)
UV monitoring	0x1E	3	LDO1_UV_THR	0h = -5% UV 1h = -10% UV

Table 4-7. NVM Registers for LDO2 Settings

	Register Address	Bit		Settings
		Bit #	Field Name	
Output Voltage	0x06	7	LDO2_VSET	see register map on data sheet
Configuration		6	LDO2_LSW_CONFIG	0h = LDO1 NOT configured as load-switch 1h = LDO1 configured as Load-switch
		5-0	LDO2_BYP_CONFIG	0h = LDO1 configured as LDO 1h = LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG 0x0)
UV Monitoring	0x1E	4	LDO2_UV_THR	0h = -5% UV 1h = -10% UV

Table 4-8. NVM Registers for LDO3 Settings

	Register Address	Bit		Settings
		Bit #	Field Name	
Output Voltage	0x05	5-0	LDO3_VSET	see register map on data sheet
Configuration		6	LDO3_LSW_CONFIG	0h = LDO Mode 1h = LSW Mode
Ramp		7	LDO3_SLOW_PU_RAMP	0h = Fast ramp for power-up 1h = Slow ramp for power-up

Table 4-8. NVM Registers for LDO3 Settings (continued)

	Register Address	Bit		Settings
		Bit #	Field Name	
UV Monitoring	0x1E	5	LDO3_UV_THR	0h = -5% UV 1h = -10% UV

Table 4-9. NVM Registers for LDO4 Settings

	Register Address	Bit		Settings
		Bit #	Field Name	
Output Voltage	0x04	5-0	LDO4_VSET	see register map on data sheet
Configuration		6	LDO4_LSW_CONFIG	0h = LDO Mode 1h = LSW Mode
Ramp		7	LDO4_SLOW_PU_RAMP	0h = Fast ramp for power-up 1h = Slow ramp for power-up
UV Monitoring	0x1E	6	LDO4_UV_THR	0h = -5% UV 1h = -10% UV

4.4 Configuring GPIOs

GPIOs can be used to enable external discrete components. GPIO can also be used for multi-PMIC configuration to sync the power-up and power-down sequence between two TPS65219 devices.

- Figure 4-5 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-10, Table 4-11 show the register fields to be written when NOT using the TPS65219-GUI.

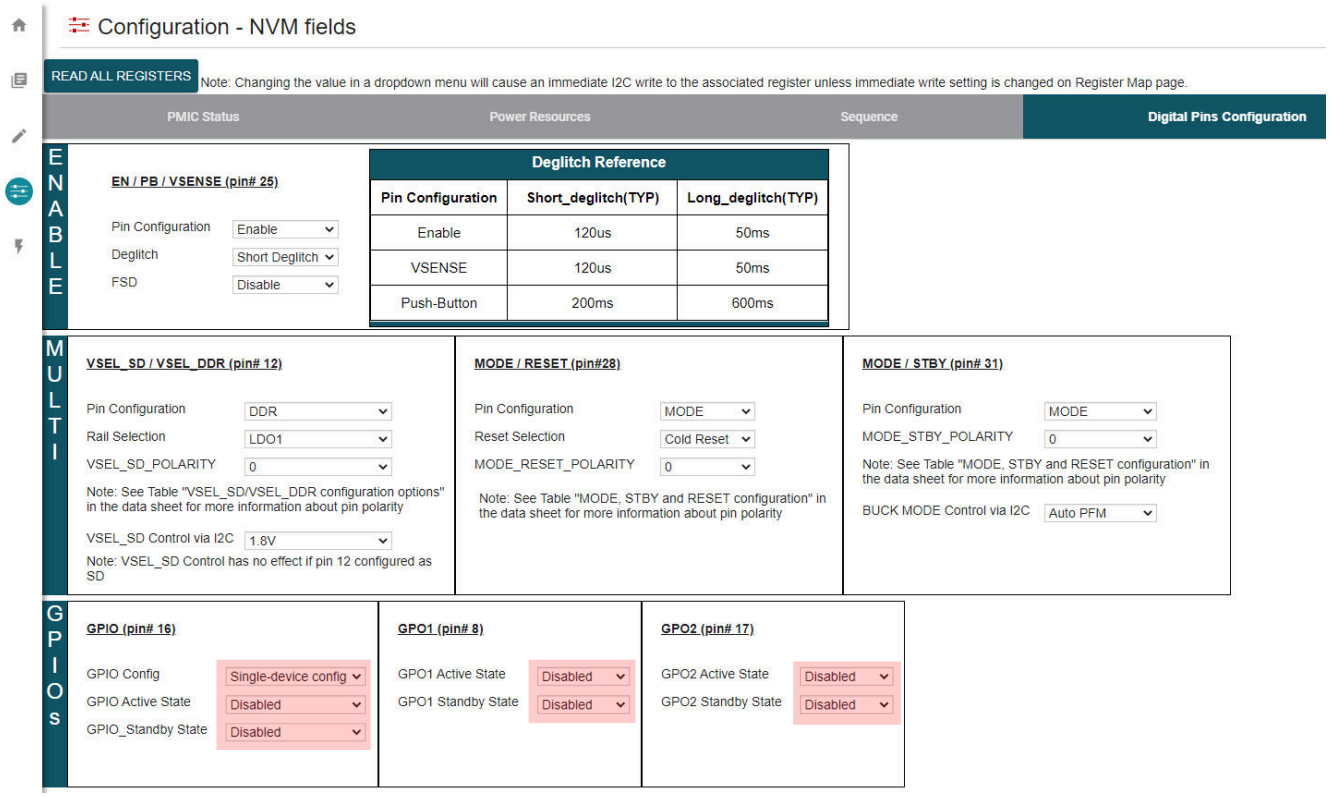

Figure 4-5. GPIOs Configuration

Table 4-10. NVM Registers for GPIO Settings

	Register Address	Bit		Settings
		Bit #	Field Name	
Enable settings in Active state	0x1E	2	GPIO_EN	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.
		1	GPO2_EN	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.
		0	GPO1_EN	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.
Enable settings in Standby state	0x22	2	GPIO_STBY_E N	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.
		1	GPO2_STBY_E N	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.
		0	GPO1_STBY_E N	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.

Table 4-11. NVM Register for Multi-PMIC Configuration

	Register Address	Bit		Settings
		Bit #	Field Name	
GPO2 configuration	0x1F	3	MULTI_DEVICE_ENABLE	0h = Single-device configuration 1h = Multi-device configuration

4.5 Configuring Sequence

The process to configure the PMIC sequence consist of the following two steps:

1. Power-up/Power-down slot assignment: The slot assignment defines the order in which rails turn ON or OFF. Each of the PMIC rails must have a slot assigned. There are 16 slots available (0-15). Multiple rails (including GPIOs) can be assigned to the same slot so they be enabled at the same time.
2. Power-up/Power-down slot duration: The slot duration is the timing between the start of one slot to the start of the next slot. For example, if Buck1 is assigned to slot0 with a 3ms duration and Buck2 is assigned to slot 1, then Buck2 turns ON 3ms after Buck1.

Note

The slot duration does not dictate how long it takes for the rails to ramp. The slot duration only specifies how long the PMIC waits before enabling (or disabling) the rails that were assigned to the next slot.

- Figure 4-6 shows the settings to be changed when using the TPS65219-GUI
- Table 4-12, Table 4-13, Table 4-14 and Table 4-15 show the register fields to be written when NOT using the TPS65219-GUI.

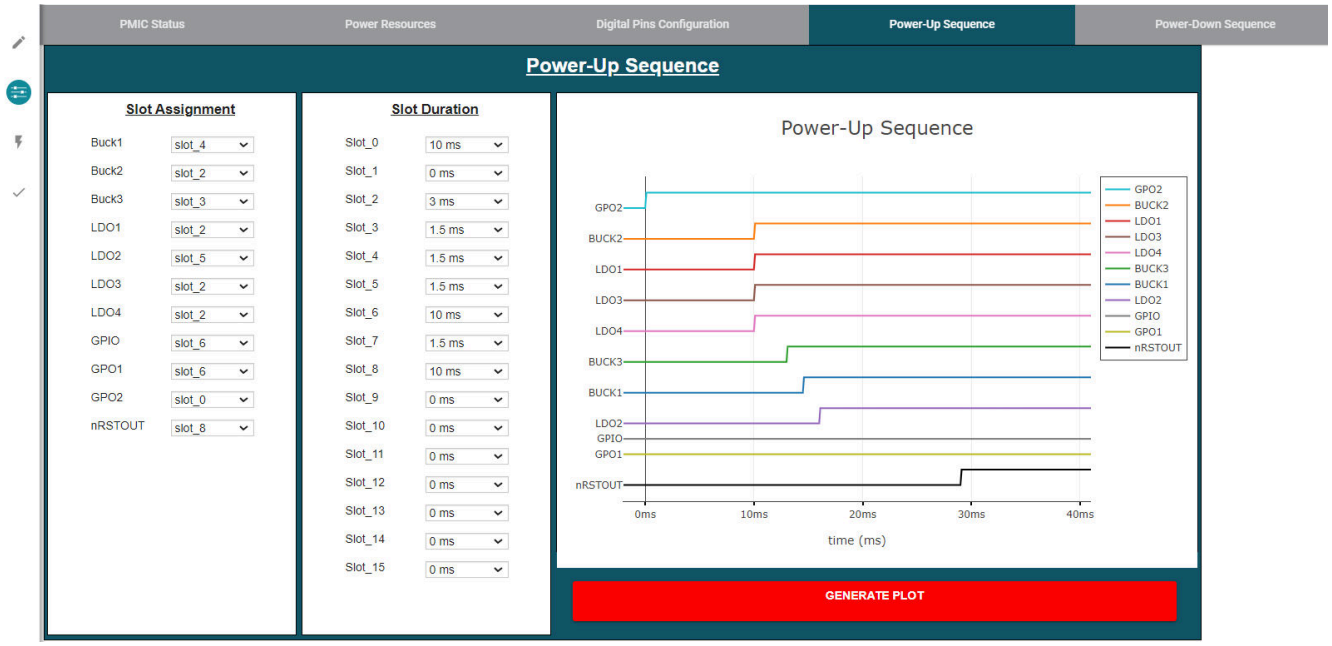

Figure 4-6. Sequence Configuration

Table 4-12. Power-Up Sequence - Slot Assignments

	Register Address	Bit		Settings
		Bit#	Field Name	
Power-up Sequence Slot Assignment	0x11	7-4	BUCK1_SEQUENCE_ON_SLOT	see register map on data sheet
	0x10	7-4	BUCK2_SEQUENCE_ON_SLOT	see register map on data sheet
	0xF	7-4	BUCK3_SEQUENCE_ON_SLOT	see register map on data sheet
	0xE	7-4	LDO1_SEQUENCE_ON_SLOT	see register map on data sheet
	0xD	7-4	LDO2_SEQUENCE_ON_SLOT	see register map on data sheet
	0xC	7-4	LDO3_SEQUENCE_ON_SLOT	see register map on data sheet
	0xB	7-4	LDO4_SEQUENCE_ON_SLOT	see register map on data sheet
	0x15	7-4	GPO1_SEQUENCE_ON_SLOT	see register map on data sheet
	0x14	7-4	GPO2_SEQUENCE_ON_SLOT	see register map on data sheet
	0x13	7-4	GPIO_SEQUENCE_ON_SLOT	see register map on data sheet
	0x12	7-4	nRST_SEQUENCE_ON_SLOT	see register map on data sheet

Table 4-13. Power-Up Sequence - Slot Duration

	Register Address	Bit		Settings
		Bit#	Field Name	
Power-up Sequence Slot Duration	0x16	7-6	POWER_UP_SLOT_0_DURATION	see register map on data sheet
		5-4	POWER_UP_SLOT_1_DURATION	see register map on data sheet
		3-2	POWER_UP_SLOT_2_DURATION	see register map on data sheet
		1-0	POWER_UP_SLOT_3_DURATION	see register map on data sheet
	0x17	7-6	POWER_UP_SLOT_4_DURATION	see register map on data sheet
		5-4	POWER_UP_SLOT_5_DURATION	see register map on data sheet
		3-2	POWER_UP_SLOT_6_DURATION	see register map on data sheet
		1-0	POWER_UP_SLOT_7_DURATION	see register map on data sheet
	0x18	7-6	POWER_UP_SLOT_8_DURATION	see register map on data sheet
		5-4	POWER_UP_SLOT_9_DURATION	see register map on data sheet
		3-2	POWER_UP_SLOT_10_DURATION	see register map on data sheet
		1-0	POWER_UP_SLOT_11_DURATION	see register map on data sheet
	0x19	7-6	POWER_UP_SLOT_12_DURATION	see register map on data sheet
		5-4	POWER_UP_SLOT_13_DURATION	see register map on data sheet
		3-2	POWER_UP_SLOT_14_DURATION	see register map on data sheet
		1-0	POWER_UP_SLOT_15_DURATION	see register map on data sheet

Table 4-14. Power-Down Sequence - Slot Assignments

	Register Address	Bit		Settings
		Bit#	Field Name	
Power-down Sequence Slot Assignment	0x11	7-4	BUCK1_SEQUENCE_OFF_SLOT	see register map on data sheet
	0x10	7-4	BUCK2_SEQUENCE_OFF_SLOT	see register map on data sheet
	0xF	7-4	BUCK3_SEQUENCE_OFF_SLOT	see register map on data sheet
	0xE	7-4	LDO1_SEQUENCE_OFF_SLOT	see register map on data sheet
	0xD	7-4	LDO2_SEQUENCE_OFF_SLOT	see register map on data sheet
	0xC	7-4	LDO3_SEQUENCE_OFF_SLOT	see register map on data sheet
	0xB	7-4	LDO4_SEQUENCE_OFF_SLOT	see register map on data sheet
	0x15	7-4	GPO1_SEQUENCE_OFF_SLOT	see register map on data sheet
	0x14	7-4	GPO2_SEQUENCE_OFF_SLOT	see register map on data sheet
	0x13	7-4	GPIO_SEQUENCE_OFF_SLOT	see register map on data sheet
	0x12	7-4	nRST_SEQUENCE_OFF_SLOT	see register map on data sheet

Table 4-15. Power-Down Sequence - Slot Duration

	Register Address	Bit		Settings
		Bit#	Field Name	
Power-down Sequence Slot Duration	0x1A	7-6	POWER_DOWN_SLOT_0_DURATION	see register map on data sheet
		5-4	POWER_DOWN_SLOT_1_DURATION	see register map on data sheet
		3-2	POWER_DOWN_SLOT_2_DURATION	see register map on data sheet
		1-0	POWER_DOWN_SLOT_3_DURATION	see register map on data sheet
	0x1B	7-6	POWER_DOWN_SLOT_4_DURATION	see register map on data sheet
		5-4	POWER_DOWN_SLOT_5_DURATION	see register map on data sheet
		3-2	POWER_DOWN_SLOT_6_DURATION	see register map on data sheet
		1-0	POWER_DOWN_SLOT_7_DURATION	see register map on data sheet
	0x1C	7-6	POWER_DOWN_SLOT_8_DURATION	see register map on data sheet
		5-4	POWER_DOWN_SLOT_9_DURATION	see register map on data sheet
		3-2	POWER_DOWN_SLOT_10_DURATION	see register map on data sheet
		1-0	POWER_DOWN_SLOT_11_DURATION	see register map on data sheet
	0x1D	7-6	POWER_DOWN_SLOT_12_DURATION	see register map on data sheet
		5-4	POWER_DOWN_SLOT_13_DURATION	see register map on data sheet
		3-2	POWER_DOWN_SLOT_14_DURATION	see register map on data sheet
		1-0	POWER_DOWN_SLOT_15_DURATION	see register map on data sheet

4.6 Configuring Multi-Function Pins

The TPS65219 PMIC has three configurable multi-function pins. MODE/STBY and MODE/RESET can be configured as MODE to select the switching, as STBY to trigger a transition to Standby state, or as RESET to trigger a cold or warm reset. The VSEL_SD/VSEL_DDR pin can be configured to set the output voltage on LDO1 or LDO2 (selectable) or to set the output voltage on Buck3. Refer to the data sheet for information on pin polarity.

Note

If VSEL_SD/VSEL_DDR is not used to set the output voltage on LDO1 (or LDO2), then it must be configured as DDR and pulled to GND with a pull-down resistor in the schematic. Additionally, VSEL_SD_I2C_CTRL must be programmed to 1h.

- Figure 4-7 shows the settings to be changed when using the TPS65219-GUI
- Figure 4-7 show the register fields to be written when NOT using the TPS65219-GUI.

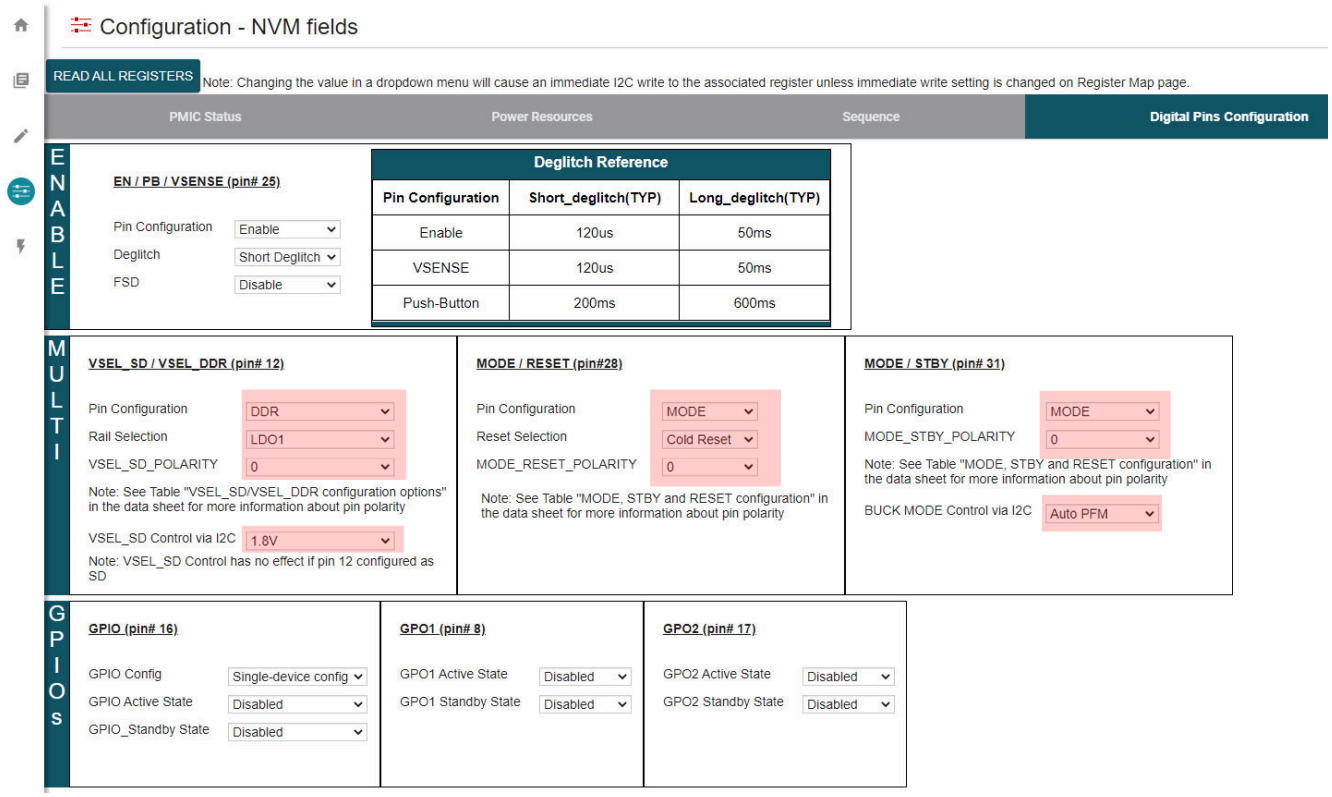

Figure 4-7. Multi-Function Configuration using the TPS65219-GUI

Table 4-16. NVM Registers for VSEL_SD / VSEL_DDR

	Register Address	Bit		Settings
		Bit #	Field Name	
Pin Function	0x1F	0	VSEL_DDR_SD	0h = VSEL pin configured as DDR to set the voltage on Buck3 1h = VSEL pin configured as SD to set the voltage on the VSEL_RAIL
VSEL rail selection		2	VSEL_RAIL	0h = LDO1 1h = LDO2
Pin polarity		1	VSEL_SD_POLARITY	0h = • LOW: 1.8V • HIGH: LDOx_VOUT register 1h = • HIGH: 1.8V • LOW: LDOx_VOUT register

Table 4-17. NVM Registers for MODE / STBY

	Register Address	Bit		Settings
		Bit #	Field Name	
Pin Function	0x20	1-0	MODE_STBY_CONFIG	0h = MODE 1h = STBY 2h = MODE and STBY 3h = MODE
Pin Polarity	0x1F	4	MODE_STBY_POLARITY	see register map on data sheet

Table 4-18. NVM Registers for MODE / RESET

	Register Address	Bit		Settings
		Bit #	Field Name	
Pin Function	0x20	2	MODE_RESET_CONFIG	0h = MODE 1h = RESET
RESET config		6	WARM_COLD_RESET_CONFIG	0h = COLD RESET 1h = WARM RESET
Pin Polarity	0x1F	5	MODE_RESET_POLARITY	see register map on data sheet

4.7 Configuring the EN/PB/VSENSE Pin

The enable pin of the PMIC can be configured as Enable, Push-Button, or VSENSE. In addition to the function, the deglitch can also be configured. Additionally, this pin has the option for first supply detection (FSD) to ignore the state of the EN/PB/VSENSE pin during the first power-up.

- Figure 4-8 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-19 show the register fields to be written when NOT using the TPS65219-GUI.

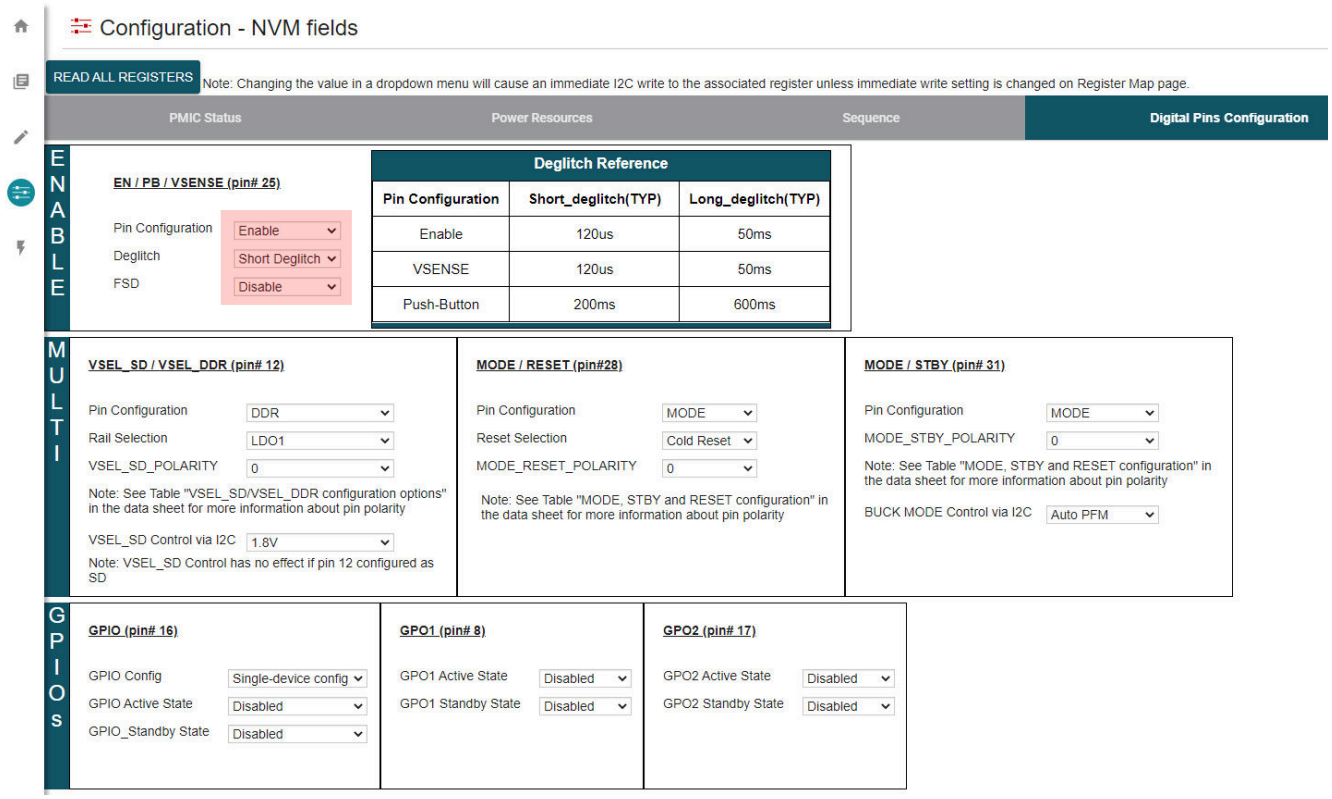

Figure 4-8. EN/PB/VSENSE Configuration Using the TPS65219-GUI

Table 4-19. NVM Registers for EN / PB / VSENSE

	Register Address	Bit		Settings
		Bit #	Field Name	
First Supply Detection	0x20	7	PU_ON_FSD	0h = FSD Disabled 1h = FSD Enabled
Pin Configuration		5-4	EN_PB_VSENSE_CONFIG	0h = Enable 1h = Push Button 2h = VSENSE 3h = Enable
Deglitch		3	EN_PB_VSENSE_DEGL	see register map on data sheet

4.8 Changing I2C Address

The TPS6521905 has the default I2C address configured as 0x30. This configuration can be changed if needed by searching for register *I2C_ADDRESS_REG* in the register map of the TPS65219_GUI and changing the default 0x30 address as shown in Figure 4-9. Once the register is changed, the new value must be saved into the NVM by writing 0x0A to register 0x34.

Note

When using multiple TPS65219 devices in multi-PMIC configuration, each device must have a unique I2C address. The I2C address for the 2nd, 3rd and other PMICs must be changed from the default 0x30 to a new value.

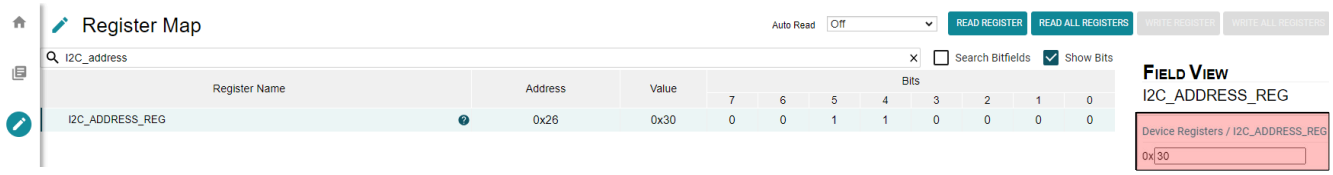

Figure 4-9. I2C_ADDRESS_REG

Table 4-20. I2C_ADDRESS_REG

Register Address	Bit	
	Bit#	Field Name
0x26	6-0	I2C_ADDRESS_REG

4.9 Configuring Mask Settings

There are several interrupt settings that can be masked to bypass specific PMIC monitoring features or modify how PMIC reacts when interrupts are detected. The interrupts that can be masked include undervoltage monitoring, temperature monitoring, among others. Figure 4-10 shows the mask settings in the configuration tab of the GUI.

Note

If any of the Mask registers is not shown in the configuration tab of the TPS65219-GUI, they can be found in the Register Map which includes the full list of registers.

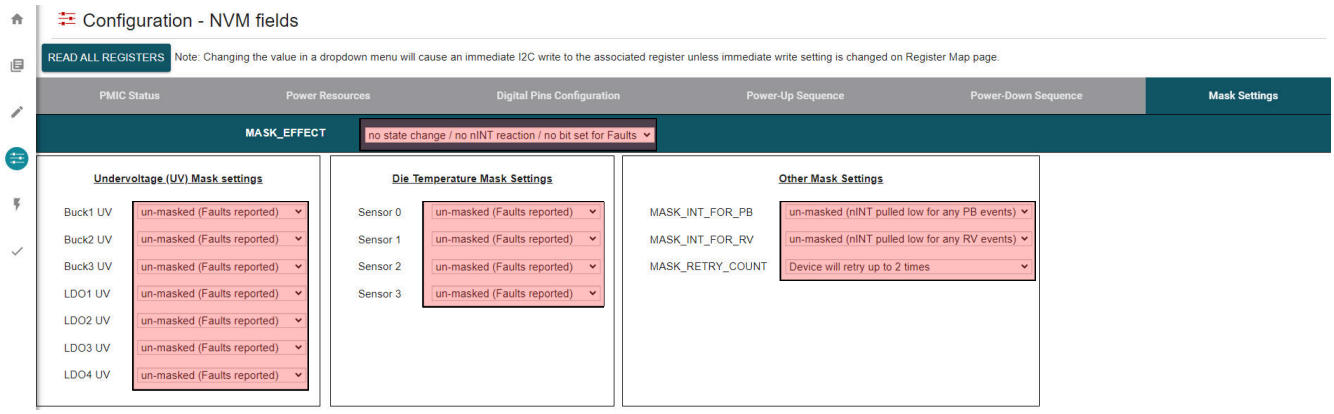

Figure 4-10. Mask Settings in TPS65219-GUI

Table 4-21. MASK Settings on Register 0x1E

Register Address	Bit	
	Bit#	Field Name
0x1E	7	BYPASS_RAILS_DISCHA RGED_CHECK

Table 4-22. MASK Settings on Register 0x1E

Register Address	Bit	
	Bit#	Field Name
0x24	7	MASK_RETRY_COUNT
	6	BUCK3_UV_MASK
	5	BUCK2_UV_MASK
	4	BUCK1_UV_MASK
	3	LDO4_UV_MASK
	2	LDO3_UV_MASK
	1	LDO2_UV_MASK
	0	LDO1_UV_MASK

Table 4-23. MASK Settings on Register 0x1E

Register Address	Bit	
	Bit#	Field Name
0x25	7	MASK_INT_FOR_PB
	6-5	MASK_EFFECT
	4	MASK_INT_FOR_RV
	3	SENSOR_0_WARM_MASK
	2	SENSOR_1_WARM_MASK
	1	SENSOR_2_WARM_MASK
	0	SENSOR_3_WARM_MASK

4.10 NVM Re-Programming

Once the register settings are updated, the new values can be saved into the NVM by writing 0x0A to register address 0x34.

- Figure 4-11 shows the button that saves the register settings into the NVM when using the TPS65219-GUI.
- Table 4-24 shows the register field to be written when NOT using the TPS65219-GUI.

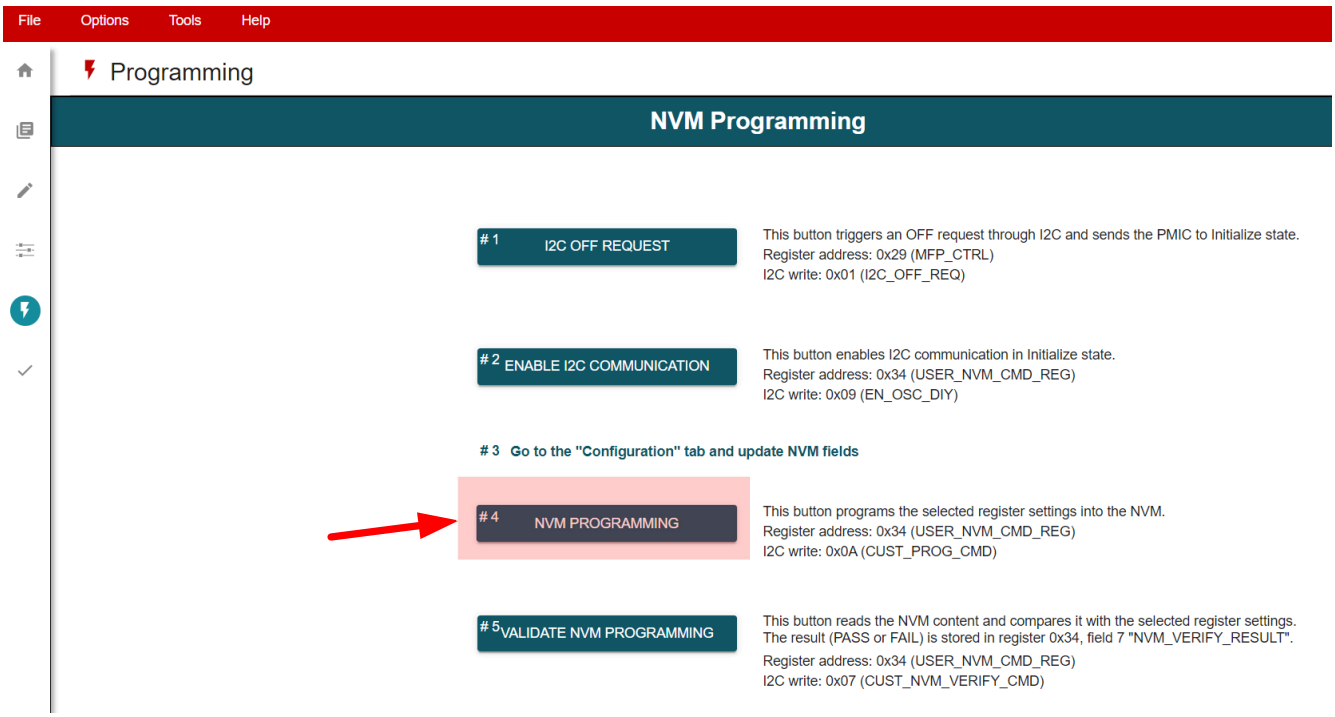

Figure 4-11. NVM Re-programming Using TPS65219-GUI

Table 4-24. I2C Write to Save Register Settings into NVM

Register Address	Bit		Data
	Bit#	Field Name	
0x34	3-0	USER_NVM_CMD	0x0A

Note

It is recommended to export the selected register settings into a CSV and JSON file using the TPS65219-GUI. Figure 4-12 shows how to export the NVM settings. The file format must be selected on "Register File Format" before using the "Save Registers As".

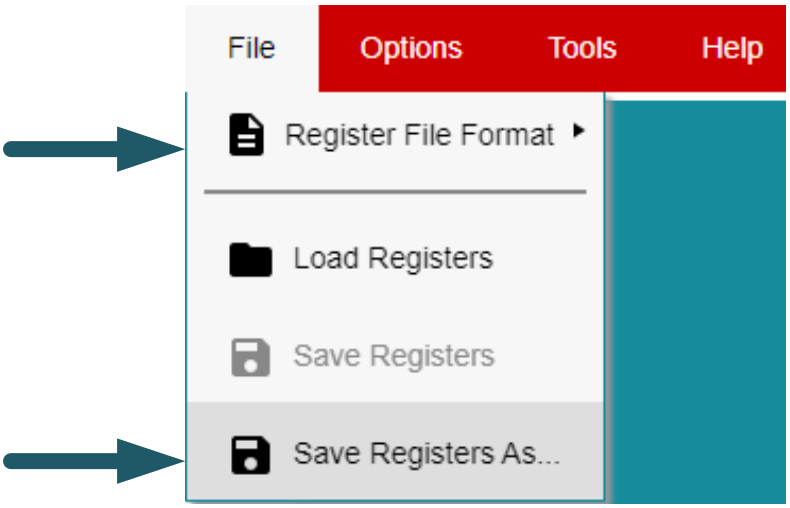

Figure 4-12. Export NVM Settings Using TPS65219-GUI

A Non-NVM Registers

The PMIC register map contains NVM and non-NVM bits. Register addresses 0x00 to 0x27 contains the NVM bits which are backed up by EEPROM. This register settings can be changed by I2C and default values can be re-programmed as described in the programming guide. The reset value for each of the NVM bits is marked as "X" in the data sheet register map as those can be re-programmed and are unique for each orderable part number.

Non-NVM bits are located in register addresses 0x28 to 0x41. These registers settings can be changed by I2C but the default values cannot be re-program. Register settings for non-NVM bits go back to their default values after a power cycle and every time the PMIC enters Initialize state. The default value for non-NVM bits can be found in the data sheet register map, under "Reset" column.

B Loading a NVM Configuration File to PMIC

The diagram shown in Figure B-1 describes the process to load a pre-configured NVM file (.CSV or .JSON extension) into the PMIC NVM. The soldered down EVM (TPS65219EVM) is used as a reference but the socketed EVM can be used as well. The TPS6521905 product page has multiple NVM files that are pre-configured to meet the requirements of specific processors or SoCs. TI's customers can reuse these files to re-program the PMICs on their production line or by working with a distributor.

Note

If the pre-configured NVM files do not meet all the application requirements, they can still be loaded to the PMIC NVM, make the necessary changes, and generate a new NVM file using the TPS65219-GUI.

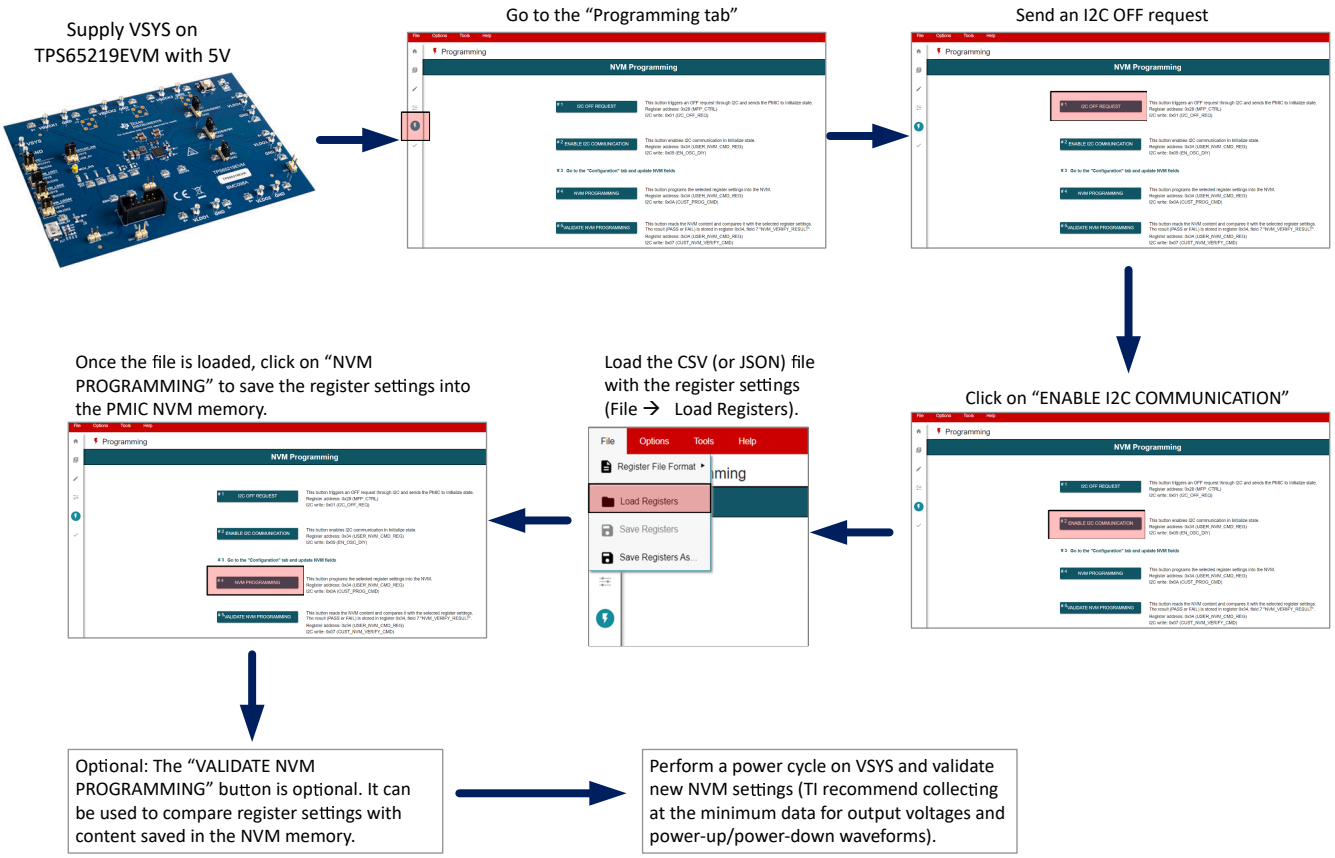

Figure B-1. Loading NVM Configuration File

C PMIC Configurable Fields

This section shows the list of programmable NVM fields for each of the PMIC power and digital resources. Some of the register fields have "x" to simplify the list. Replace "x" with the corresponding rail number to identify the correct register field in the data sheet or programming guide. Similarly, for the sequence slot duration, "y" was used to simplify the list but those can be replaced with the specific slot#.

PMIC rail	Configurable Setting	Register Field
Bucks	Enable settings	Active State: Buck**x**_EN Standby State: BUCK**x**_STBY_EN
	Output voltage	BUCK**x**_VSET
	Under-voltage monitoring	BUCK**x**_UV_THR_SEL
	Bandwidth	BUCK**x**_BW_SEL
	Power-up sequence	Slot#: BUCK**x**_SEQUENCE_ON_SLOT Duration: POWER_UP_SLOT_**y**_DURATION
	Power-down sequence	Slot#: BUCK**x**_SEQUENCE_OFF_SLOT Duration: POWER_DOWN_SLOT_**y**_DURATION
LDOs	Enable settings	Active State: LDO**x**_EN Standby State: LDO**x**_STBY_EN
	Output voltage	LDO**x**_VSET
	Under-voltage monitoring	LDO**x**_UV_THR_SEL
	Rail config (LDO, load-switch, bypass)	LDO**x**_LSW_CONFIG LDO**x**_BYP_CONFIG (LDO1, LDO2 only)
	Ramp	LDO**x**_SLOW_PU_RAMP (LDO3, LDO4 only)
	Power-up sequence	Slot#: LDO**x**_SEQUENCE_ON_SLOT Duration: POWER_UP_SLOT_**y**_DURATION
	Power-down sequence	Slot#: LDO**x**_SEQUENCE_OFF_SLOT Duration: POWER_DOWN_SLOT_**y**_DURATION
GPIOs	Enable settings GPIO	Active State: GPI/O**x**_EN Standby State: GPI/O**x**_STBY_EN
	Pin Function	MULTI_DEVICE_ENABLE (GPIO only)
	Power-up sequence	Slot#: GPI/O**x**_SEQUENCE_ON_SLOT Duration: POWER_UP_SLOT_**y**_DURATION
	Power-down sequence	Slot#: GPI/O**x**_SEQUENCE_OFF_SLOT Duration: POWER_DOWN_SLOT_**y**_DURATION
Enable pin	Pin Function	EN_PB_VSENSE_DEGL
	Deglitch	EN_PB_VSENSE_CONFIG
	First Supply Detection (FSD)	PU_ON_FSD
VSEL_SD VSEL_DDR	Pin Function	VSEL_DDR_SD
	Rail Selection	VSEL_RAIL
	Pin Polarity	VSEL_SD_POLARITY
MODE/STBY	Pin Function	MODE_STBY_CONFIG
	Pin Polarity	MODE_STBY_POLARITY
MODE/RESET	Pin Function	MODE_RESET_CONFIG
	RESET selection	WARM_COLD_RESET_CONFIG
	Pin Polarity	MODE_RESET_POLARITY
nRSTOUT	Power-up sequence	Slot#: nRST_SEQUENCE_ON_SLOT Duration: POWER_UP_SLOT_**y**_DURATION
	Power-down sequence	Slot#: nRST_SEQUENCE_OFF_SLOT Duration: POWER_DOWN_SLOT_**y**_DURATION

Figure C-1. NVM programmable Fields

D References

1. Texas Instruments, TPS6521905 data sheet
2. Texas Instruments, TPS65219EVM-SKT user's guide

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