Power-supply sequencing for FPGAs

By Sami Sirhan
Analog Systems Engineering
Sureena Gupta
Applications Engineer

Introduction

Power-supply sequencing is an important aspect to consider when designing with a field programmable gate array (FPGA). Typically, FPGA vendors specify power-sequencing requirements because an FPGA can require anywhere from three to over ten rails.

By following the recommended power sequence, excessive current draw during startup can be avoided, which in turn prevents damage to devices. Sequencing the power supplies in a system can be accomplished in several ways. This article elaborates on sequencing solutions that can be implemented based on the level of sophistication needed by a system.

Sequencing solutions addressed in this article are:

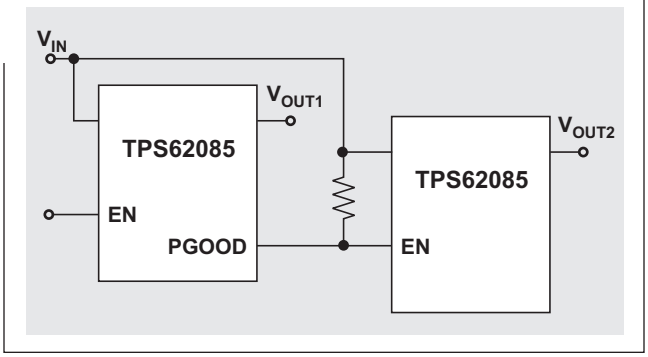
1. Cascading PGOOD pin into enable pin
2. Sequencing using a reset IC
3. Analog up/down sequencers
4. Digital system health monitors with PMBus interface

Method 1: Cascading PGOOD pin into enable pin

A basic, cost-effective way to implement sequencing is to cascade the power good (PG) pin of one power supply into the enable (EN) pin of the next sequential supply (Figure 1). The second supply begins to turn on when the PG threshold is met, usually when the supply is at 90% of its final value. This method offers a low-cost approach, but timing cannot be easily controlled. Adding a capacitor to the EN pin can introduce timing delays between stages. However, this method is unreliable during temperature variations and repeated power cycling.

Also, this method does not support power-down sequencing.

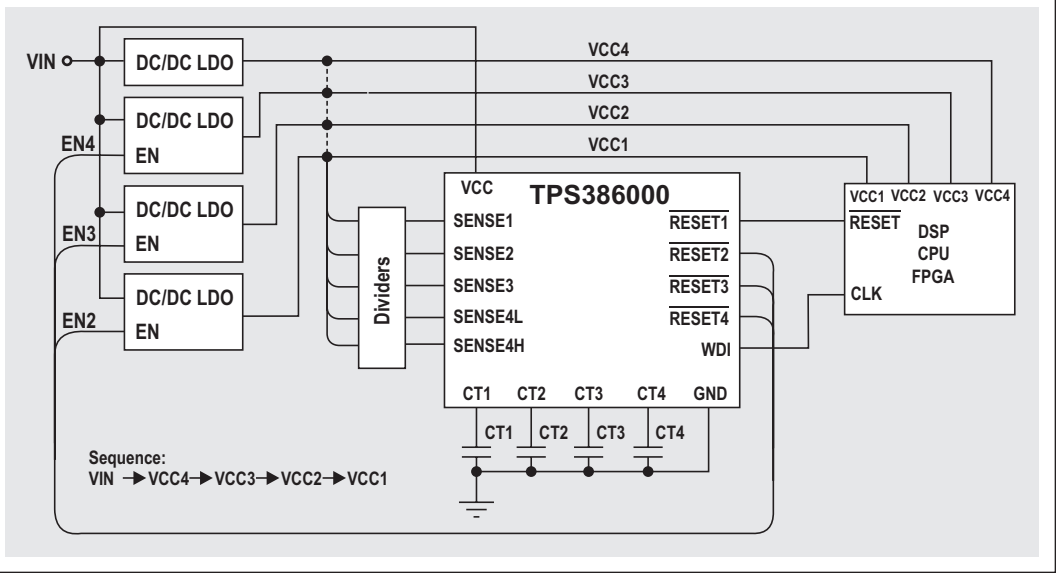
Figure 1. Cascading PGOOD pin into enable pin



Method 2: Sequencing using a reset IC

Another simple option to consider for power-up sequencing is a reset IC with time delay. With this option, the reset IC monitors the power rails with tight threshold limits. Once the power rail is within 3% or less of its final value, the reset IC enters the wait period defined by the solution before powering up the next rail. The wait period can be programmed into the reset IC using EEPROM or be set by external capacitors. A typical multi-channel reset IC is shown in Figure 2. The advantage of using a reset IC for power-up sequencing is that the solution is monitored.

Figure 2. Power-up sequencing with a multi-output reset IC



Each rail is confirmed to be within regulation before releasing the next rail and there is no need for a PGOOD pin on the power converter. The drawback of using a reset-IC solution for sequencing is that it does not implement power-down sequencing.

Method 3: Analog up/down sequencers

Implementing power-up sequencing can be easier than implementing power-down sequencing. To achieve power-up and power-down sequencing, there are simple analog sequencers (Figure 3) that can reverse (Sequence 1) or even mix (Sequence 2) the power-down sequence relative to the power-up sequence. Upon power up, all the flags are held low until EN is pulled high. After EN is asserted, each flag goes open drain (pull-up resistor is required) sequentially after an internal timer has elapsed. The power-down sequence is the same as power up, but in reverse order.

Cascading multiple sequencers

Sequencers can be cascaded together to support many power rails, as well as provide fixed and adjustable delay times between enable signals. In Figure 4, two sequencers cascade together to achieve six sequenced rails. Upon power up, the AND gate ensures that the second sequencer does not trigger until it has received both an EN signal and rail C has triggered. On power down, the AND gate ensures that the second sequencer sees the EN falling edge, irrespective of output C. The OR gate ensures that the first sequencer is triggered with the EN rising edge. Upon power down, the OR gate ensures that the first sequencer can't see the EN falling edge until D has fallen. This guarantees power-up and power-down sequencing, but does not offer a monitored sequence.

Monitored up/down sequencing

Monitored sequencing can be added to the circuit in Figure 4 by simply adding a couple of AND gates between the FlagX output and the PG pin as shown in Figure 5. In this example, PS2 is enabled only if PS1 is greater than 90% of its final value. This method offers a low-cost, monitored sequencing solution.

Method 4: Digital system health monitors with PMBus interface

If a system requires the utmost flexibility, a good solution is a PMBus/I²C-compatible, digital-system health monitor such as the UCD90120A. Such solutions offer maximum control for any sequencing need by allowing the designer to configure ramp up/down times, on/off delays, sequence dependencies, and even voltage and current monitoring.

Figure 3. Implementation of an analog up/down sequencer

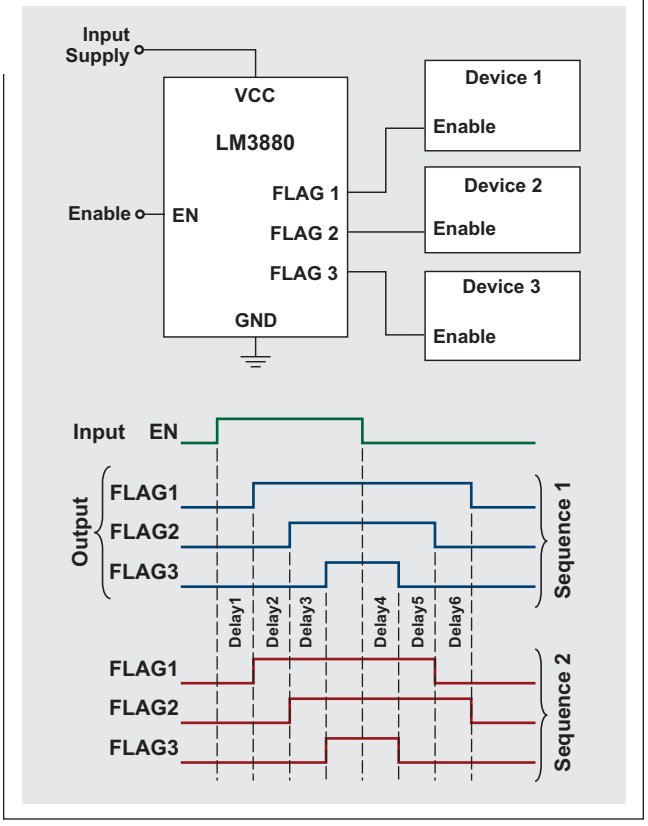


Figure 4. Cascading multiple analog sequencers

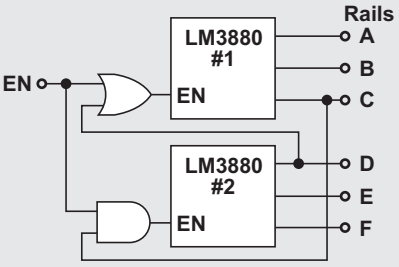


Figure 5. Adding monitored sequencing to a simple time-based sequencer

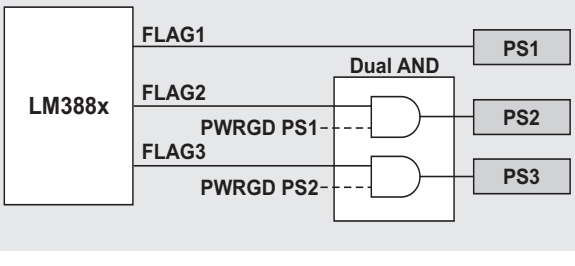
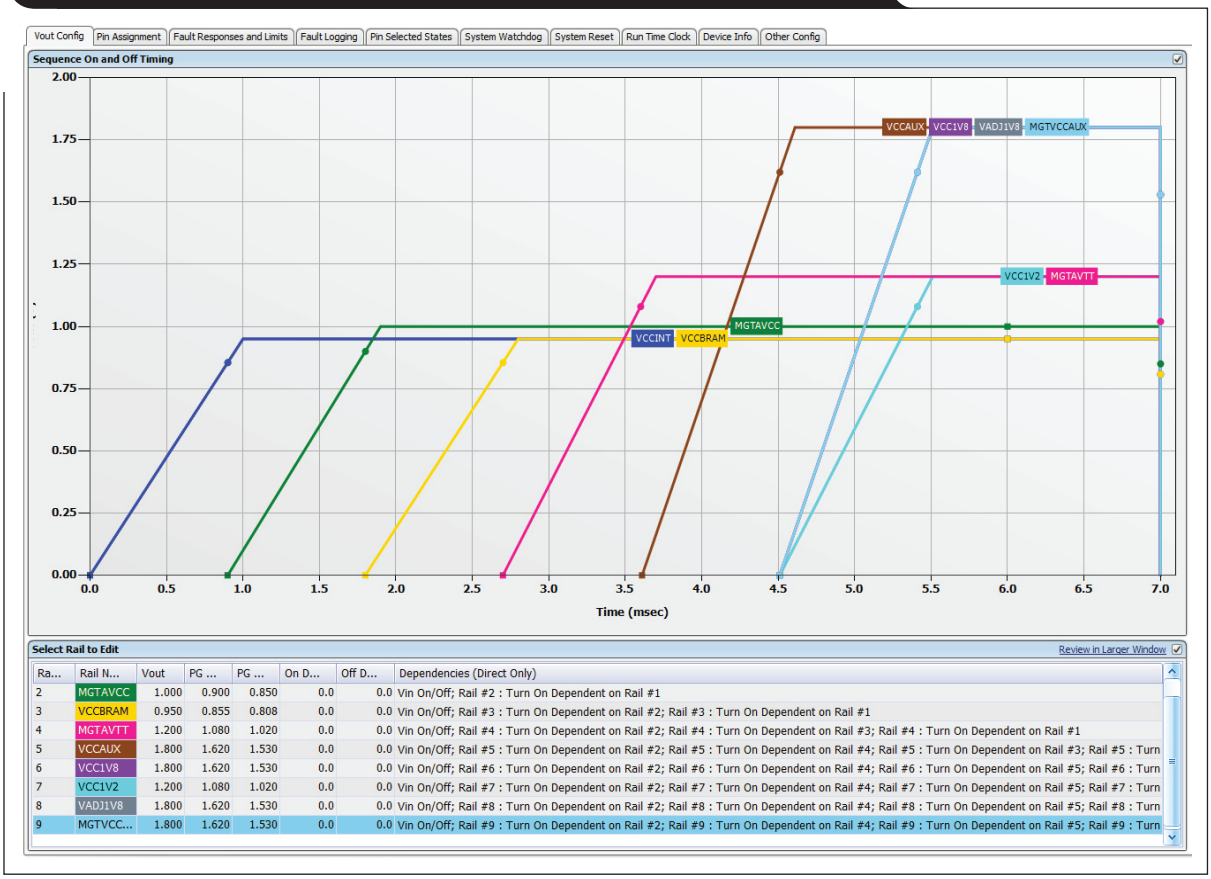


Figure 6. Example of power up sequencing using the UCD90120A GUI



Ra...	Rail N...	Vout	PG ...	PG ...	On D...	Off D...	Dependencies (Direct Only)
2	MGTAVCC	1.000	0.900	0.850	0.0	0.0	Vin On/Off; Rail #2 : Turn On Dependent on Rail #1
3	VCCBRAM	0.950	0.855	0.808	0.0	0.0	Vin On/Off; Rail #3 : Turn On Dependent on Rail #2; Rail #3 : Turn On Dependent on Rail #1
4	MGTAVTT	1.200	1.080	1.020	0.0	0.0	Vin On/Off; Rail #4 : Turn On Dependent on Rail #2; Rail #4 : Turn On Dependent on Rail #3; Rail #4 : Turn On Dependent on Rail #1
5	VCCAUX	1.800	1.620	1.530	0.0	0.0	Vin On/Off; Rail #5 : Turn On Dependent on Rail #2; Rail #5 : Turn On Dependent on Rail #4; Rail #5 : Turn On Dependent on Rail #3; Rail #5 : Turn
6	VCC1V8	1.800	1.620	1.530	0.0	0.0	Vin On/Off; Rail #6 : Turn On Dependent on Rail #2; Rail #6 : Turn On Dependent on Rail #4; Rail #6 : Turn On Dependent on Rail #5; Rail #6 : Turn
7	VCC1V2	1.200	1.080	1.020	0.0	0.0	Vin On/Off; Rail #7 : Turn On Dependent on Rail #2; Rail #7 : Turn On Dependent on Rail #4; Rail #7 : Turn On Dependent on Rail #5; Rail #7 : Turn
8	VADJ1V8	1.800	1.620	1.530	0.0	0.0	Vin On/Off; Rail #8 : Turn On Dependent on Rail #2; Rail #8 : Turn On Dependent on Rail #4; Rail #8 : Turn On Dependent on Rail #5; Rail #8 : Turn
9	MGTVCC...	1.800	1.620	1.530	0.0	0.0	Vin On/Off; Rail #9 : Turn On Dependent on Rail #2; Rail #9 : Turn On Dependent on Rail #4; Rail #9 : Turn On Dependent on Rail #5; Rail #9 : Turn

Digital-system health monitors come with a graphical user interface (GUI) that can be used to program power-up and power-down sequencing along with other system parameters (Figure 6). Some digital system health monitors also have non-volatile-error and peak-value logging that helps with system-failure analysis in case of a brown-out event.

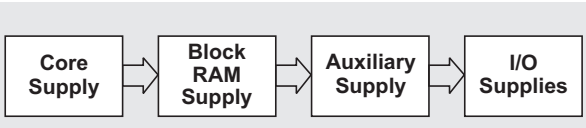
FPGA sequencing requirements examples

FPGA vendors such as Xilinx or Altera provide either a recommended or required power-up sequence in their datasheets that are easily accessible online. Sequencing requirements vary between vendors and vary from one vendor's FPGA family to another. Also listed in datasheets are timing requirements for ramp-up and shutdown. The recommended power-down sequence is typically the reverse order of the power-up sequence. An example of power-up sequencing is shown in Figure 7.

Conclusion

There are several sequencing solutions that can be utilized to follow the requirements specified by FPGA vendors. System requirements may include power monitoring in addition to power-up and power-down sequencing, but the optimal power solution for an FPGA will depend on system complexity and specifications.

Figure 7. Example of a FPGA power-logic sequence



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