LP38788-ADJ High PSRR, Ultra Low Noise, 800mA Linear Voltage Regulator for RF/Analog Circuits

Check for Samples: LP38788, LP38788-ADJ

FEATURES

- **Ultra-Low Output Noise: 4 μV_{RMS} (10Hz to 100 kHz)**
- **High PSRR: 70db at 1 kHz; 60dB at 10 kHz**
- **Wide Operating Input Voltage Range: 4.5V to 15V**
- **±1.0% Output Voltage Initial Accuracy (T_J = 25°C)**
- **Very Low Dropout : 250 mV (typical) at 800mA**
- **Stable with Ceramic or Tantalum Output Capacitors**
- **Excellent Line and Load Transient Response**
- **Over-Current and Over-Temperature Protection**

APPLICATIONS

- **RF and VCO Power**
- **Wireless LAN Devices**
- **Wireless Cable Modems**
- **Low Noise Post Regulation**

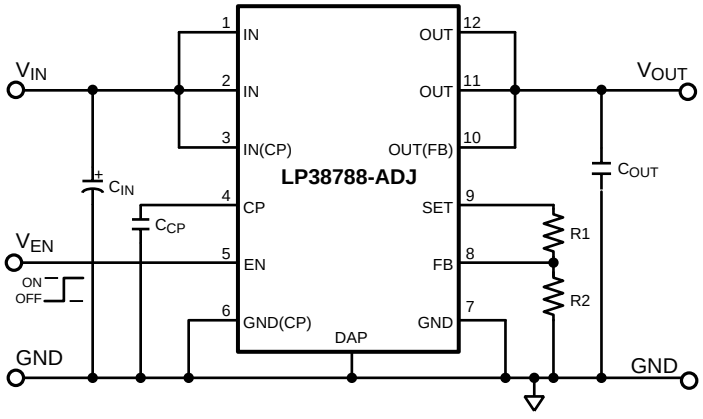
DESCRIPTION

The LP38788-ADJ is a high performance linear regulator capable of supplying 800 mA output current. Designed to meet the requirements of sensitive RF/Analog circuitry, the LP38788 implements a novel linear topology on an advanced CMOS process to deliver ultra-low output noise and high PSRR at switching power supply frequencies. The LP38788-ADJ is stable with both ceramic and tantalum output capacitors and requires a minimum output capacitor of only 1 µF for stability.

The LP38788-ADJ can operate over a wide input voltage range (4.5V to 15V) making it well suited for many post regulation applications.

Available in a 12-Lead LLP package (4.0 x 4.0 x 0.8 mm).

Typical Application Circuit



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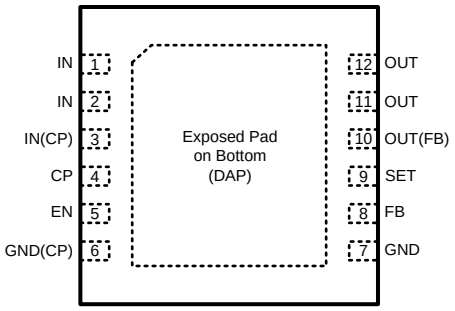
PRODUCT PREVIEW

Connection Diagram



Connect LLP DAP to GND

Figure 1. LP38788SD-ADJ (Top View)
12-Lead LLP Package

Pin Functions

Pin Descriptions

Pin	Name	Function
1, 2	IN	Device unregulated input voltage pins. Connect pins together at the package.
3	IN(CP)	Charge pump input voltage pin. Connect directly to pins 1 and 2 at the package.
4	CP	Charge pump output. See CHARGE PUMP section in the Applications Information for more information.
5	EN	Enable pin. A Logic high level is required on this pin to enable the LDO output. A Logic low level will turn the output off and reduce the operating current of the device. See ENABLE INPUT OPERATION section in the Applications Information for more information.
6	GND	Device charge pump ground pin.
7	GND	Device analog ground pin.
8	FB	Feedback pin for programming the output voltage.
9	SET	Internally filtered pre-buffered output. A feedback resistor divider network from this pin to FB and GND will set the output voltage of the device.
10	OUT(FB)	OUT buffer feedback pin. Connect directly to pins 11 and 12 at the package.
11, 12	OUT	Device regulated output voltage pins. Connect pins together at the package.
Exposed Pad	DAP	The exposed die attach pad on the bottom of the package should be connected to a thermal pad at ground potential. See LLP THERMAL CONSIDERATIONS section in the Applications Information for more information.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PRODUCT PREVIEW

Absolute Maximum Ratings (1)

IN	-0.3V to 20V
OUT	-0.3V to V_{IN} + 0.3V
FB, EN	-0.3V to 6.0V
Storage Temperature Range	-65°C to +150°C
Soldering (2)	260°C, 10 sec
ESD Rating (HBM) (3)	2 kV
Power Dissipation (4)	Internally Limited
I_{OUT} (Survival)	Internally Limited

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For guaranteed specifications and conditions, see the Electrical Characteristics table.

(2) Peak Reflow Temperatures for Surface Mount devices are defined in “Absolute Maximum Ratings for Soldering”, Literature Number: SNOA549C

(3) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Applicable standard is JESD-22-A114-C.

(4) The value of θ_{J-A} for the LLP-8 and package is dependent on PCB copper area, copper thickness, the number of copper layers in the PCB, and the number of thermal vias under the exposed thermal pad (DAP). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See LLP THERMAL CONSIDERATIONS in the Applications Information.

Operating Ratings (1)

Input Voltage, V_{IN}	V_{OUT} + V_{DO} to 15.0V
Output Voltage, V_{OUT}	4.00V to V_{IN} - V_{DO}
Enable Voltage, V_{EN}	0.0V to 5.0V
Junction Temperature, T_J	-40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For guaranteed specifications and conditions, see the Electrical Characteristics table.

PRODUCT PREVIEW

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the operating junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 5.5V, V_{SET} = 5.00V, C_{CP}= 10 nF, C_{IN} = 10 µF 50mΩ Tantalum, C_{OUT} = 10 µF X7R MLCC, I_{OUT} = 10 mA, and T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{FB}	Feedback Voltage		1.188 (-1%)	1.200	1.212 (+1%)	V
		5.5V ≤ V_{IN} ≤ 15.0V	**1.176 (-2%)**		**1.224 (+2%)**	
V_{OS}	Voltage Offset	V_{OUT} - V_{SET}	0	3	**25**	mV
I_{FB}	Feedback Pin Current	V_{FB} = 1.200V	-	0	**1**	µA
I_{SET}	SET Pin Internal Current Sink	V_{IN} = 4.5V, V_{SET} = 4.00V	-	46	-	µA
		V_{IN} = 5.5V, V_{SET} = 5.00V	**28.0**	52	**76.0**	
		V_{IN} = 12.5V, V_{SET} = 12.0V	-	71	-	
ΔV_{OUT} / ΔV_{IN}	Line Regulation (1)	5.5V ≤ V_{IN} ≤ 15.0V I_{OUT} = 10mA	-	0.005	-	%/V
ΔV_{OUT} / ΔI_{OUT}	Load Regulation (2)	V_{IN} = 5.5V 10 mA ≤ I_{OUT} ≤ 800 mA	-	-0.2	-	%/A
V_{DO}	Dropout Voltage (3)	I_{OUT} = 800 mA	-	250	**565**	mV
UVLO	Under-Voltage Lock-Out	V_{IN} Rising	**2.31**	2.65	**3.00**	V
ΔUVLO	UVLO Hysteresis	V_{IN} Falling from UVLO threshold	-	180	-	mV
I_{GND}	Ground Pin Current (4)	I_{OUT} = 800mA	-	1.2	**5.0**	mA
I_Q	Ground Pin Current, Quiescent (4)	I_{OUT} = 0 mA	-	1.3	**5.0**	mA
I_{SD}	Ground Pin Current, Shutdown (4)	V_{EN} = 0.0V	-	6.7	**20.0**	µA
I_{SC}	Short Circuit Current	R_{LOAD} = 0Ω	**540**	1100	**2000**	mA
ΔV_{CP}	CP Pin Voltage above V_{IN}	V_{CP} - V_{IN}	-	2.8	-	V
t_{START}	Start-up Time	From V_{EN} > $V_{EN(ON)}$ to V_{OUT} ≥ 98% of $V_{OUT(NOM)}$	-	150	**250**	µs
PSRR	Power Supply Rejection Ratio	V_{IN} = 5.00V, V_{OUT} = 4.70V, f = 10 kHz	-	60	-	dB
		V_{IN} = 5.00V, V_{OUT} = 4.70V, f = 100 kHz	-	23	-	
		V_{IN} = 5.00V, V_{OUT} = 4.70V, f = 1 MHz	-	33	-	
e_N	Output Noise Voltage (RMS)	V_{IN} = 5.5V, V_{OUT} = 5.00V BW = 10 Hz to 100 kHz	-	4	-	$\mu V_{(RMS)}$
ENABLE INPUT						
$V_{EN(ON)}$	Enable ON Threshold Voltage	V_{EN} rising from 0.50V until Output is ON	**1.05**	1.25	**1.45**	V
ΔV_{EN}	Enable Threshold Voltage Hysteresis	V_{EN} Falling from $V_{EN(ON)}$ until Output is OFF	-	100	-	mV
$I_{EN(IL)}$	EN Pin Low Bias Current	V_{EN} = 500 mV	-	2	**3.0**	µA
$I_{EN(IH)}$	EN Pin High Bias Current	V_{EN} = 2.0V	-	2	**3.0**	µA

(1) Line Regulation: % change in $V_{OUT(NOM)}$ for every 1V change in V_{IN}= ((ΔV_{OUT} / $V_{OUT(NOM)}$) / ΔV_{IN}) x 100%
(2) Load Regulation: % change in $V_{OUT(NOM)}$ for every 1A change in I_{OUT} = ((ΔV_{OUT} / $V_{OUT(NOM)}$) / ΔI_{OUT}) x 100%
(3) Dropout voltage (V_{DO}) is defined as the differential voltage measured between V_{OUT} and V_{IN} when V_{IN}, falling from V_{IN} = V_{OUT} + 1V, causes V_{OUT} to drop 2% below the value measured with V_{IN} = V_{OUT} + 1V.
(4) Ground pin current is the sum of the current in both GND pins (Pin 4 + Pin 5) only, and does not include current from the SET pin.

PRODUCT PREVIEW

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the operating junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 5.5V, V_{SET} = 5.00V, C_{CP}= 10 nF, C_{IN} = 10 µF 50mΩ Tantalum, C_{OUT} = 10 µF X7R MLCC, I_{OUT} = 10 mA, and T_J = 25°C.

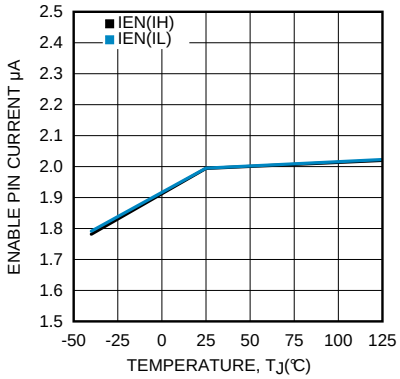
Symbol	Parameter	Conditions	Min	Typical	Max	Units
$V_{EN(CLAMP)}$	Enable Pin Clamp Voltage	EN Pin = Open	**3.6**	4.9	**6.2**	V
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Junction Temperature (T_J) Rising	-	145	-	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	Junction Temperature (T_J) Falling from T_{SD}	-	12	-	

PRODUCT PREVIEW

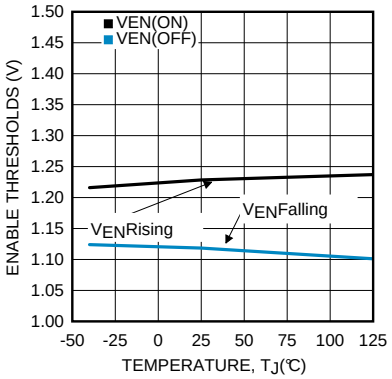
Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.00V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

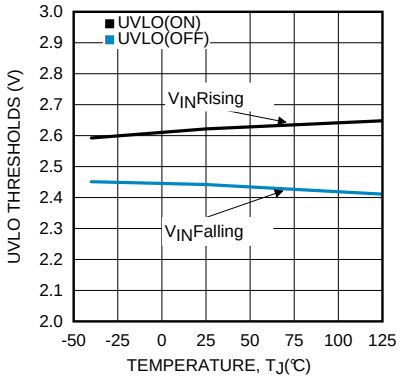
Enable Pin Current



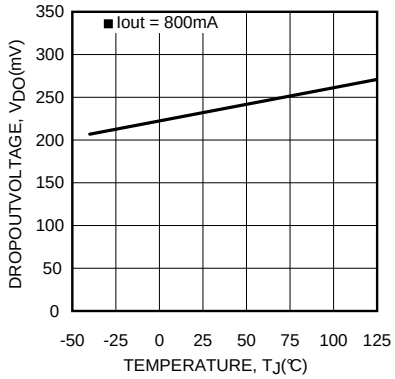
Enable Thresholds



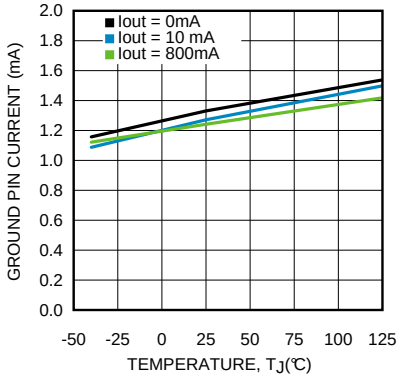
UVLO Thresholds



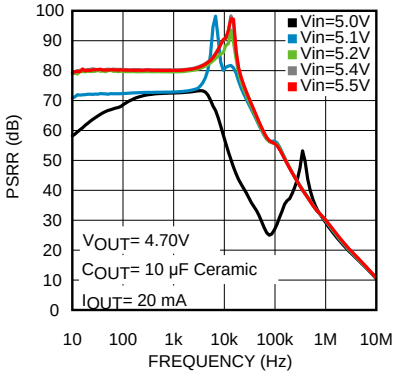
Dropout Voltage, V_{DO}



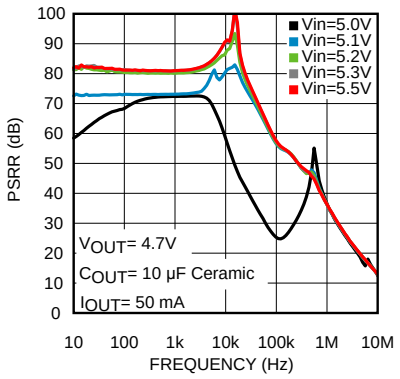
Ground Pin Current



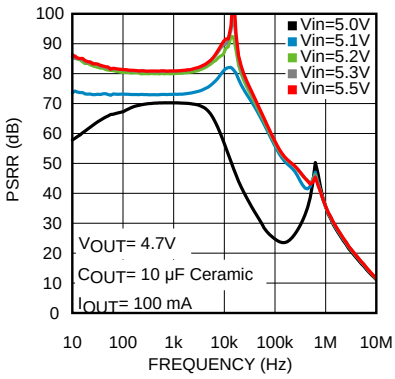
PSRR, I_{OUT} = 20 mA



PSRR, I_{OUT} = 50 mA



PSRR, I_{OUT} = 100 mA

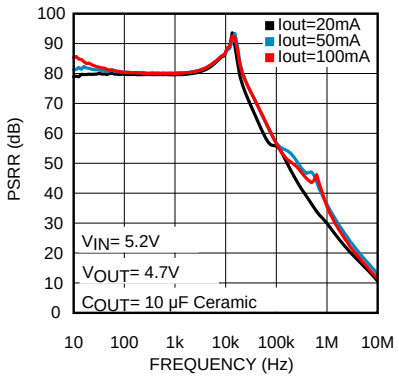


PRODUCT PREVIEW

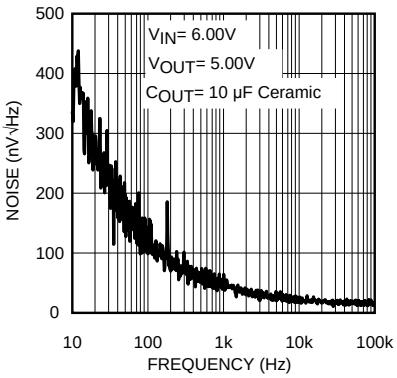
Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.00V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

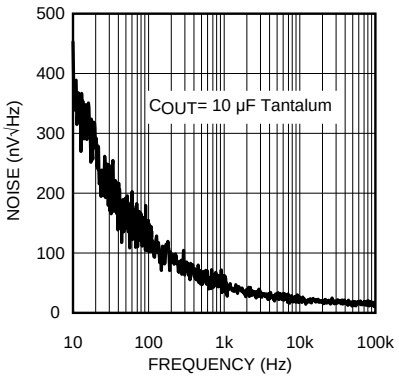
PSRR, V_{IN} - V_{OUT} = 500 mV



NOISE, C_{OUT} = 10 µF Ceramic

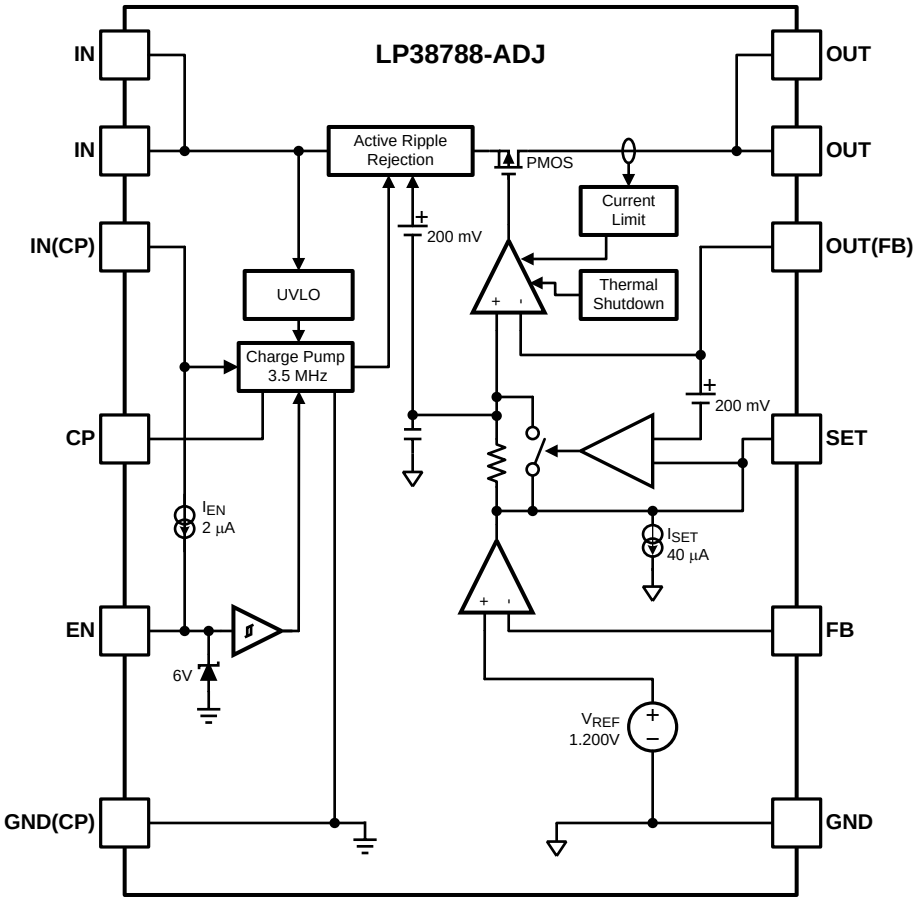


NOISE, C_{OUT} = 10 µF Tantalum



PRODUCT PREVIEW

Block Diagram



Application Information

PACKAGE INFORMATION

The LP38788SD-ADJ is available in the 12-Lead LLP (SDA12B) surface mount package that allows for increased power dissipation compared to the standard PSOP-8 and LLP-8 packages.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP38788SD-ADJ requires external capacitors for regulator stability. These capacitors must be correctly selected for optimum performance.

INPUT CAPACITOR: Minimum recommended input capacitance is 1 µF.

Capacitor tolerance and variations due temperature and applied voltage must be considered when selecting a capacitor to assure the minimum requirement of input capacitance is met over the intended operating range.

The input capacitor must be located as close as physically possible to the input pin and returned to a clean analog ground. Any good quality Tantalum capacitor may be used, while a Ceramic capacitor should be X5R or X7R rated with appropriate adjustments due to the loss of capacitance value from the applied DC voltage.

OUTPUT CAPACITOR: The LP38788 requires an output capacitor whose value is at least 1 µF, however a minimum output capacitance of 10 µF is strongly recommended. While the LP38788 is designed to work with Ceramic output capacitors, the output capacitor can be Ceramic, Tantalum, or a combination. Capacitance type, tolerance, ESR, as well as temperature and voltage characteristics, must be considered when selecting an output capacitor for the application.

PRODUCT PREVIEW

The output capacitor must be located not more than 0.5" from the output pin and returned to a clean analog ground to the LP38788 GND pin.

CHARGE PUMP

The charge pump is running when both the input voltage is above the UVLO threshold (2.65V typical) and the EN pin voltage is above the $V_{EN(ON)}$ threshold (1.25V typical). The typical charge pump operating frequency is 3.5 MHz.

A low leakage 10 nF (0.01 µF) to 100 nF (0.1 µF) storage capacitor is required between the CP pin and ground to store the energy required for gate drive of the internal NMOS pass device.

Do not make any other connection to the CP pin. Loading this pin in any manner will degrade regulator performance. No external biasing may be applied to, or derived from, this pin, as permanent damage to the internal charge pump circuitry may occur.

SETTING THE OUTPUT VOLTAGE

Current sourced from the SET pin, through R1 and R2, must be kept to less than 100 µA. The minimum allowed value for R2 is 12.9 kΩ

$$I_{SET} = V_{FB} / R2 \quad (1)$$

$$R2_{MIN} = V_{FB(MAX)} / 100\ \mu A \quad (2)$$

$$R2_{MIN} = 12.9\ k\Omega \quad (3)$$

The values for R1 and R2 may be adjusted as needed to achieve the desired output voltage as long as the value for R2 is no less than 12.9 kΩ. The maximum recommended value for R2 is 100 kΩ.

The following equation is used to determine the output voltage:

$$V_{OUT} = (V_{FB} \times (1 + (R1 / R2))) + V_{OS} \quad (4)$$

Alternately, the following formula can be used to determine the appropriate R1 value for a given R2 value:

$$R1 = R2 \times (((V_{OUT} - V_{OS}) / V_{FB}) - 1) \quad (5)$$

The following table suggests some ±1% values for R1 and R2 for a range of output voltages using the typical V_{FB} value of 1.200V. This is not a definitive list, as other combinations exist that will provide similar, possibly better, performance.

Target V_{OUT}	R1	R2	Typical V_{OUT}
4.70V	47.5 kΩ	16.2 kΩ	4.719V
5.00V	47.5 kΩ	15.0 kΩ	5.000V

ENABLE INPUT OPERATION

The Enable pin (EN) is pulled high internally by a 2 µA (typical) current source from the IN pin, and clamped at 4.9V (typical) by a zener. Pulling the EN pin low will turn the output off.

LLP THERMAL CONSIDERATIONS

The value of θ_{J-A} for the LLP package is specifically dependent on PCB copper area, copper thickness, the number of layers, and thermal vias under the exposed thermal pad (DAP). Please refer to AN-1520 (Literature Number: SNVA183A) for general guidelines for mounting packages with exposed thermal pads.

Exceeding the maximum allowable power dissipation defined by the final θ_{J-A} will cause excessive die temperature, and the regulator may go into thermal shutdown.

Note that Thermal Shutdown is provided as a safety feature and is outside the guaranteed Operating Ratings temperature range. Operation with a junction temperature (T_J) above 125°C is not recommended as device behavior is not guaranteed.

PRODUCT PREVIEW

MOUNTING THE LLP PACKAGE

The SDA12B (No Pullback) 12-Lead LLP package requires specific mounting techniques that are detailed in AN-1187 (Literature Number: snoa401q). Referring to the section ***PCB Design Recommendations*** in AN-1187 (Page 5), it should be noted that the pad style that should be used with the SDA12B LLP package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The thermal dissipation of the LLP package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the LLP package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the twelve pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device leads 6 and 7 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP38788 in the SDA12B 12-Lead LLP package, the junction-to-case thermal resistance rating, θ_{JC}, is 5°C/W, where the case is on the bottom of the package at the center of the DAP.

The junction-to-ambient thermal performance for the LP38788SD in the SDA12B 12-Lead LLP package, using the JEDEC JESD51 standards, is summarized in the following table:

LP38788SD-ADJ (LLP-12) Thermal Performance				
Board Type	**Thermal Vias**	**θ_{JA}**	**PSI_{JB}**	**θ_{JC}**
JEDEC 2-Layer JESD 51-3	None	138°C/W	45.9°C/W	5°C/W
JEDEC 4-Layer JESD 51-7	1	51°C/W	26.1°C/W	5°C/W
	2	45°C/W	24.7°C/W	
	4	39°C/W	18.0°C/W	
	6	36°C/W	14.9°C/W	
	8	34°C/W	13.2°C/W	

PRODUCT PREVIEW

Typical Applications

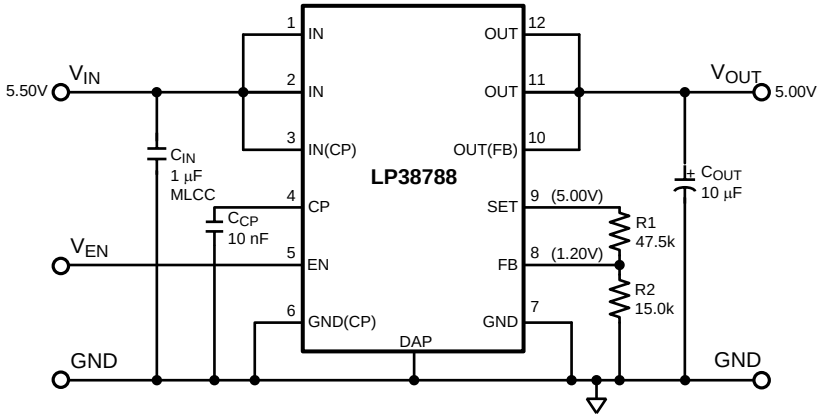


Figure 2. Typical Application, V_{OUT}= 5.0V

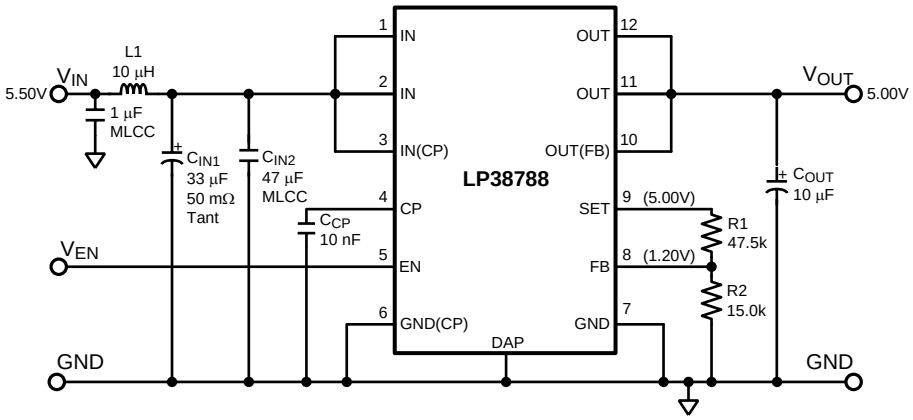


Figure 3. Improving PSRR at High Frequencies

PRODUCT PREVIEW

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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