01 CHANGE HISTORY

Date	Editor	Page	Content
20200117	Lu Yueqiang		V1 was done.

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02 DIAGRAM

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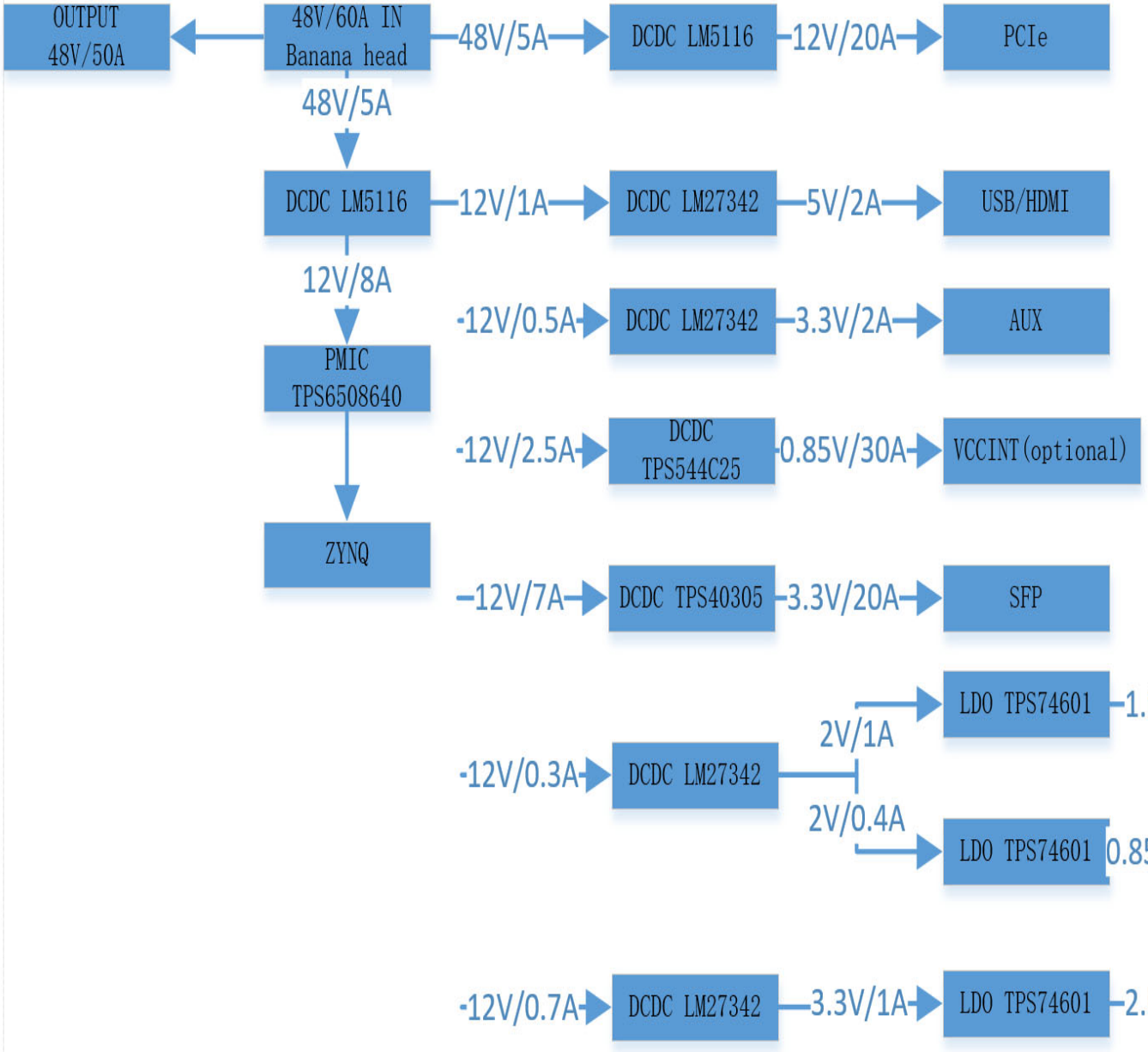
03 POWER TREE



电源合并后

时序	电压网络名称	电压大小	电流（mA）	功率(mW)	总功率（W）
0	VCC_12V0	12			
1	VCC_0V85_BUCK2	0.85	58000	49300	
4	VCC_1V8_BUCK5	1.8	3600	6480	
3	VCC_0V85_VPS_MGTRAVCC	0.85	400	340	
7	VCC_1V2_BUCK6	1.2	1948	2337.6	
3	VCC_1V2_BUCK3	1.2	6200	7440	
5	VCC_1V8_SWB1	1.8	1100	1980	
2	VCC_0V9_BUCK4	0.9	6000	5400	
6	VCC_3V3_SWA1	3.3	600	1980	168.4819
8	VCC_1V8_IO	1.8	4000	7200	
8	VCC_1V2_IO	1.2	0	0	
7	VCC_2V5_DDR	2.5	664	1660	
7	VCC_0V6_DDRVTT	0.6	2000	1200	
1	VCC_3V3_AUX	3.3	1896	6256.8	
8	VCC_1V1_AUX	1.1	825	907.5	
8	VCC_5V_AUX	5	2000	10000	
8	VCC_3V3_SFP	3.3	20000	66000	

NOTE:
1、如果PCIe要用，需要增加12V/20A电源,其他12V/15电流为用于向下级转换的电流，加上转换效率后为12V/40A，再加上80%余量设计，12V需要50A以上MOS；
2、如果SFP要用，需要增加3.3V/20A电源，可以额外增加一个电源芯片用于其的供电；
3、上电时序主要是根据PMIC TPS6508640的时序来确定SOC的时序，另外SYS MCU的上电要优先，用于控制系统上电，其他外设电最后上电即可放到第8优先级。

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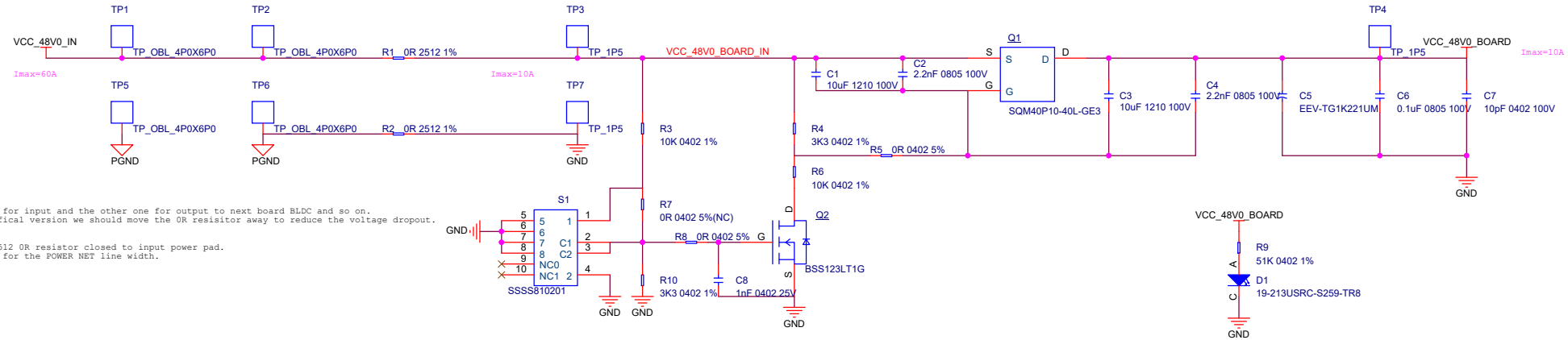
04 POWER INPUT & SWITCH



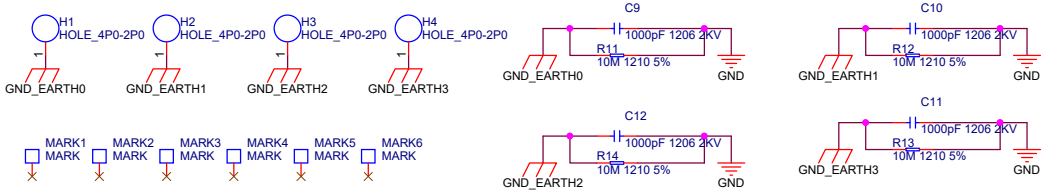
NOTE:
SCH:
1. One pair for input and the other one for output to next board BLDC and so on.
2.In the offical version we should move the 0R resisitor away to reduce the voltage dropout.

PCB:
1.Put the 2512 0R resistor closed to input power pad.
2.Watch out for the POWER NET line width.

NOTE:
SCH:
1.Mass production version the Swtich should be taken away.
2.To match the NMOS and PMOS Vgs<20V, here we need two resistors devider.

NOTE:
SCH:
1.Power good indication.

MARKS & HOLES



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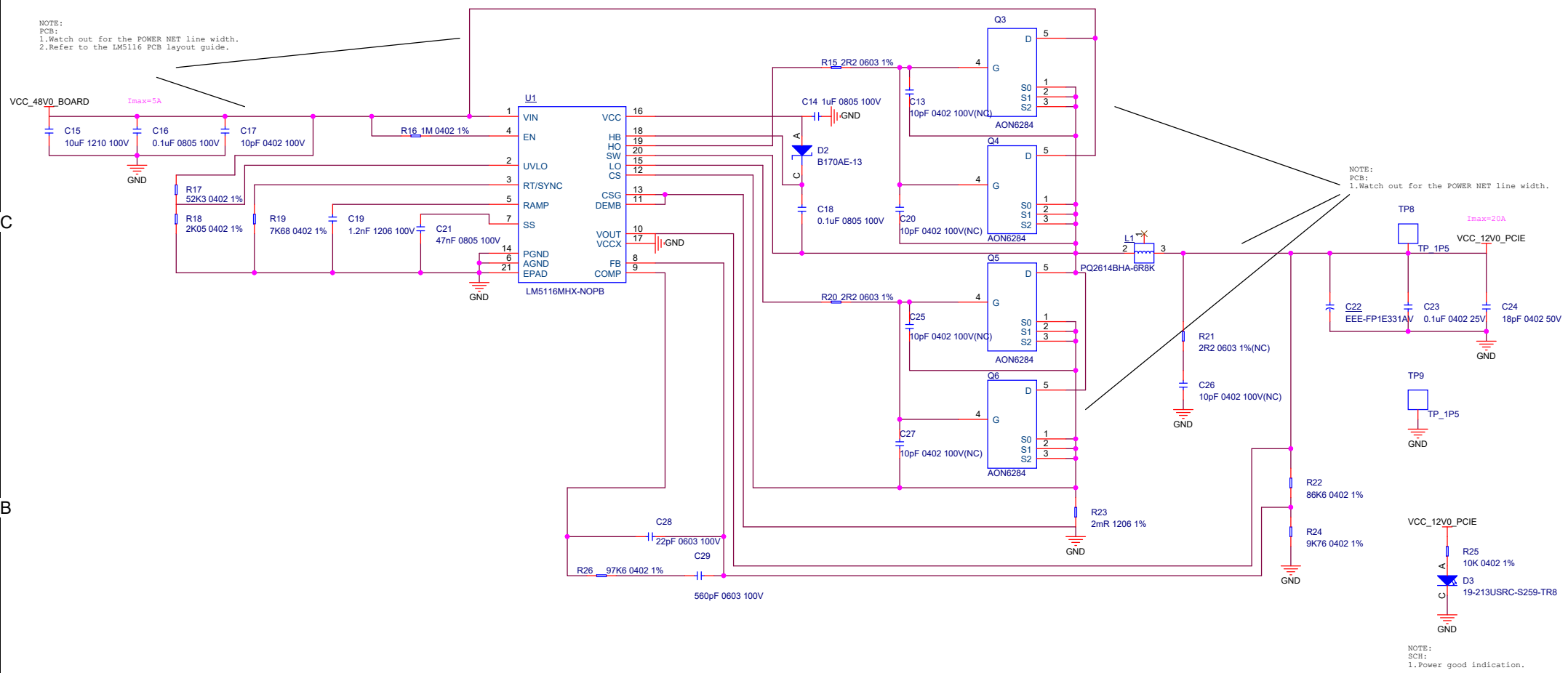
05 POWER LM5116 VCC_12V0_PCIE



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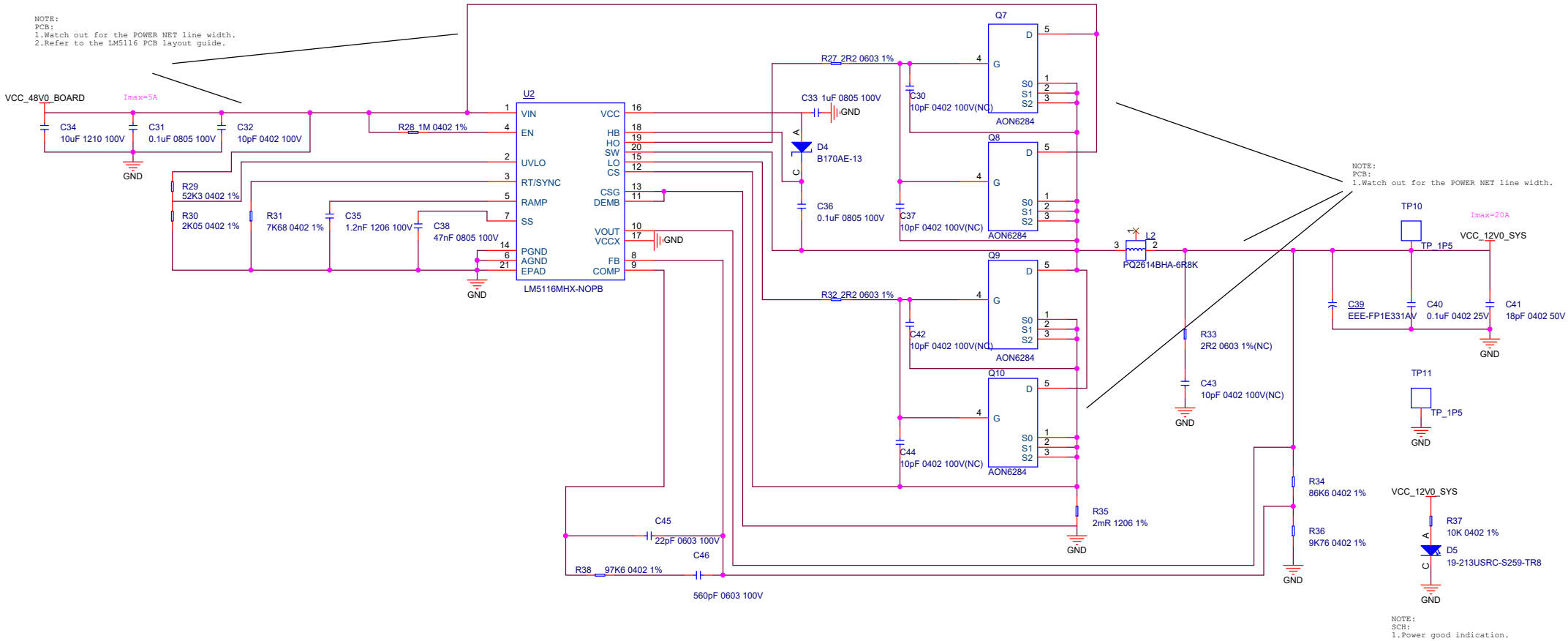
06 POWER LM5116 VCC_12V0_SYS



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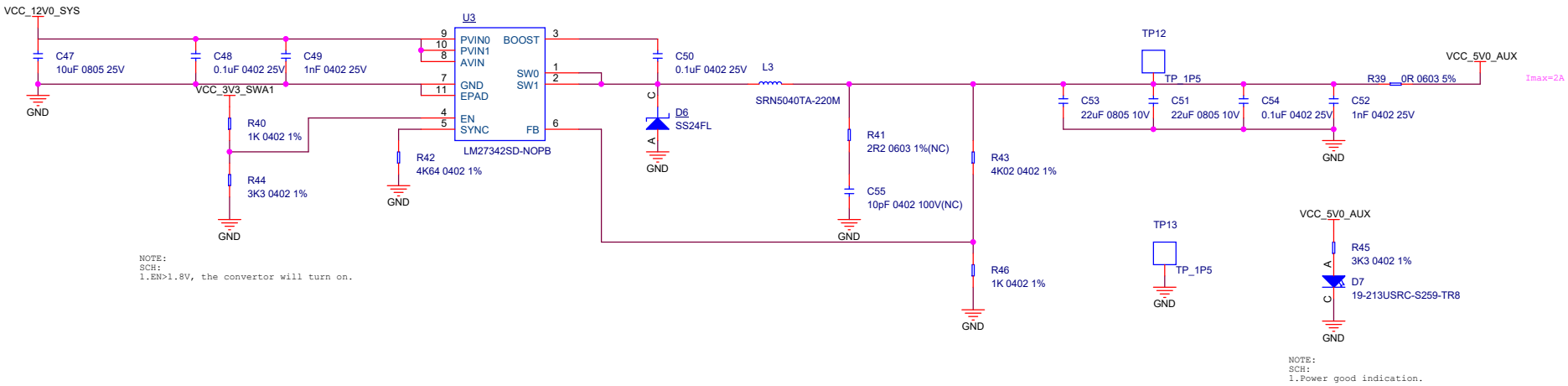
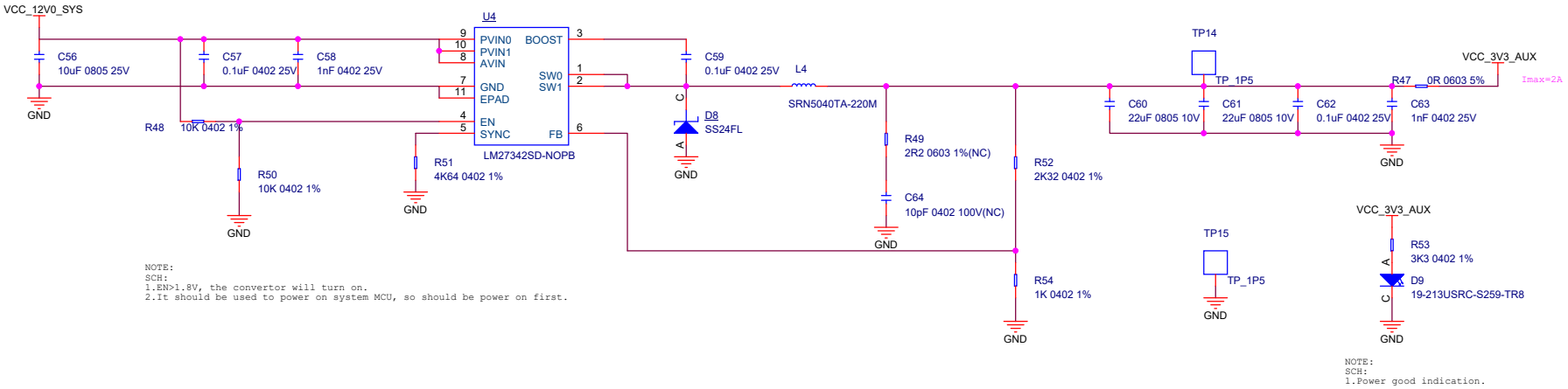
07 POWER LM27342 VCC_5V/3V3_AUX





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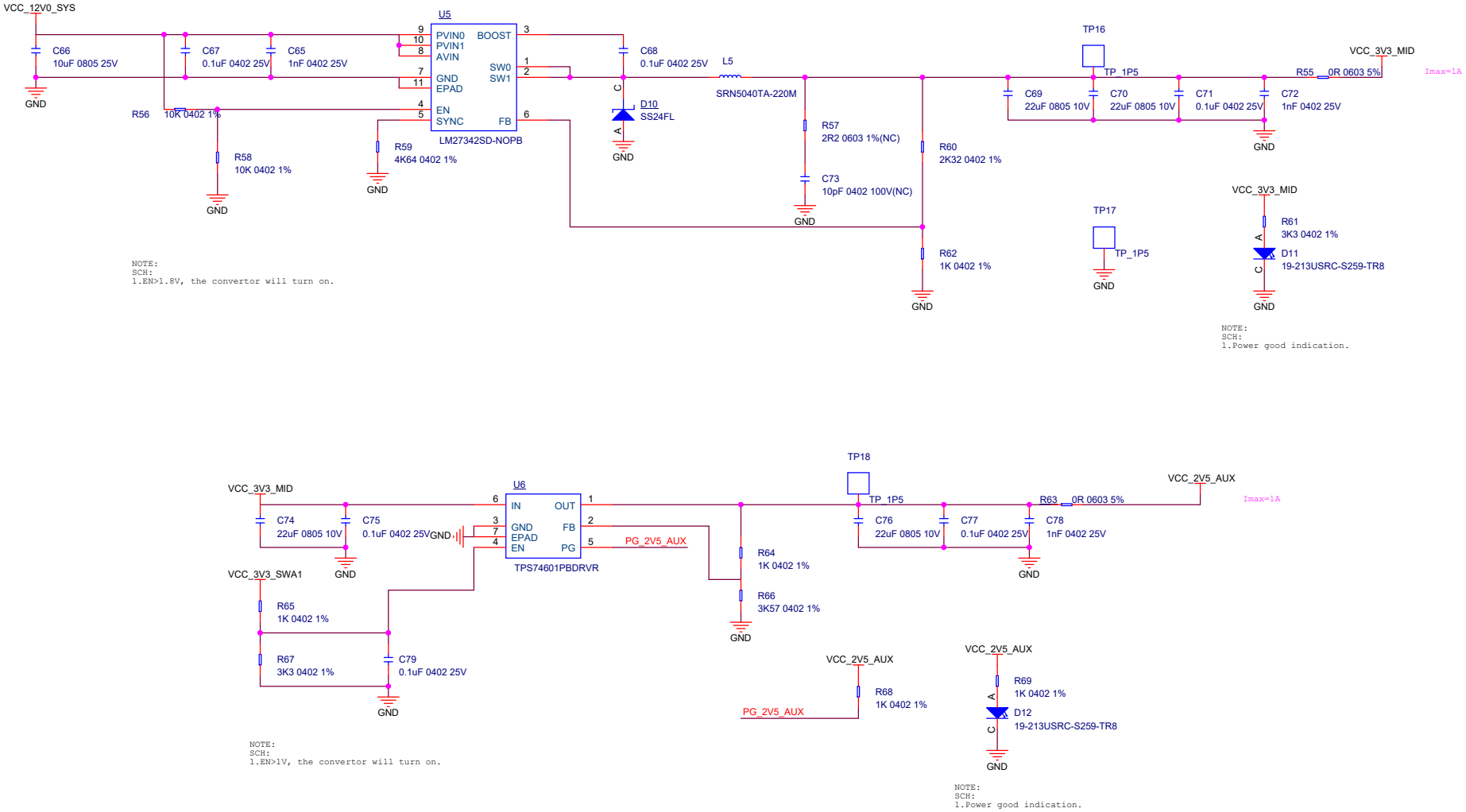
08 POWER 2V5_AUX



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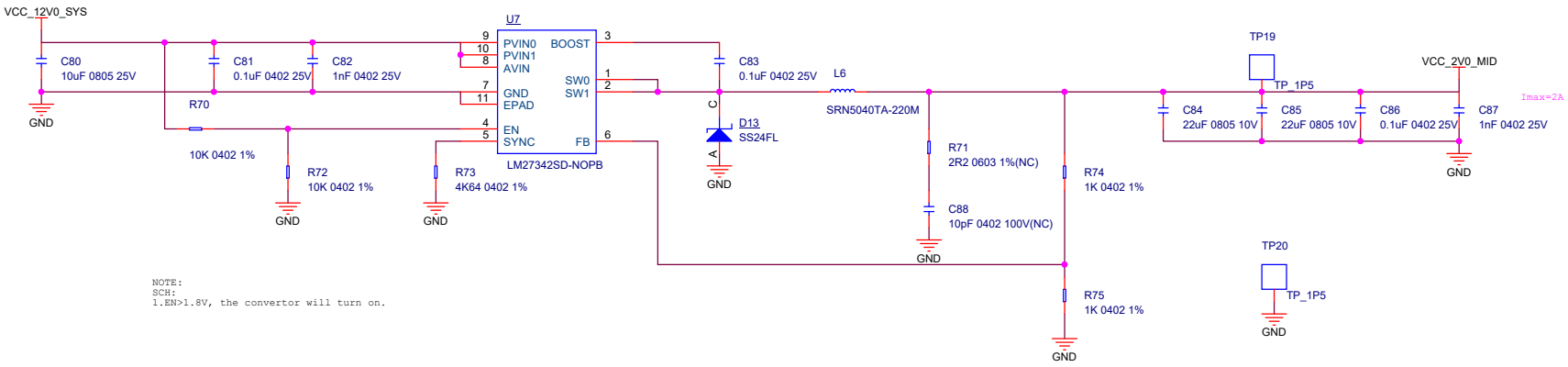
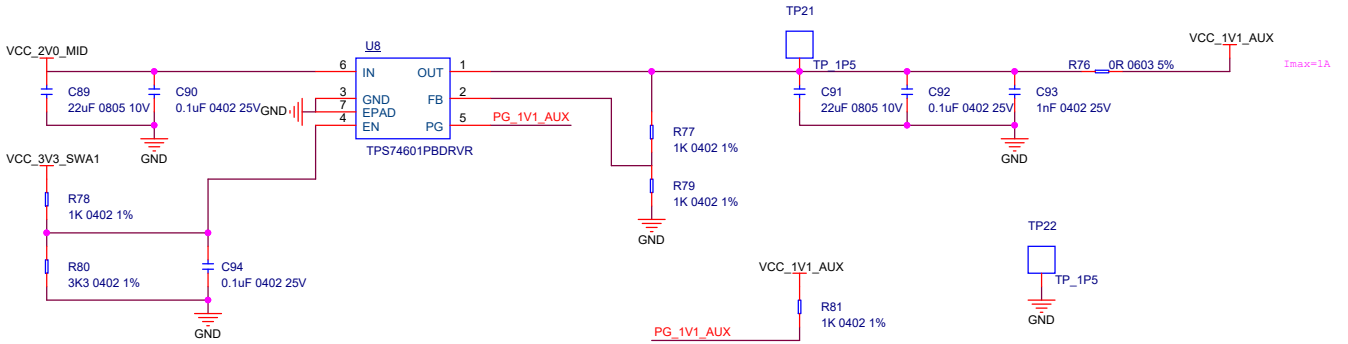
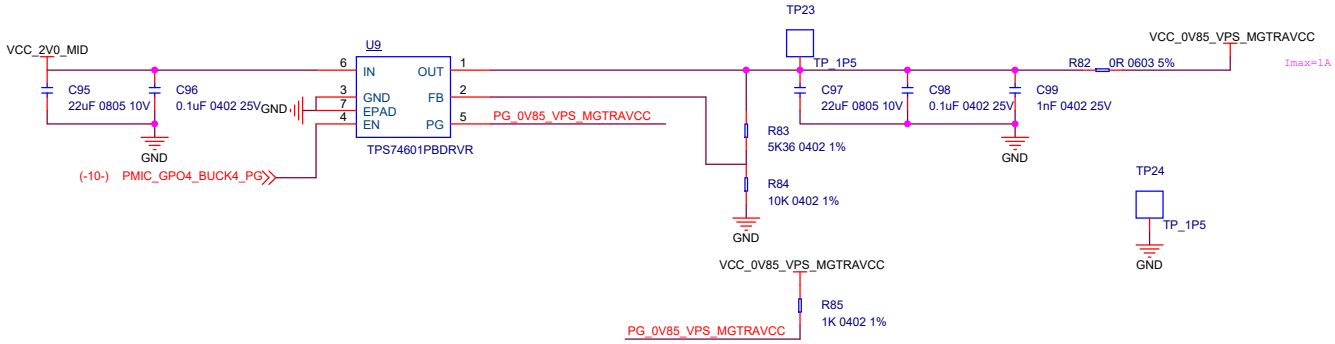
09 POWER 1V1_AUX & 0V85



NOTE:
SCH:
1.EN>1.8V, the convertor will turn on.



NOTE:
SCH:
1.EN>1V, the convertor will turn on.
2.After VCC_PSIO power on, the AUX VCC will powen on.



NOTE:
SCH:
1.EN>1V, the convertor will turn on.
2.After VPS_MGTRAVCC power on, the VPS_MGTRAVTT will powen on.

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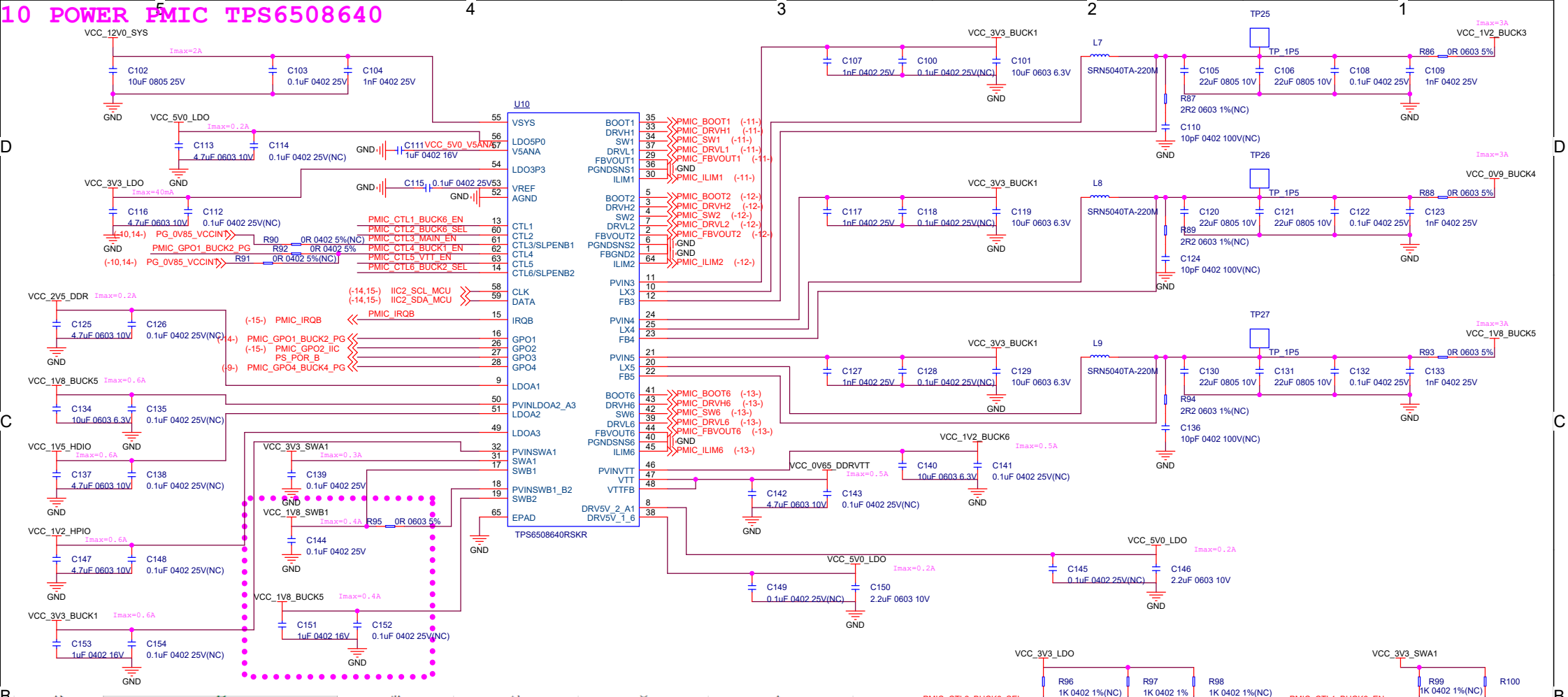
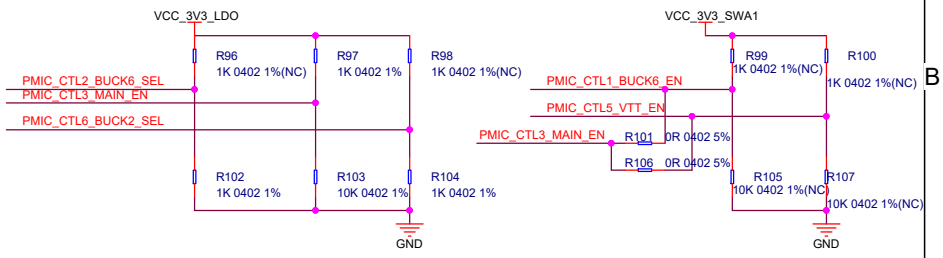
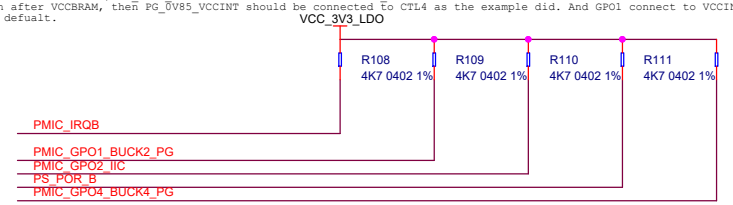
10 POWER PMIC TPS6508640





NOTE:
SCH:
1.If we don't use VCCINT seperately, we should leave PG_0V85_VCCINT alone, don't use it. But connect GPO1 to CTL4.
2.If we use VCCINT seperately. Then as below:
1)If VCCINT power on before VCCBRAM, PG_0V85_VCCINT should connected to PMIC_CTL3 to controll the whole PMIC;
2)If VCCINT power on after VCCBRAM, then PG_0V85_VCCINT should be connected to CTL4 as the example did. And GPO1 connect to VCCINT's CNTL.
3)We designed as 2) defualt.



电源合并后

时序	电压网络名称	电压大小	电流（mA）	功率(mW)	总功率（W）
0	VCC_12V0	12			
1	VCC_0V85_BUCK2	0.85	58000	49300	
4	VCC_1V8_BUCK5	1.8	3600	6480	
3	VCC_0V85_VPS_MGTRAVCC	0.85	400	340	
7	VCC_1V2_BUCK6	1.2	1948	2337.6	
3	VCC_1V2_BUCK3	1.2	6200	7440	
5	VCC_1V8_SWB1	1.8	1100	1980	
2	VCC_0V9_BUCK4	0.9	6000	5400	
6	VCC_3V3_SWA1	3.3	600	1980	168.4819
8	VCC_1V8_IO	1.8	4000	7200	
8	VCC_1V2_IO	1.2	0	0	
7	VCC_2V5_DDR	2.5	664	1660	
7	VCC_0V6_DDRVTT	0.6	2000	1200	
1	VCC_3V3_AUX	3.3	1896	6256.8	
8	VCC_1V1_AUX	1.1	825	907.5	
8	VCC_5V_AUX	5	2000	10000	
8	VCC_3V3_SFP	3.3	20000	66000	

NOTE：
1、 如果PCIe要用， 需要增加12V/20A电源，其他12V/15电流为用于向下级转换的电流， 加上转换效率后为12V/40A， 再加上80%余量设计， 12V需要50A以上MOS；
2、 如果SFP要用， 需要增加3.3V/20A电源， 可以额外增加一个电源芯片用于其的供电；
3、 上电时序主要是根据PMIC TPS6508640的时序来确定SOC的时序， 另外SYS MCU的上电要优先，用于控制系统上电， 其他外设电最后上电即可放到第8优先级。

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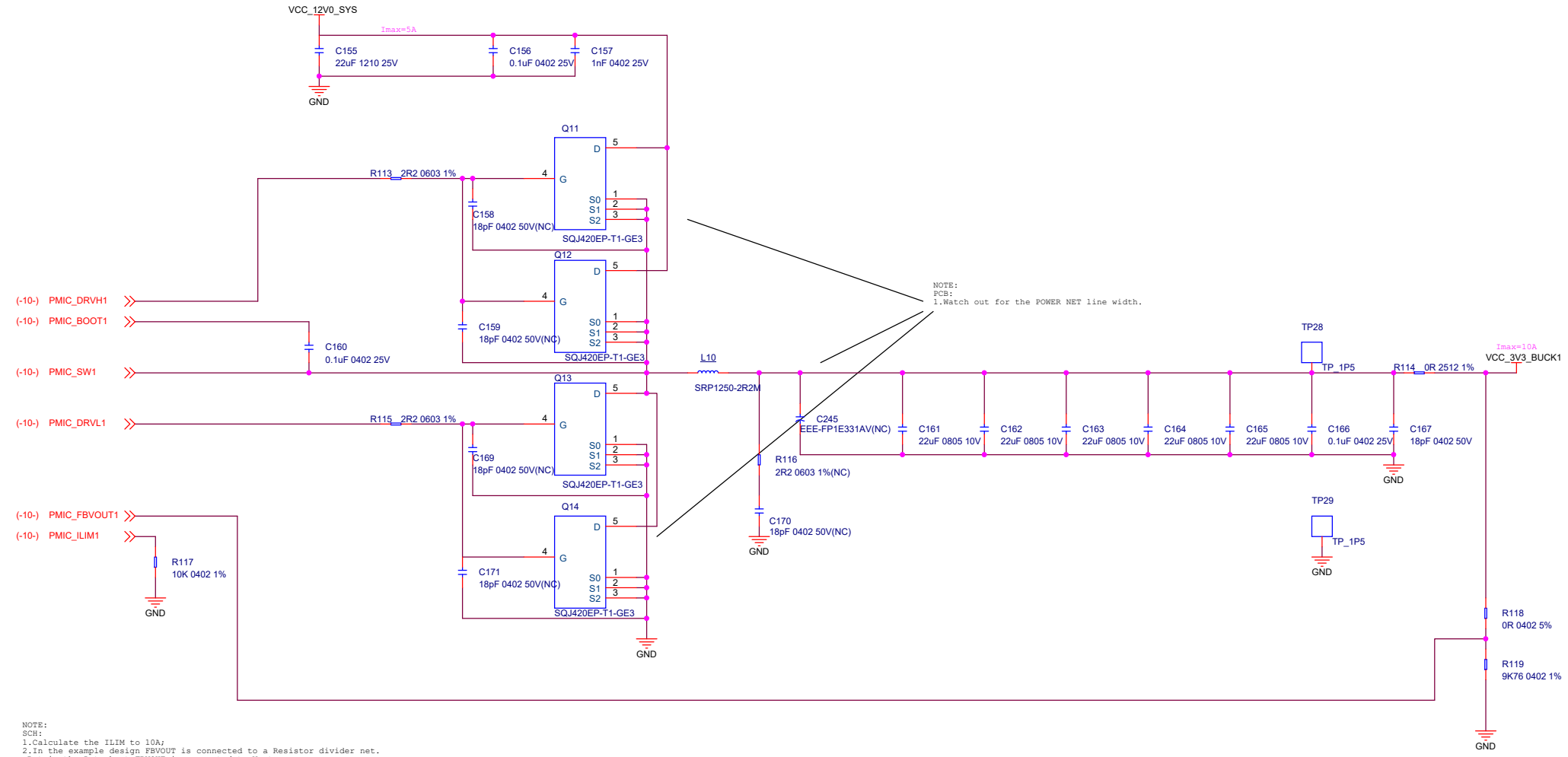
11 POWER PMIC VCC_3V3_BUCK1



NOTE:
SCH:
1.Calculate the ILIM to 10A;
2.In the example design FBVOUT is connected to a Resistor divider net.
But in the Datasheet FBVOUT is connected to Vout.
3.In the offical version we should move the 0R resisitor away to reduce the voltage dropout.

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12 POWER PMIC VCC_0V85_BUCK2

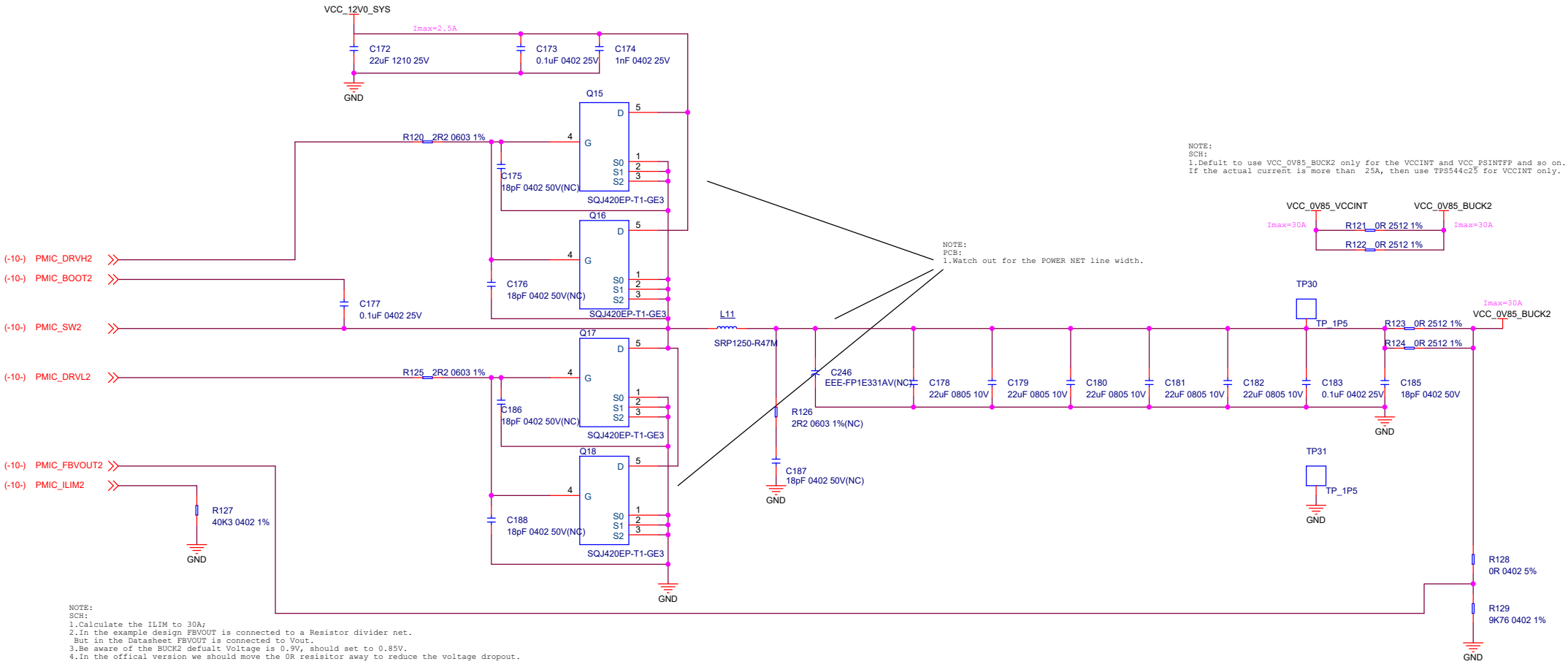

Table 6-2. TPS6508640 Settings Summary—Buck Regulators

REGULATOR	DEFAULT VOLTAGE	SLEEP VOLTAGE	STEP SIZE	SLP PIN	SLP_EN	POWER FAULT MASKED	FORCE PWM
BUCK1	3.3 V	3.3 V	25 mV	CTL6	No	No	Yes
BUCK2	0.9 V	0.85 V	10 mV	CTL6	Yes	No	Yes
BUCK3	1.2 V	1.2 V	25 mV	CTL6	Yes	No	Yes
BUCK4	0.9 V	0.9 V	25 mV	CTL6	No	No	Yes
BUCK5	1.8 V	1.8 V	25 mV	CTL6	No	No	Yes
BUCK6	1.35 V / 1.2 V	1.35	10 mV	CTL2 & CTL6	No	No	Yes

Table 6-3. TPS6508640 Settings Summary—General Purpose LDOs

REGULATOR	DEFAULT VOLTAGE	SLEEP VOLTAGE	ALWAYS ON	SLP PIN	SLP_EN	POWER FAULT MASKED
LDOA1	2.5 V	—	No	—	—	No
LDOA2	1.5 V	1.5 V	No	CTL6	No	Yes
LDOA3	1.2 V	1.2 V	No	CTL6	No	Yes

Table 6-4. TPS6508640 Settings Summary—VTT LDO

REGULATOR	ILIM SETTING	ENABLE PIN	POWER FAULT MASKED
VTT LDO	1.8 A	CTL3	No

Table 6-5. TPS6508640 Settings Summary—Load Switches

REGULATOR	POWER GOOD VOLTAGE	SWB1_2 MERGED	POWER FAULT MASKED
SWA1	3.3 V	—	Yes
SWB1	1.8 V	No	Yes
SWB2	1.8 V	No	Yes

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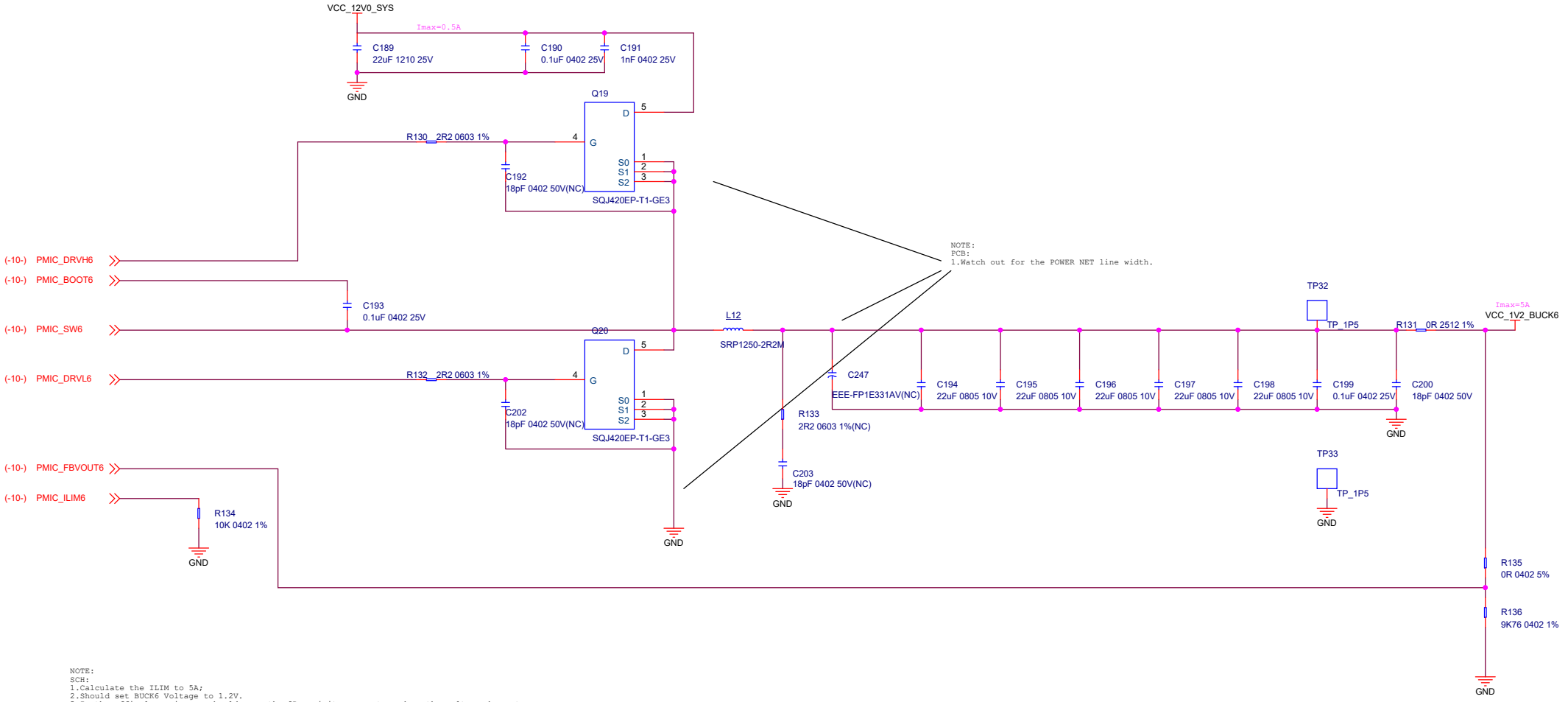
13 POWER PMIC VCC_1V2_BUCK6



NOTE:
SCH:
1.Calculate the ILIM to 5A;
2.Should set BUCK6 Voltage to 1.2V.
3.In the offical version we should move the 0R resisitor away to reduce the voltage dropout.

Table 6-2. TPS6508640 Settings Summary—Buck Regulators

REGULATOR	DEFAULT VOLTAGE	SLEEP VOLTAGE	STEP SIZE	SLP PIN	SLP_EN	POWER FAULT MASKED	FORCE PWM
BUCK1	3.3 V	3.3 V	25 mV	CTL6	No	No	Yes
BUCK2	0.9 V	0.85 V	10 mV	CTL6	Yes	No	Yes
BUCK3	1.2 V	1.2 V	25 mV	CTL6	Yes	No	Yes
BUCK4	0.9 V	0.9 V	25 mV	CTL6	No	No	Yes
BUCK5	1.8 V	1.8 V	25 mV	CTL6	No	No	Yes
BUCK6	1.35 V / 1.2 V	1.35	10 mV	CTL2 & CTL6	No	No	Yes

Table 6-3. TPS6508640 Settings Summary—General Purpose LDOs

REGULATOR	DEFAULT VOLTAGE	SLEEP VOLTAGE	ALWAYS ON	SLP PIN	SLP_EN	POWER FAULT MASKED
LDOA1	2.5 V	—	No	—	—	No
LDOA2	1.5 V	1.5 V	No	CTL6	No	Yes
LDOA3	1.2 V	1.2 V	No	CTL6	No	Yes

Table 6-4. TPS6508640 Settings Summary—VTT LDO

REGULATOR	ILIM SETTING	ENABLE PIN	POWER FAULT MASKED
VTT LDO	1.8 A	CTL3	No

Table 6-5. TPS6508640 Settings Summary—Load Switches

REGULATOR	POWER GOOD VOLTAGE	SWB1_2 MERGED	POWER FAULT MASKED
SWA1	3.3 V	—	Yes
SWB1	1.8 V	No	Yes
SWB2	1.8 V	No	Yes

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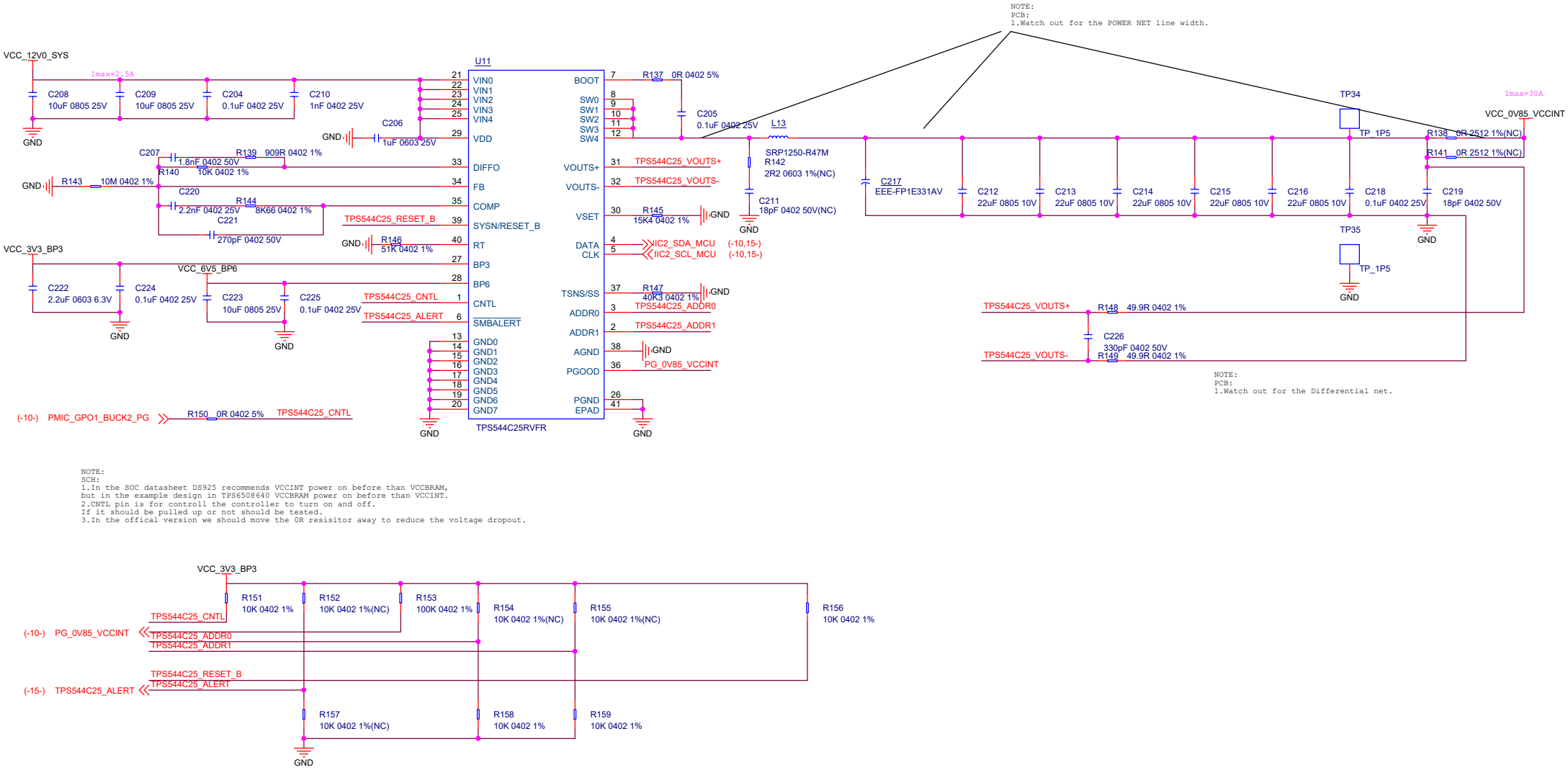
14 POWER VCC_0V85_VCCINT



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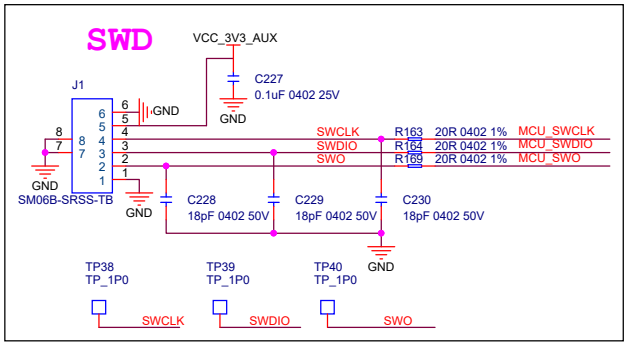
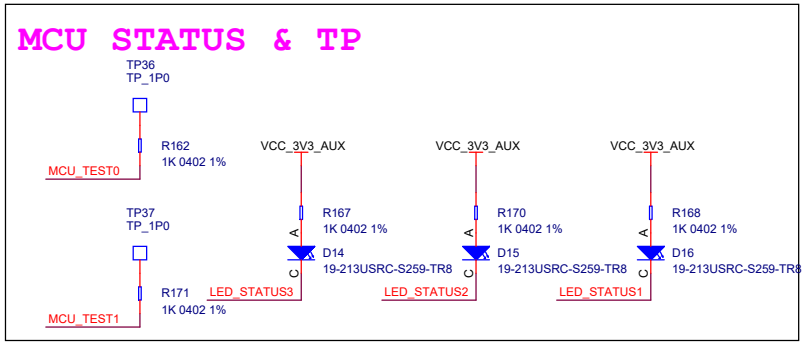
15 SYS MCU STM32F407

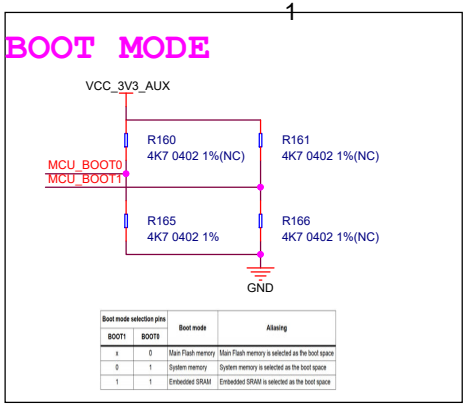
SWD



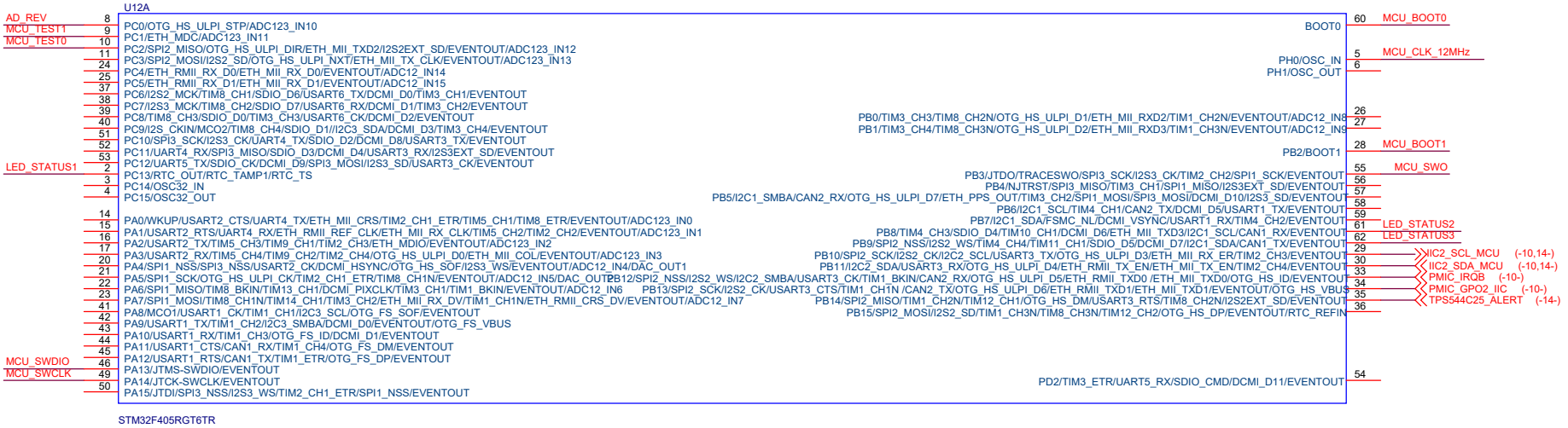
MCU STATUS & TP

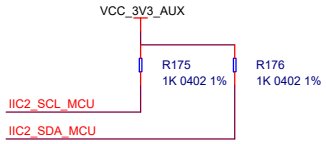


BOOT MODE



U12A





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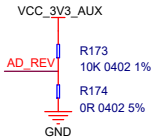
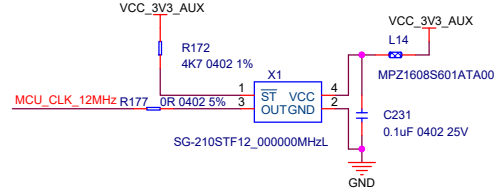


Note
SCH:
1.0.3v for one version for ADC.

CLOCK



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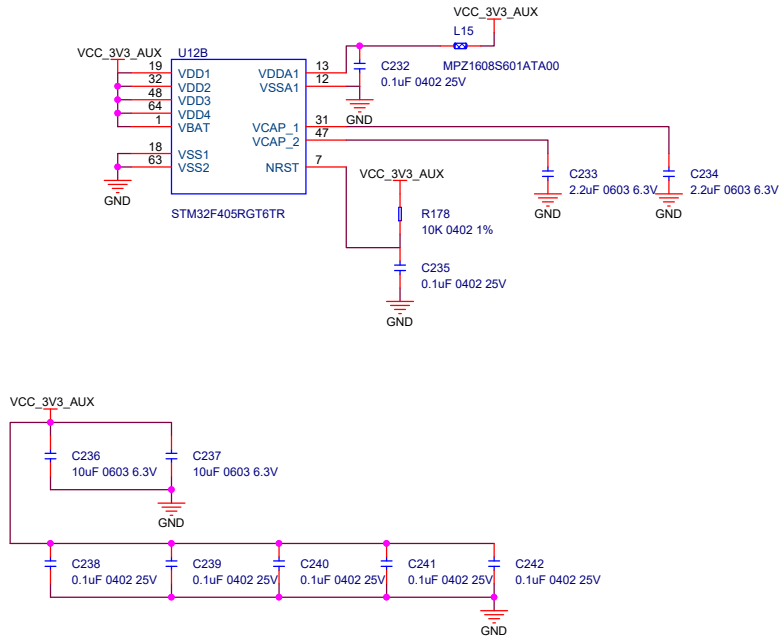
16 SYS MCU POWER



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