TPS65913 and TPS65914 Register Mapping

User's Guide

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Register Mapping

1.1 FUNC_SMPS_DVS Registers

1.1.1 FUNC_SMPS_DVS Registers Mapping Summary

This section provides information on the FUNC_SMPS_DVS Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.1.1.1 FUNC_SMPS_DVS Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
SMPS12_FORCE	RW	8	0b1xxx xxxx	0x12	0x02	0x022
SMPS12_VOLTAGE	RW	8	0xXX	0x12	0x03	0x023
SMPS45_FORCE	RW	8	0b1xxx xxxx	0x12	0x0A	0x02A
SMPS45_VOLTAGE	RW	8	0xXX	0x12	0x0B	0x02B
SMPS6_FORCE	RW	8	0b1xxx xxxx	0x12	0x0E	0x02E
SMPS6_VOLTAGE	RW	8	0xXX	0x12	0x0F	0x02F
SMPS8_FORCE	RW	8	0b1xxx xxxx	0x12	0x16	0x036
SMPS8_VOLTAGE	RW	8	0xXX	0x12	0x17	0x037

1.1.2 FUNC_SMPS_DVS Register Descriptions

1.1.2.1 SMPS12_FORCE Register

Table 1-1. SMPS12_FORCE

Address offset	0x02	**I2C Address**	0x12
Physical Address	0x022 **Instance**	FUNC_SMPS_DVS	
Description	SMPS12 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config). RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
CMD	VSEL						

Bits	Field Name	Description	Type	Reset
7	CMD	DVS command register selection: When 0: SMPS12_FORCE.VSEL voltage is applied When 1: SMPS12_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS12_CTRL.ROOF_FLOOR_EN='0'	RW	1
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).	RW	0bxxx xxxx

1.1.2.2 SMPS12_VOLTAGE Register

Table 1-2. SMPS12_VOLTAGE

Address offset	0x03			**I2C Address**	0x12
Physical Address	0x023	**Instance**		FUNC_SMPS_DVS	
Description	SMPS12 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS12_VOLTAGE.VSEL and SPMS12_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).	RW	0bxxx xxxx

1.1.2.3 SMPS45_FORCE Register

Table 1-3. SMPS45_FORCE

Address offset	0x0A			**I2C Address**	0x12
Physical Address	0x02A	**Instance**		FUNC_SMPS_DVS	
Description	SMPS45 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
CMD	VSEL						

Bits	Field Name	Description	Type	Reset
7	CMD	DVS command register selection: When 0: SMPS45_FORCE.VSEL voltage is applied When 1: SMPS45_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS45_CTRL.ROOF_FLOOR_EN='0'	RW	1
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).	RW	0bxxx xxxx

1.1.2.4 SMPS45_VOLTAGE Register

Table 1-4. SMPS45_VOLTAGE

Address offset	0x0B			**I2C Address**	0x12
Physical Address	0x02B	**Instance**		FUNC_SMPS_DVS	
Description	SMPS45 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS45_VOLTAGE.VSEL and SPMS45_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).	RW	0bxxx xxxx

1.1.2.5 SMPS6_FORCE Register

Table 1-5. SMPS6_FORCE

Address offset	0x0E			**I2C Address**	0x12
Physical Address	0x02E	**Instance**		FUNC_SMPS_DVS	
Description	SMPS6 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
CMD	VSEL						

Bits	Field Name	Description	Type	Reset
7	CMD	DVS command register selection: When 0: SMPS6_FORCE.VSEL voltage is applied When 1: SMPS6_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS6_CTRL.ROOF_FLOOR_EN='0'	RW	1
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).	RW	0bxxx xxxx

1.1.2.6 SMPS6_VOLTAGE Register

Table 1-6. SMPS6_VOLTAGE

Address offset	0x0F	**I2C Address**	0x12
Physical Address	0x02F **Instance**	FUNC_SMPS_DVS	
Description	SMPS6 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS6_VOLTAGE.VSEL and SPMS6_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).	RW	0bxxx xxxx

1.1.2.7 SMPS8_FORCE Register

Table 1-7. SMPS8_FORCE

Address offset	0x16	**I2C Address**	0x12
Physical Address	0x036 **Instance**	FUNC_SMPS_DVS	
Description	SMPS8 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config). RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
CMD	VSEL						

Bits	Field Name	Description	Type	Reset
7	CMD	DVS command register selection: When 0: SMPS8_FORCE.VSEL voltage is applied When 1: SMPS8_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS8_CTRL.ROOF_FLOOR_EN='0'	RW	1
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).	RW	0bxxx xxxx

1.1.2.8 SMPS8_VOLTAGE Register

Table 1-8. SMPS8_VOLTAGE

Address offset	0x17			**I2C Address**	0x12
Physical Address	0x037	**Instance**		FUNC_SMPS_DVS	
Description	SMPS8 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS8_VOLTAGE.VSEL and SPMS8_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).	RW	0bxxx xxxx

1.2 FUNC_RTC Registers

1.2.1 FUNC_RTC Registers Mapping Summary

This section provides information on the FUNC_RTC Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.2.1.1 FUNC_RTC Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
SECONDS_REG	RW	8	0x00	0x48	0x00	0x100
MINUTES_REG	RW	8	0x00	0x48	0x01	0x101
HOURS_REG	RW	8	0x00	0x48	0x02	0x102
DAYS_REG	RW	8	0x01	0x48	0x03	0x103
MONTHS_REG	RW	8	0x01	0x48	0x04	0x104
YEARS_REG	RW	8	0x00	0x48	0x05	0x105
WEEKS_REG	RW	8	0x00	0x48	0x06	0x106
ALARM_SECONDS_REG	RW	8	0x00	0x48	0x08	0x108
ALARM_MINUTES_REG	RW	8	0x00	0x48	0x09	0x109
ALARM_HOURS_REG	RW	8	0x00	0x48	0x0A	0x10A
ALARM_DAYS_REG	RW	8	0x01	0x48	0x0B	0x10B
ALARM_MONTHS_REG	RW	8	0x01	0x48	0x0C	0x10C
ALARM_YEARS_REG	RW	8	0x00	0x48	0x0D	0x10D
RTC_CTRL_REG	RW	8	0x00	0x48	0x10	0x110
RTC_STATUS_REG	RW	8	0x80	0x48	0x11	0x111
RTC_INTERRUPTS_REG	RW	8	0x00	0x48	0x12	0x112
RTC_COMP_LSB_REG	RW	8	0x00	0x48	0x13	0x113
RTC_COMP_MSB_REG	RW	8	0x00	0x48	0x14	0x114
RTC_RES_PROG_REG	RW	8	0x27	0x48	0x15	0x115
RTC_RESET_STATUS_REG	RW	8	0x00	0x48	0x16	0x116

1.2.2 FUNC_RTC Register Descriptions

1.2.2.1 SECONDS_REG Register

Table 1-9. SECONDS_REG

Address offset	0x00	**I2C Address**	0x48
Physical Address	0x100 **Instance**	FUNC_RTC	
Description	RTC register for seconds RESET register domain: POR MSECURE register protected : Yes		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEC1			SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO Rreturns0 s	0
6:4	SEC1	Second digit of seconds (range is 0 up to 5)	RW	0x0
3:0	SEC0	First digit of seconds (range is 0 up to 9)	RW	0x0

1.2.2.2 MINUTES_REG Register

Table 1-10. MINUTES_REG

Address offset	0x01	**I2C Address**	0x48
Physical Address	0x101 **Instance**	FUNC_RTC	
Description	RTC register for minutes RESET register domain: POR MSECURE register protected : Yes		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	MIN1			MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO Rreturns0 s	0
6:4	MIN1	Second digit of minutes (range is 0 up to 5)	RW	0x0
3:0	MIN0	First digit of minutes (range is 0 up to 9)	RW	0x0

1.2.2.3 HOURS_REG Register

Table 1-11. HOURS_REG

Address offset	0x02			**I2C Address**	0x48
Physical Address	0x102	**Instance**		FUNC_RTC	
Description	RTC register for hours RESET register domain: POR MSECURE register protected : Yes				
Type	RW				

7	6	5	4	3	2	1	0
PM_NAM	Reserved	HOUR1		HOUR0			

Bits	Field Name	Description	Type	Reset
7	PM_NAM	Only used in PM_AM mode (otherwise it is set to 0) 0 is AM 1 is PM	RW	0
6	Reserved	Reserved bit	RO Rreturns0 s	0
5:4	HOUR1	Second digit of hours(range is 0 up to 2)	RW	0x0
3:0	HOUR0	First digit of hours (range is 0 up to 9)	RW	0x0

1.2.2.4 DAYS_REG Register

Table 1-12. DAYS_REG

Address offset	0x03			**I2C Address**	0x48
Physical Address	0x103	**Instance**		FUNC_RTC	
Description	RTC register for days RESET register domain: POR MSECURE register protected : Yes				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		DAY1		DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO Rreturns0 s	0x0
5:4	DAY1	Second digit of days (range is 0 up to 3)	RW	0x0
3:0	DAY0	First digit of days (range is 0 up to 9)	RW	0x1

1.2.2.5 MONTHS_REG Register

Table 1-13. MONTHS_REG

Address offset	0x04			**I2C Address**	0x48
Physical Address	0x104	**Instance**		FUNC_RTC	
Description	RTC register for months RESET register domain: POR MSECURE register protected : Yes				
Type	RW				

7	6	5	4	3	2	1	0
Reserved			MONTH1	MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO Rreturns0 s	0x0
4	MONTH1	Second digit of months (range is 0 up to 1)	RW	0
3:0	MONTH0	First digit of months (range is 0 up to 9)	RW	0x1

1.2.2.6 YEARS_REG Register

Table 1-14. YEARS_REG

Address offset	0x05			**I2C Address**	0x48
Physical Address	0x105	**Instance**		FUNC_RTC	
Description	RTC register for years RESET register domain: POR MSECURE register protected : Yes				
Type	RW				

7	6	5	4	3	2	1	0
YEAR1				YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	YEAR1	Second digit of years (range is 0 up to 9)	RW	0x0
3:0	YEAR0	First digit of years (range is 0 up to 9)	RW	0x0

1.2.2.7 WEEKS_REG Register

Table 1-15. WEEKS_REG

Address offset	0x06			**I2C Address**	0x48
Physical Address	0x106	**Instance**		FUNC_RTC	
Description	RTC register for day of the week RESET register domain: POR MSECURE register protected : Yes				
Type	RW				

7	6	5	4	3	2	1	0
Reserved						WEEK	

Bits	Field Name	Description	Type	Reset
7:3	Reserved	Reserved bit	RO Rreturns0 s	0x00
2:0	WEEK	First digit of day of the week (range is 0 up to 6)	RW	0x0

1.2.2.8 ALARM_SECONDS_REG Register

Table 1-16. ALARM_SECONDS_REG

Address offset	0x08		**I2C Address**	0x48	
Physical Address	0x108	**Instance**	FUNC_RTC		
Description	RTC register for alarm programmation for seconds RESET register domain: POR MSECURE register protected : No				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	ALARM_SEC1			ALARM_SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO Rreturns0 s	0
6:4	ALARM_SEC1	Second digit of alarm programmation for seconds (range is 0 up to 5)	RW	0x0
3:0	ALARM_SEC0	First digit of alarm programmation for seconds (range is 0 up to 9)	RW	0x0

1.2.2.9 ALARM_MINUTES_REG Register

Table 1-17. ALARM_MINUTES_REG

Address offset	0x09		**I2C Address**	0x48	
Physical Address	0x109	**Instance**	FUNC_RTC		
Description	RTC register for alarm programmation for minutes RESET register domain: POR MSECURE register protected : No				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	ALARM_MIN1			ALARM_MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO Rreturns0 s	0
6:4	ALARM_MIN1	Second digit of alarm programmation for minutes (range is 0 up to 5)	RW	0x0
3:0	ALARM_MIN0	First digit of alarm programmation for minutes (range is 0 up to 9)	RW	0x0

1.2.2.10 ALARM_HOURS_REG Register

Table 1-18. ALARM_HOURS_REG

Address offset	0x0A	**I2C Address**	0x48
Physical Address	0x10A **Instance**	FUNC_RTC	
Description	RTC register for alarm programmation for hours RESET register domain: POR MSECURE register protected : No		
Type	RW		

7	6	5	4	3	2	1	0
ALARM_PM_NAM	Reserved	ALARM_HOUR1		ALARM_HOUR0			

Bits	Field Name	Description	Type	Reset
7	ALARM_PM_NAM	Only used in PM_AM mode for alarm programmation (otherwise it is set to 0) 0 is AM 1 is PM	RW	0
6	Reserved	Reserved bit	RO Rreturns0 s	0
5:4	ALARM_HOUR1	Second digit of alarm programmation for hours(range is 0 up to 2)	RW	0x0
3:0	ALARM_HOUR0	First digit of alarm programmation for hours (range is 0 up to 9)	RW	0x0

1.2.2.11 ALARM_DAYS_REG Register

Table 1-19. ALARM_DAYS_REG

Address offset	0x0B	**I2C Address**	0x48
Physical Address	0x10B **Instance**	FUNC_RTC	
Description	RTC register for alarm programmation for days RESET register domain: POR MSECURE register protected : No		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		ALARM_DAY1		ALARM_DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO RSpecial	0x0
5:4	ALARM_DAY1	Second digit of alarm programmation for days (range is 0 up to 3)	RW	0x0
3:0	ALARM_DAY0	First digit of alarm programmation for days (range is 0 up to 9)	RW	0x1

1.2.2.12 ALARM_MONTHS_REG Register

Table 1-20. ALARM_MONTHS_REG

Address offset	0x0C			**I2C Address**	0x48
Physical Address	0x10C	**Instance**		FUNC_RTC	
Description	RTC register for alarm programmation for months RESET register domain: POR MSECURE register protected : No				
Type	RW				

7	6	5	4	3	2	1	0
Reserved			ALARM_MONTH1	ALARM_MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO Rreturns0 s	0x0
4	ALARM_MONTH1	Second digit of alarm programmation for months (range is 0 up to 1)	RW	0
3:0	ALARM_MONTH0	First digit of alarm programmation for months (range is 0 up to 9)	RW	0x1

1.2.2.13 ALARM_YEARS_REG Register

Table 1-21. ALARM_YEARS_REG

Address offset	0x0D			**I2C Address**	0x48
Physical Address	0x10D	**Instance**		FUNC_RTC	
Description	RTC register for alarm programmation for years RESET register domain: POR MSECURE register protected : No				
Type	RW				

7	6	5	4	3	2	1	0
ALARM_YEAR1				ALARM_YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	ALARM_YEAR1	Second digit of alarm programmation for years (range is 0 up to 9)	RW	0x0
3:0	ALARM_YEAR0	First digit of alarm programmation for years (range is 0 up to 9)	RW	0x0

1.2.2.14 RTC_CTRL_REG Register

Table 1-22. RTC_CTRL_REG

Address offset	0x10	**I2C Address**	0x48
Physical Address	0x110 **Instance**	FUNC_RTC	
Description	RTC control register: NOTES: A dummy read of this register is necessary before each I2C read in order to update the ROUND_30S bit value. RESET register domain: POR MSECURE register protected : Yes (excepted GET_TIME bit)		
Type	RW		

7	6	5	4	3	2	1	0
RTC_V_OPT	GET_TIME	SET_32_COUNTER	TEST_MODE	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC

Bits	Field Name	Description	Type	Reset
7	RTC_V_OPT	RTC date / time register selection: 0: Read access directly to dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG, WEEKS_REG) 1: Read access to static shadowed registers: (see GET_TIME bit).	RW	0
6	GET_TIME	When writing a 1 into this register, the content of the dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG and WEEKS_REG) is transferred into static shadowed registers. Each update of the shadowed registers needs to be done by re-asserting GET_TIME bit to 1 (i.e.: reset it to 0 and then re-write it to 1) Note: Shadowed registers, linked to the GET_TIME feature, are a parallel set of calendar static registers, at the same I2C addresses as the dynamic registers. Note: The GET_TIME feature loads the RTC counter in the shadow registers and make the content of the shadow registers available and stable for reading. Note: The GET_TIME bit has to be set to 0 and again to 1 to get a new timing value. Note: If the time reading is done without GET_TIME, the read value comes directly from the RTC counter and software has to manage the counter change during the reading. Time reading remains always at the same address, with or without using the GET_TIME feature. Note: This bit is not protected by MSECURE.	RW	0
5	SET_32_COUNTER	0: No action 1: set the 32kHz counter with RTC_COMP_MSB_REG/RTC_COMP_LSB_REG value Note: This bit must only be used when the RTC is frozen.	RW	0
4	TEST_MODE	0: functional mode 1: test mode (Auto compensation is enable when the 32kHz counter reaches at its end)	RW	0
3	MODE_12_24	0: 24 hours mode 1: 12 hours mode (PM-AM mode) Note: It is possible to switch between the two modes at any time without disturbed the RTC, read or write are always performed with the current mode.	RW	0
2	AUTO_COMP	0: No auto compensation 1: Auto compensation enabled	RW	0

Bits	Field Name	Description	Type	Reset
1	ROUND_30S	0: No update 1: When a one is written, the time is rounded to the closest minute Note: This bit is a toggle bit, the micro-controller can only write one and RTC clears it. If the micro-controller sets the ROUND_30S bit and then read it, the micro-controller will read one until the rounded to the closet minute is perform at the next second.	RW	0
0	STOP_RTC	0: RTC is frozen 1: RTC is running	RW	0

1.2.2.15 RTC_STATUS_REG Register

Table 1-23. RTC_STATUS_REG

Address offset	0x11	**I2C Address**	0x48
Physical Address	0x111 **Instance**	FUNC_RTC	
Description	RTC status register: NOTES: A dummy read of this register is necessary before each I2C read in order to update the status register value. RESET register domain: POR MSECURE register protected : No		
Type	RW		

7	6	5	4	3	2	1	0
POWER_UP	ALARM	EVENT_1D	EVENT_1H	EVENT_1M	EVENT_1S	RUN	Reserved

Bits	Field Name	Description	Type	Reset
7	POWER_UP	Indicates that a reset occurred (bit cleared to 0 by writing 1) and that RTC data are not valid anymore. Note: POWER_UP is set by a reset, is cleared by writing one in this bit. Note: The POWER_UP (RTC_STATUS_REG) and RESET_STATUS (RTC_RESET_STATUS_REG) register bits indicate the same information.	RW	1
6	ALARM	Indicates that an alarm interrupt has been generated (bit clear by writing 1). Note: The alarm interrupt keeps its low level, until the micro-controller write 1 in the ALARM bit of the RTC_STATUS_REG register. Note: The timer interrupt is a low-level pulse (15us duration).	RW	0
5	EVENT_1D	One day has occurred	RO	0
4	EVENT_1H	One hour has occurred	RO	0
3	EVENT_1M	One minute has occurred	RO	0
2	EVENT_1S	One second has occurred	RO	0
1	RUN	0: RTC is frozen 1: RTC is running Note: This bit shows the real state of the RTC, indeed because of STOP_RTC (RTC_CTRL_REG) signal was resynchronized on 32kHz clock, the action of this bit is delayed.	RO	0
0	Reserved		RO Rreturns0 s	0

1.2.2.16 RTC_INTERRUPTS_REG Register

Table 1-24. RTC_INTERRUPTS_REG

Address offset	0x12	**I2C Address**	0x48
Physical Address	0x112 **Instance**	FUNC_RTC	
Description	RTC interrupt control register RESET register domain: POR MSECURE register protected : No		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			IT_SLEEP_MASK_EN	IT_ALARM	IT_TIMER	EVERY	

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO Rreturns0 s	0x0
4	IT_SLEEP_MASK_EN	1: Mask periodic interrupt while the device is in SLEEP mode. Interrupt event is back up in a register and occurred as soon as the device is no more in SLEEP mode. 0: Normal mode, no interrupt masked	RW	0
3	IT_ALARM	Enable one interrupt when the alarm value is reached (TC ALARM registers: ALARM_SECONDS_REG, ALARM_MINUTES_REG, ALARM_HOURS_REG, ALARM_DAYS_REG, ALARM_MONTHS_REG, ALARM_YEARS_REG)) by the TC registers	RW	0
2	IT_TIMER	Enable periodic interrupt 0: interrupt disabled 1: interrupt enabled	RW	0
1:0	EVERY	Interrupt period 00: every second 01: every minute 10: every hour 11: every day	RW	0x0

1.2.2.17 RTC_COMP_LSB_REG Register

Table 1-25. RTC_COMP_LSB_REG

Address offset	0x13			**I2C Address**	0x48
Physical Address	0x113	**Instance**		FUNC_RTC	
Description	RTC compensation register (LSB) NOTES: This register must be written in 2-complement. This means that to add one 32kHz oscillator period every hour, micro-controller needs to write FFFF into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. To remove one 32kHz oscillator period every hour, micro-controller needs to write 0001 into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. The 7FFF value is forbidden. RESET register domain: POR MSECURE register protected : No				
Type	RW				

7	6	5	4	3	2	1	0
RTC_COMP_LSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_LSB	This register contains the number of 32kHz periods to be added into the 32kHz counter every hour [LSB]	RW	0x00

1.2.2.18 RTC_COMP_MSB_REG Register

Table 1-26. RTC_COMP_MSB_REG

Address offset	0x14			**I2C Address**	0x48
Physical Address	0x114	**Instance**		FUNC_RTC	
Description	RTC compensation register (MSB) NOTES: See RTC_COMP_LSB_REG Notes. RESET register domain: POR MSECURE register protected : No				
Type	RW				

7	6	5	4	3	2	1	0
RTC_COMP_MSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_MSB	This register contains the number of 32kHz periods to be added into the 32kHz counter every hour [MSB]	RW	0x00

1.2.2.19 RTC_RES_PROG_REG Register

Table 1-27. RTC_RES_PROG_REG

Address offset	0x15			**I2C Address**	0x48
Physical Address	0x115	**Instance**		FUNC_RTC	
Description	RTC register containing oscillator resistance value RESET register domain: POR MSECURE register protected : No				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		SW_RES_PROG					

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO Rreturns0 s	0x0
5:0	SW_RES_PROG	Value of the oscillator resistance	RW	0x27

1.2.2.20 RTC_RESET_STATUS_REG Register

Table 1-28. RTC_RESET_STATUS_REG

Address offset	0x16	**I2C Address**	0x48
Physical Address	0x116 **Instance**	FUNC_RTC	
Description	RTC register for reset status RESET register domain: POR MSECURE register protected : No		
Type	RW		

7	6	5	4	3	2	1	0
Reserved							RESET_STATUS

Bits	Field Name	Description	Type	Reset
7:1	Reserved	Reserved bit	RO Rreturns0 s	0x00
0	RESET_STATUS	This bit can only be set to one and is cleared when a manual reset or a POR (case of VBAT below the VBAT min) occur. If this bit is reset it means that the RTC has lost its configuration. Note: The RESET_STATUS (RTC_RESET_STATUS_REG) and POWER_UP (RTC_STATUS_REG) register bits indicate the same information.	RW	0

1.3 FUNC_BACKUP Registers

1.3.1 FUNC_BACKUP Registers Mapping Summary

This section provides information on the FUNC_BACKUP Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.3.1.1 FUNC_VALIDITY Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
BACKUP0	RW	8	0x00	0x48	0x00	0x118
BACKUP1	RW	8	0x00	0x48	0x01	0x119
BACKUP2	RW	8	0x00	0x48	0x02	0x11A
BACKUP3	RW	8	0x00	0x48	0x03	0x11B
BACKUP4	RW	8	0x00	0x48	0x04	0x11C
BACKUP5	RW	8	0x00	0x48	0x05	0x11D
BACKUP6	RW	8	0x00	0x48	0x06	0x11E
BACKUP7	RW	8	0x00	0x48	0x07	0x11F

1.3.2 FUNC_BACKUP Register Descriptions

1.3.2.1 BACKUP0 Register

Table 1-29. BACKUP0

Address offset	0x00			**I2C Address**	0x48
Physical Address	0x118	**Instance**		FUNC_VALIDITY	
Description	Backup register #0 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR MSECURE register protected : Yes				
Type	RW				

7	6	5	4	3	2	1	0
BACKUP							

Bits	Field Name	Description	Type	Reset
7:0	BACKUP		RW	0x00

1.3.2.2 BACKUP1 Register

Table 1-30. BACKUP1

Address offset	0x01			**I2C Address**	0x48
Physical Address	0x119	**Instance**		FUNC_VALIDITY	
Description	Backup register #1 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR MSECURE register protected : Yes				
Type	RW				

7	6	5	4	3	2	1	0
BACKUP							

Bits	Field Name	Description	Type	Reset
7:0	BACKUP		RW	0x00

1.3.2.3 BACKUP2 Register

Table 1-31. BACKUP2

Address offset	0x02			**I2C Address**	0x48
Physical Address	0x11A	**Instance**		FUNC_VALIDITY	
Description	Backup register #2 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR MSECURE register protected : Yes				
Type	RW				

7	6	5	4	3	2	1	0
BACKUP							

Bits	Field Name	Description	Type	Reset
7:0	BACKUP		RW	0x00

1.3.2.4 BACKUP3 Register

Table 1-32. BACKUP3

Address offset	0x03	**I2C Address**	0x48
Physical Address	0x11B **Instance**	FUNC_VALIDITY	
Description	Backup register #3 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR MSECURE register protected : Yes		
Type	RW		

7	6	5	4	3	2	1	0
BACKUP							

Bits	Field Name	Description	Type	Reset
7:0	BACKUP		RW	0x00

1.3.2.5 BACKUP4 Register

Table 1-33. BACKUP4

Address offset	0x04	**I2C Address**	0x48
Physical Address	0x11C **Instance**	FUNC_VALIDITY	
Description	Backup register #4 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR MSECURE register protected : Yes		
Type	RW		

7	6	5	4	3	2	1	0
BACKUP							

Bits	Field Name	Description	Type	Reset
7:0	BACKUP		RW	0x00

1.3.2.6 BACKUP5 Register

Table 1-34. BACKUP5

Address offset	0x05	**I2C Address**	0x48
Physical Address	0x11D **Instance**	FUNC_VALIDITY	
Description	Backup register #5 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR MSECURE register protected : Yes		
Type	RW		

7	6	5	4	3	2	1	0
BACKUP							

Bits	Field Name	Description	Type	Reset
7:0	BACKUP		RW	0x00

1.3.2.7 BACKUP6 Register

Table 1-35. BACKUP6

Address offset	0x06	**I2C Address**	0x48
Physical Address	0x11E **Instance**	FUNC_VALIDITY	
Description	Backup register #6 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR MSECURE register protected : Yes		
Type	RW		

7	6	5	4	3	2	1	0
BACKUP							

Bits	Field Name	Description	Type	Reset
7:0	BACKUP		RW	0x00

1.3.2.8 BACKUP7 Register

Table 1-36. BACKUP7

Address offset	0x07	**I2C Address**	0x48
Physical Address	0x11F **Instance**	FUNC_VALIDITY	
Description	Backup register #7 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR MSECURE register protected : Yes		
Type	RW		

7	6	5	4	3	2	1	0
BACKUP							

Bits	Field Name	Description	Type	Reset
7:0	BACKUP		RW	0x00

1.4 FUNC_SMPS Registers

1.4.1 FUNC_SMPS Registers Mapping Summary

This section provides information on the FUNC_SMPS Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.4.1.1 FUNC_SMPS Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
SMPS12_CTRL	RW	8	0x00	0x48	0x00	0x120
SMPS12_TSTEP	RW	8	0x02	0x48	0x01	0x121
SMPS12_FORCE	RW	8	0b1XXX XXXX	0x48	0x02	0x122
SMPS12_VOLTAGE	RW	8	0xXX	0x48	0x03	0x123
SMPS3_CTRL	RW	8	0x00	0x48	0x04	0x124
SMPS3_VOLTAGE	RW	8	0xXX	0x48	0x07	0x127
SMPS45_CTRL	RW	8	0x00	0x48	0x08	0x128
SMPS45_TSTEP	RW	8	0x02	0x48	0x09	0x129
SMPS45_FORCE	RW	8	0b1XXX XXXX	0x48	0x0A	0x12A
SMPS45_VOLTAGE	RW	8	0xXX	0x48	0x0B	0x12B
SMPS6_CTRL	RW	8	0x00	0x48	0x0C	0x12C
SMPS6_TSTEP	RW	8	0x02	0x48	0x0D	0x12D
SMPS6_FORCE	RW	8	0b1XXX XXXX	0x48	0x0E	0x12E
SMPS6_VOLTAGE	RW	8	0xXX	0x48	0x0F	0x12F
SMPS7_CTRL	RW	8	0x00	0x48	0x10	0x130
SMPS7_VOLTAGE	RW	8	0xXX	0x48	0x13	0x133
SMPS8_CTRL	RW	8	0x00	0x48	0x14	0x134
SMPS8_TSTEP	RW	8	0x02	0x48	0x15	0x135
SMPS8_FORCE	RW	8	0b1XXX XXXX	0x48	0x16	0x136
SMPS8_VOLTAGE	RW	8	0xXX	0x48	0x17	0x137
SMPS9_CTRL	RW	8	0x00	0x48	0x18	0x138
SMPS9_VOLTAGE	RW	8	0xXX	0x48	0x1B	0x13B
SMPS10_CTRL	RW	8	0bX000 X000	0x48	0x1C	0x13C
SMPS10_STATUS	RO	8	0x00	0x48	0x1F	0x13F
SMPS_CTRL	RW	8	0b00XX 0000	0x48	0x24	0x144
SMPS_PD_CTRL	RW	8	0x7F	0x48	0x25	0x145
SMPS_DITHER_EN	RW	8	0x7F	0x48	0x26	0x146
SMPS_THERMAL_EN	RW	8	0xFF	0x48	0x27	0x147
SMPS_THERMAL_STATUS	RO	8	0x00	0x48	0x28	0x148
SMPS_SHORT_STATUS	RO	8	0x00	0x48	0x29	0x149
SMPS_NEGATIVE_CURRENT_LIMIT_EN	RW	8	0xFF	0x48	0x2A	0x14A
SMPS_POWERGOOD_MASK1	RW	8	0xFE	0x48	0x2B	0x14B
SMPS_POWERGOOD_MASK2	RW	8	0x07	0x48	0x2C	0x14C

1.4.2 FUNC_SMPS Register Descriptions

1.4.2.1 SMPS12_CTRL Register

Table 1-37. SMPS12_CTRL

Address offset	0x00	**I2C Address**	0x48
Physical Address	0x120 **Instance**	FUNC_SMPS	
Description	SMPS12 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS12_VOLTAGE.VSEL and SMPS12_FORCE.VSEL register and re-load the default value (reset value) in SMPS12_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).	RW	0
6	ROOF_FLOOR_EN	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS12_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1, ENABLE2).	RW	0
5:4	STATUS	SMPS12 status 00: OFF 01: AUTO 10: ECO 11: Forced PWM	RO	0x0
3:2	MODE_SLEEP	SMPS12 SLEEP Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0
1:0	MODE_ACTIVE	SMPS12 ACTIVE Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0

1.4.2.2 SMPS12_TSTEP Register

Table 1-38. SMPS12_TSTEP

Address offset	0x01			**I2C Address**	0x48
Physical Address	0x121	**Instance**		FUNC_SMPS	
Description	SMPS12 TSTEP register. RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved						TSTEP	

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1:0	TSTEP	Time Step (TSTEP) selection, when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate(1) of the output voltage is: TSTEP[1:0]: 00 Jump (no slope control) slew TSTEP[1:0]: 01 10mV/us TSTEP[1:0]: 10 5mV/us (default) TSTEP[1:0]: 11 2.5mV/us	RW	0x2

(1) Slew rate is averaged over full range. Slew rate can vary as a function of initial voltage and final voltage. See Application note SWCA226 – How to Use SMPS Slew-Rate control in TPS65913/TPS65914 for an accurate calculation the slew rate and settling time.

1.4.2.3 SMPS12_FORCE Register

Table 1-39. SMPS12_FORCE

Address offset	0x02			**I2C Address**	0x48
Physical Address	0x122	**Instance**		FUNC_SMPS	
Description	SMPS12 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
CMD	VSEL						

Bits	Field Name	Description	Type	Reset
7	CMD	DVS command register selection: When 0: SMPS12_FORCE.VSEL voltage is applied When 1: SMPS12_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS12_CTRL.ROOF_FLOOR_EN='0'	RW	1
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register	RW	0bXXX XXXX

1.4.2.4 SMPS12_VOLTAGE Register

Table 1-40. SMPS12_VOLTAGE

Address offset	0x03			**I2C Address**	0x48
Physical Address	0x123	**Instance**		FUNC_SMPS	
Description	SMPS12 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS12_VOLTAGE.VSEL and SMPS12_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.	RW	X

Bits	Field Name	Description	Type	Reset
6:0	VSEL	VSEL[6:0] cross table voltage (OFF,0.5V to 3.3V) RANGE[0]=0 (x1 multiplier)/ 1(x2 multiplier) 0000000 = SMPS OFF/OFF 1000000 = 1.08V/2.16V 0000001 = 0.5V/1V 1000001 = 1.09V/2.18V 0000010 = 0.5V/1V 1000010 = 1.1V/2.2V 0000011 = 0.5V/1V 1000011 = 1.11V/2.22V 0000100 = 0.5V/1V 1000100 = 1.12V/2.24V 0000101 = 0.5V/1V 1000101 = 1.13V/2.26V 0000110 = 0.5V/1V 1000110 = 1.14V/2.28V 0000111 = 0.51V/1.02V 1000111 = 1.15V/2.3V 0001000 = 0.52V/1.04V 1001000 = 1.16V/2.32V 0001001 = 0.53V/1.06V 1001001 = 1.17V/2.34V 0001010 = 0.54V/1.08V 1001010 = 1.18V/2.36V 0001011 = 0.55V/1.1V 1001011 = 1.19V/2.38V 0001100 = 0.56V/1.12V 1001100 = 1.2V/2.4V 0001101 = 0.57V/1.14V 1001101 = 1.21V/2.42V 0001110 = 0.58V/1.16V 1001110 = 1.22V/2.44V 0001111 = 0.59V/1.18V 1001111 = 1.23V/2.46V 0010000 = 0.60V/1.2V 1010000 = 1.24V/2.48V 0010001 = 0.61V/1.22V 1010001 = 1.25V/2.5V 0010010 = 0.62V/1.24V 1010010 = 1.26V/2.52V 0010011 = 0.63V/1.26V 1010011 = 1.27V/2.54V 0010100 = 0.64V/1.28V 1010100 = 1.28V/2.56V 0010101 = 0.65V/1.3V 1010101 = 1.29V/2.58V 0010110 = 0.66V/1.32V 1010110 = 1.3V/2.6V 0010111 = 0.67V/1.34V 1010111 = 1.31V/2.62V 0011000 = 0.68V/1.36V 1011000 = 1.32V/2.64V 0011001 = 0.69V/1.38V 1011001 = 1.33V/2.66V 0011010 = 0.70V/1.4V 1011010 = 1.34V/2.68V 0011011 = 0.71V/1.42V 1011011 = 1.35V/2.7V 0011100 = 0.72V/1.44V 1011100 = 1.36V/2.72V 0011101 = 0.73V/1.46V 1011101 = 1.37V/2.74V 0011110 = 0.74V/1.48V 1011110 = 1.38V/2.76V 0011111 = 0.75V/1.50V 1011111 = 1.39V/2.78V 0100000 = 0.76V/1.52V 1100000 = 1.4V/2.8V 0100001 = 0.77V/1.54V 1100001 = 1.41V/2.82V 0100010 = 0.78V/1.56V 1100010 = 1.42V/2.84V 0100011 = 0.79V/1.58V 1100011 = 1.43V/2.86V 0100100 = 0.8V/1.6V 1100100 = 1.44V/2.88V 0100101 = 0.81V/1.62V 1100101 = 1.45V/2.9V 0100110 = 0.82V/1.64V 1100110 = 1.46V/2.92V 0100111 = 0.83V/1.66V 1100111 = 1.47V/2.94V 0101000 = 0.84V/1.68V 1101000 = 1.48V/2.96V 0101001 = 0.85V/1.7V 1101001= 1.49V/2.98V 0101010 = 0.86V/1.72V 1101010 = 1.5V/3V 0101011 = 0.87V/1.74V 1101011 = 1.51V/3.02V 0101100 = 0.88V/1.76V 1101100 = 1.52V/3.04V 0101101 = 0.89V/1.78V 1101101 = 1.53V/3.06V 0101110 = 0.9V/1.8V 1101110 = 1.54V/3.08V 0101111 = 0.91V/1.82V 1101111 = 1.55V/3.1V 0110000 = 0.92V/1.84V 1110000 = 1.56V/3.12V 0110001 = 0.93V/1.86V 1110001 = 1.57V/3.14V 0110010 = 0.94V/1.88V 1110010 = 1.58V/3.16V 0110011 = 0.95V/1.90V 1110011 = 1.59V/3.18V 0110100 = 0.96V/1.92V 1110100 = 1.6V/3.2V 0110101 = 0.97V/1.94V 1110101 = 1.61V/3.22V 0110110 = 0.98V/1.96V 1110110 = 1.62V/3.24V 0110111 = 0.99V/1.98V 1110111 = 1.63V/3.26V 0111000 = 1.00V/2V 1111000 = 1.64V/3.28V 0111001 = 1.01V/2.02V 1111001 = 1.65V/3.3V 0111010 = 1.02V/2.04V 1111010 = 1.65V/3.3V 0111011 = 1.03V/2.06V 1111011 = 1.65V/3.3V 0111100 = 1.04V/2.08V 1111100 = 1.65V/3.3V 0111101 = 1.05V/2.1V 1111101 = 1.65V/3.3V 0111110 = 1.06V/2.12V 1111110 = 1.65V/3.3V 0111111 = 1.07V/2.14V 1111111 = 1.65V/3.3V	RW	0bXXX XXXX

1.4.2.5 SMPS3_CTRL Register

Table 1-41. SMPS3_CTRL

Address offset	0x04	**I2C Address**	0x48
Physical Address	0x124 **Instance**	FUNC_SMPS	
Description	SMPS3 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	Reserved	STATUS		MODE_SLEEP		MODE_ACTIVE	

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default value (from OTP in SMPS3_VOLTAGE.VSEL register during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).	RW	0
6	Reserved		RO	0
5:4	STATUS	SMPS3 Status 00: OFF 01: AUTO 10: ECO 11: Forced PWM	RO	0x0
3:2	MODE_SLEEP	SMPS3 SLEEP mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0
1:0	MODE_ACTIVE	SMPS3 ACTIVE Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0

1.4.2.6 SMPS3_VOLTAGE Register

Table 1-42. SMPS3_VOLTAGE

Address offset	0x07	**I2C Address**	0x48
Physical Address	0x127 **Instance**	FUNC_SMPS	
Description	SMPS3 register. Voltage to apply to the resource. RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS3_VOLTAGE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.	RW	X

Bits	Field Name	Description	Type	Reset
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.7 SMPS45_CTRL Register

Table 1-43. SMPS45_CTRL

Address offset	0x08		**I2C Address**	0x48	
Physical Address	0x128	**Instance**	FUNC_SMPS		
Description	SMPS45 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).				
Type	RW				

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS45_VOLTAGE.VSEL and SMPS45_FORCE.VSEL register and re-load the default value (reset value) in SMPS45_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).	RW	0
6	ROOF_FLOOR_EN	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS45_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1, ENABLE2).	RW	0
5:4	STATUS	SMPS45 Status 00: OFF 01: AUTO 10: ECO 11: Forced PWM	RO	0x0
3:2	MODE_SLEEP	SMPS45 SLEEP mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0
1:0	MODE_ACTIVE	SMPS45 ACTIVE Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0

1.4.2.8 SMPS45_TSTEP Register

Table 1-44. SMPS45_TSTEP

Address offset	0x09			**I2C Address**	0x48
Physical Address	0x129	**Instance**		FUNC_SMPS	
Description	SMPS45 TSTEP register. RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved						TSTEP	

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1:0	TSTEP	Time Step (TSTEP) selection, when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate(1) of the output voltage is: TSTEP[1:0]: 00 Jump (no slope control) TSTEP[1:0]: 01 10mV/us TSTEP[1:0]: 10 5mV/us (default) TSTEP[1:0]: 11 2.5mV/us	RW	0x2

(1) Slew rate is averaged over full range. Slew rate can vary as a function of initial voltage and final voltage. See Application note SWCA226 – How to Use SMPS Slew-Rate control in TPS65913/TPS65914 for an accurate calculation the slew rate and settling time.

1.4.2.9 SMPS45_FORCE Register

Table 1-45. SMPS45_FORCE

Address offset	0x0A			**I2C Address**	0x48
Physical Address	0x12A	**Instance**		FUNC_SMPS	
Description	SMPS45 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
CMD	VSEL						

Bits	Field Name	Description	Type	Reset
7	CMD	DVS command register selection: When 0: SMPS45_FORCE.VSEL voltage is applied When 1: SMPS45_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS45_CTRL.ROOF_FLOOR_EN='0'	RW	1
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.10 SMPS45_VOLTAGE Register

Table 1-46. SMPS45_VOLTAGE

Address offset	0x0B	**I2C Address**	0x48
Physical Address	0x12B **Instance**	FUNC_SMPS	
Description	SMPS45 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS45_VOLTAGE.VSEL and SMPS45_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.11 SMPS6_CTRL Register

Table 1-47. SMPS6_CTRL

Address offset	0x0C	**I2C Address**	0x48
Physical Address	0x12C **Instance**	FUNC_SMPS	
Description	SMPS6 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS6_VOLTAGE.VSEL and SMPS6_FORCE.VSEL register and re-load the default value (reset value) in SMPS6_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).	RW	0
6	ROOF_FLOOR_EN	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS6_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1, ENABLE2).	RW	0

Bits	Field Name	Description	Type	Reset
5:4	STATUS	SMPS6 Status 00: OFF 01: AUTO 10: ECO 11: Forced PWM	RO	0x0
3:2	MODE_SLEEP	SMPS6 SLEEP mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0
1:0	MODE_ACTIVE	SMPS6 ACTIVE Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0

1.4.2.12 SMPS6_TSTEP Register

Table 1-48. SMPS6_TSTEP

Address offset	0x0D	**I2C Address**	0x48
Physical Address	0x12D **Instance**	FUNC_SMPS	
Description	SMPS6 TSTEP register. RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						TSTEP	

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1:0	TSTEP	Time Step (TSTEP) selection, when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate(1) of the output voltage is: TSTEP[1:0]: 00 Jump (no slope control) TSTEP[1:0]: 01 10mV/us TSTEP[1:0]: 10 5mV/us (default) TSTEP[1:0]: 11 2.5mV/us	RW	0x2

(1) Slew rate is averaged over full range. Slew rate can vary as a function of initial voltage and final voltage. See Application note SWCA226 – How to Use SMPS Slew-Rate control in TPS65913/TPS65914 for an accurate calculation the slew rate and settling time.

1.4.2.13 SMPS6_FORCE Register

Table 1-49. SMPS6_FORCE

Address offset	0x0E	**I2C Address**	0x48
Physical Address	0x12E **Instance**	FUNC_SMPS	
Description	SMPS6 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
CMD	VSEL						

Bits	Field Name	Description	Type	Reset
7	CMD	DVS command register selection: When 0: SMPS6_FORCE.VSEL voltage is applied When 1: SMPS6_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS6_CTRL.ROOF_FLOOR_EN='0'	RW	1
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.14 SMPS6_VOLTAGE Register

Table 1-50. SMPS6_VOLTAGE

Address offset	0x0F	**I2C Address**	0x48
Physical Address	0x12F **Instance**	FUNC_SMPS	
Description	SMPS6 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS6_VOLTAGE.VSEL and SMPS6_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.15 SMPS7_CTRL Register

Table 1-51. SMPS7_CTRL

Address offset	0x10	**I2C Address**	0x48
Physical Address	0x130 **Instance**	FUNC_SMPS	
Description	SMPS7 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	Reserved	STATUS		MODE_SLEEP		MODE_ACTIVE	

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS7_VOLTAGE.VSEL register during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).	RW	0
6	Reserved		RO	0

Bits	Field Name	Description	Type	Reset
5:4	STATUS	SMPS7 Status 00: OFF 01: AUTO 10: ECO 11: Forced PWM	RO	0x0
3:2	MODE_SLEEP	SMPS7 SLEEP mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0
1:0	MODE_ACTIVE	SMPS7 ACTIVE Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0

1.4.2.16 SMPS7_VOLTAGE Register

Table 1-52. SMPS7_VOLTAGE

Address offset	0x13	**I2C Address**	0x48
Physical Address	0x133 **Instance**	FUNC_SMPS	
Description	SMPS7 register. Voltage to apply to the resource. RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS7_VOLTAGE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.17 SMPS8_CTRL Register

Table 1-53. SMPS8_CTRL

Address offset	0x14	**I2C Address**	0x48
Physical Address	0x134 **Instance**	FUNC_SMPS	
Description	SMPS8 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS8_VOLTAGE.VSEL and SMPS8_FORCE.VSEL register and re-load the default value (reset value) in SMPS8_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).	RW	0
6	ROOF_FLOOR_EN	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS8_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1, ENABLE2).	RW	0
5:4	STATUS	SMPS8 Status 00: OFF 01: AUTO 10: ECO 11: Forced PWM	RO	0x0
3:2	MODE_SLEEP	SMPS8 SLEEP mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0
1:0	MODE_ACTIVE	SMPS8 ACTIVE Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0

1.4.2.18 SMPS8_TSTEP Register

Table 1-54. SMPS8_TSTEP

Address offset	0x15			**I2C Address**	0x48
Physical Address	0x135	**Instance**		FUNC_SMPS	
Description	SMPS8 TSTEP register. RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved						TSTEP	

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1:0	TSTEP	Time Step (TSTEP) selection, when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate(1) of the output voltage is: TSTEP[1:0]: 00 Jump (no slope control) TSTEP[1:0]: 01 10mV/us TSTEP[1:0]: 10 5mV/us (default) TSTEP[1:0]: 11 2.5mV/us	RW	0x2

(1) Slew rate is averaged over full range. Slew rate can vary as a function of initial voltage and final voltage. See Application note SWCA226 – How to Use SMPS Slew-Rate control in TPS65913/TPS65914 for an accurate calculation the slew rate and settling time.

1.4.2.19 SMPS8_FORCE Register

Table 1-55. SMPS8_FORCE

Address offset	0x16			**I2C Address**	0x48
Physical Address	0x136	**Instance**		FUNC_SMPS	
Description	SMPS8 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
CMD	VSEL						

Bits	Field Name	Description	Type	Reset
7	CMD	DVS command register selection: When 0: SMPS8_FORCE.VSEL voltage is applied When 1: SMPS8_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS8_CTRL.ROOF_FLOOR_EN='0'	RW	1
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.20 SMPS8_VOLTAGE Register

Table 1-56. SMPS8_VOLTAGE

Address offset	0x17	**I2C Address**	0x48
Physical Address	0x137 **Instance**	FUNC_SMPS	
Description	SMPS8 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS8_VOLTAGE.VSEL and SMPS8_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.21 SMPS9_CTRL Register

Table 1-57. SMPS9_CTRL

Address offset	0x18	**I2C Address**	0x48
Physical Address	0x138 **Instance**	FUNC_SMPS	
Description	SMPS9 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	Reserved	STATUS		MODE_SLEEP		MODE_ACTIVE	

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS9_VOLTAGE.VSEL register during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).	RW	0
6	Reserved		RO	0
5:4	STATUS	SMPS9 Status 00: OFF 01: AUTO 10: ECO 11: Forced PWM	RO	0x0
3:2	MODE_SLEEP	SMPS9 SLEEP Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0
1:0	MODE_ACTIVE	SMPS9 ACTIVE Mode 00: OFF (default) 01: AUTO 10: ECO 11: Forced PWM	RW	0x0

1.4.2.22 SMPS9_VOLTAGE Register

Table 1-58. SMPS9_VOLTAGE

Address offset	0x1B			**I2C Address**	0x48
Physical Address	0x13B	**Instance**		FUNC_SMPS	
Description	SMPS9 register. Voltage to apply to the resource. RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
RANGE	VSEL						

Bits	Field Name	Description	Type	Reset
7	RANGE	Range of the VSEL voltage. This bit is applied to SMPS9_VOLTAGE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE cannot be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.	RW	X
6:0	VSEL	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.	RW	0bXXX XXXX

1.4.2.23 SMPS10_CTRL Register

Table 1-59. SMPS10_CTRL

Address offset	0x1C			**I2C Address**	0x48
Physical Address	0x13C	**Instance**		FUNC_SMPS	
Description	SMPS10 (BOOST) control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).				
Type	RW				

7	6	5	4	3	2	1	0
MODE_SLEEP				MODE_ACTIVE			

Bits	Field Name	Description	Type	Reset
7:4	MODE_SLEEP	SMPS10 SLEEP mode MODE_SLEEP[3] = VSEL, SMPS10_OUT1 and SMPS10_OUT2 output voltage selection (same on both) - OTP bit 0: 3.75V 1: 5V (default) MODE_SLEEP[2] = BOOST_EN, Boost enable (or bypass mode enabled !) 0: Boost not enabled 1: Boost is enabled (or bypass mode enabled) MODE_SLEEP[1] = BYPASS_EN, Bypass SMPS10_IN to SMPS10_OUT2 0: Bypass not enabled 1: Bypass is enabled MODE_SLEEP[0] = SWITCH_EN, Switch SMPS10_OU1 to SMPS10_OUT2 0: Switch not enabled 1: Switch is enabled MODE_SLEEP[3:0]= X 0 X 0 OFF state - SMPS10_OUT1 is floating and SMPS10_OUT2 is connected to VSYS through a diode MODE_SLEEP[3:0]= X 1 1 0 BYPASS state (IN shorted to OUT2) - SMPS10_OUT2 is supplied by SMPS10_IN (VSYS). SMPS10_OUT1 is floating (not driven) MODE_SLEEP[3:0]= 0 1 0 0 BOOST state (OUT2 supplied by boosting VSYS, OUT1 not connected)- SMPS10_OUT2=3.75V as MODE_ACTIVE[3] = VSEL = â€˜0â€™. SMPS10_OUT1 is floating (not driven) MODE_SLEEP[3:0]= 1 1 0 0 BOOST state (OUT2 supplied by boosting VSYS, OUT1 not connected)- SMPS10_OUT2=5.0V as MODE_ACTIVE[3] = VSEL = â€˜1â€™. SMPS10_OUT1 is floating (not driven) MODE_SLEEP[3:0]= 0 1 0 1 BOOST state (OUT2 supplied by boosting VSYS, OUT1 connected to OUT2)- SMPS10_OUT2=3.75V as MODE_ACTIVE[3] = VSEL = â€˜0â€™. MODE_SLEEP[3:0]= 1 1 0 1 BOOST state (OUT2 supplied by boosting VSYS, OUT1 connected to OUT2)- SMPS10_OUT2=5.0V as MODE_ACTIVE[3] = VSEL = â€˜1â€™. PS: The performance 3.75V is not guaranteed on SMPS10_OUT1 output MODE_SLEEP[3:0]= X 0 X 1 SHORTED state (OUT1 shorted to OUT2) - SMPS10_OUT2 is shorted to SMPS10_OUT1, BOOST is not enabled. The IP connected to SMPS10_OUT2 is supplied at the voltage available at SMPS10_OU1	RW	0bX000

Bits	Field Name	Description	Type	Reset
3:0	MODE_ACTIVE	SMPS10 ACTIVE mode MODE_ACTIVE[3] = VSEL, SMPS10_OUT1 and SMPS10_OUT2 output voltage selection (same on both) - OTP bit 0: 3.75V 1: 5V (default) MODE_ACTIVE[2] = BOOST_EN, Boost enable (or bypass mode enabled !) 0: Boost not enabled 1: Boost is enabled (or bypass mode enabled) MODE_ACTIVE[1] = BYPASS_EN, Bypass SMPS10_IN to SMPS10_OUT2 0: Bypass not enabled 1: Bypass is enabled MODE_ACTIVE[0] = SWITCH_EN, Switch SMPS10_OU1 to SMPS10_OUT2 0: Switch not enabled 1: Switch is enabled MODE_ACTIVE[3:0]= X 0 X 0 OFF state - SMPS10_OUT1 is floating and SMPS10_OUT2 is connected to VSYS through a diode MODE_ACTIVE[3:0]= X 1 1 0 BYPASS state (IN shorted to OUT2) - SMPS10_OUT2 is supplied by SMPS10_IN (VSYS). SMPS10_OUT1 is floating (not driven) MODE_ACTIVE[3:0]= 0 1 0 0 BOOST state (OUT2 supplied by boosting VSYS, OUT1 not connected)- SMPS10_OUT2=3.75V as MODE_ACTIVE[3] = VSEL = â€˜0â€™. SMPS10_OUT1 is floating (not driven) MODE_ACTIVE[3:0]= 1 1 0 0 BOOST state (OUT2 supplied by boosting VSYS, OUT1 not connected)- SMPS10_OUT2=5.0V as MODE_ACTIVE[3] = VSEL = â€˜1â€™. SMPS10_OUT1 is floating (not driven) MODE_ACTIVE[3:0]= 0 1 0 1 BOOST state (OUT2 supplied by boosting VSYS, OUT1 connected to OUT2)- SMPS10_OUT2=3.75V as MODE_ACTIVE[3] = VSEL = â€˜0â€™. MODE_ACTIVE[3:0]= 1 1 0 1 BOOST state (OUT2 supplied by boosting VSYS, OUT1 connected to OUT2)- SMPS10_OUT2=5.0V as MODE_ACTIVE[3] = VSEL = â€˜1â€™. PS: The performance 3.75V is not guaranteed on SMPS10_OUT1 output MODE_ACTIVE[3:0]= X 0 X 1 SHORTED state (OUT1 shorted to OUT2) - SMPS10_OUT2 is shorted to SMPS10_OUT1, BOOST is not enabled. The IP connected to SMPS10_OUT2 is supplied at the voltage available at SMPS10_OU1	RW	0bX000

1.4.2.24 SMPS10_STATUS Register

Table 1-60. SMPS10_STATUS

Address offset	0x1F		**I2C Address**	0x48	
Physical Address	0x13F	**Instance**	FUNC_SMPS		
Description	SMPS10 (BOOST) status register. Voltage to apply to the resource when it is not a DVS force command. RESET register domain: SWORST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved				STATUS			

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:0	STATUS	STATUS[3] = VSEL, SMPS10_OUT1 and SMPS10_OUT2 output voltage selection (same on both) 0: 3.75V 1: 5V STATUS [2] = BOOST_EN, Boost enable (or bypass mode enabled !) 0: Boost not enabled 1: Boost is enabled (or bypass mode enabled) STATUS [1] = BYPASS_EN, Bypass SMPS10_IN to SMPS10_OUT2 0: Bypass not enabled 1: Bypass is enabled STATUS [0] = SWITCH_EN, Switch SMPS10_OU1 to SMPS10_OUT2 0: Switch not enabled 1: Switch is enabled	RO	0x0

1.4.2.25 SMPS_CTRL Register

Table 1-61. SMPS_CTRL

Address offset	0x24			**I2C Address**	0x48
Physical Address	0x144	**Instance**		FUNC_SMPS	
Description	SMPS control register. RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		SMPS45_SMPS457_EN	SMPS12_SMPS123_EN	SMPS45_PHASE_CTRL		SMPS123_PHASE_CTRL	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5	SMPS45_SMPS457_EN	Selection of the type of configuration of the SMPS457 0: SMPS45 dual phase, SMPS7 single phase 1: SMPS457 triple phase (Reserved)	RO	X
4	SMPS12_SMPS123_EN	Selection of the type of configuration of the SMPS123 0: SMPS12 dual phase, SMPS3 single phase 1: SMPS123 triple phase	RO	X
3:2	SMPS45_PHASE_CTRL	Selection of the phase mode of the SMPS45 00: Automatic Phase Selection - Multi Phase or Single Phase (default) 11: Automatic Phase Selection - Multi Phase or Single Phase 01: Force Single Phase mode 10: Force Multi Phase phase mode	RW	0x0
1:0	SMPS123_PHASE_CTRL	Selection of the phase mode of the SMPS123 (SMPS12 Dual Phase + SMPS3 Single Phase configuration or SMPS123 Triple Phase configuration) 00: Automatic Phase Selection per SMPS - Multi Phase or Single Phase (default) 11: Automatic Phase Selection per SMPS - Multi Phase or Single Phase 01: Force Single Phase mode (for SMPS12 and SMPS3) 10: Force Multi Phase mode (for SMPS12 and SMPS3)	RW	0x0

1.4.2.26 SMPS_PD_CTRL Register

Table 1-62. SMPS_PD_CTRL

Address offset	0x25			**I2C Address**	0x48
Physical Address	0x145	**Instance**		FUNC_SMPS	
Description	SMPS Pull-Down enable register. RESET register domain: HWRST Notes: SMPS pull-down register bits validate the control of the active discharge of each power resource to full-fill the turn-off timing requirements. When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restart correctly at the next power-up sequence.				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	SMPS9	0: Pull-down is disabled 1: Pull-down is enabled when SPMS9 is in OFF state (default)	RW	1
5	SMPS8	0: Pull-down is disabled 1: Pull-down is enabled when SPMS8 is in OFF state (default)	RW	1
4	SMPS7	0: Pull-down is disabled 1: Pull-down is enabled when SPMS7 is in OFF state (default)	RW	1
3	SMPS6	0: Pull-down is disabled 1: Pull-down is enabled when SPMS6 is in OFF state (default)	RW	1
2	SMPS45	0: Pull-down is disabled 1: Pull-down is enabled when SPMS45 is in OFF state (default)	RW	1
1	SMPS3	0: Pull-down is disabled 1: Pull-down is enabled when SPMS3 is in OFF state (default)	RW	1
0	SMPS12	0: Pull-down is disabled 1: Pull-down is enabled when SPMS12 is in OFF state (default)	RW	1

1.4.2.27 SMPS_DITHER_EN Register

Table 1-63. SMPS_DITHER_EN

Address offset	0x26			**I2C Address**	0x48
Physical Address	0x146	**Instance**		FUNC_SMPS	
Description	SMPS Dither feature enable register. Feature not supported as each SMPS has his own asynchronous oscillator. RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RW	0x7F

1.4.2.28 SMPS_THERMAL_EN Register

Table 1-64. SMPS_THERMAL_EN

Address offset	0x27	**I2C Address**	0x48
Physical Address	0x147 **Instance**	FUNC_SMPS	
Description	SMPS Thermal feature enable register. RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	SMPS6	SMPS457	Reserved	SMPS123

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	1
6	Reserved		RO	1
5	Reserved		RO	1
4	Reserved		RO	1
3	SMPS6	0: SMPS6 Thermal feature is not enabled 1: SMPS6 Thermal feature is enabled (default)	RW	1
2	SMPS457	0: SMPS457 Thermal feature is not enabled 1: SMPS457 Thermal feature is enabled (default)	RW	1
1	Reserved		RO	1
0	SMPS123	0: SMPS123 Thermal feature is not enabled 1: SMPS123 Thermal feature is enabled (default) Note: A unique Thermal Sensor is protecting SMPS12 and SMPS3	RW	1

1.4.2.29 SMPS_THERMAL_STATUS Register

Table 1-65. SMPS_THERMAL_STATUS

Address offset	0x28	**I2C Address**	0x48
Physical Address	0x148 **Instance**	FUNC_SMPS	
Description	SMPS Thermal status register. RESET register domain: POR		
Type	RO		

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	SMPS6	SMPS457	Reserved	SMPS123

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	SMPS6	0: SMPS6 Thermal measurement is below the limit (SMPS is functional) 1: SMPS6 Thermal measurement is over the limit (see specification)	RO	0
2	SMPS457	0: SMPS457 Thermal measurement is below the limit (SMPS is functional) 1: SMPS457 Thermal measurement is over the limit (see specification)	RO	0
1	Reserved		RO	0
0	SMPS123	0: SMPS123 Thermal measurement is below the limit (SMPS is functional) 1: SMPS123 Thermal measurement is over the limit (see specification)	RO	0

1.4.2.30 SMPS_SHORT_STATUS Register

Table 1-66. SMPS_SHORT_STATUS

Address offset	0x29			**I2C Address**	0x48
Physical Address	0x149	**Instance**		FUNC_SMPS	
Description	SMPS Short circuit status. RESET register domain: POR				
Type	RO				

7	6	5	4	3	2	1	0
SMPS10	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12

Bits	Field Name	Description	Type	Reset
7	SMPS10	0: SMPS10 is functional . No short detected (default) 1: SMPS10 output is shorted	RO	0
6	SMPS9	0: SMPS9 is functional . No short detected (default) 1: SMPS9 output is shorted	RO	0
5	SMPS8	0: SMPS8 is functional . No short detected (default) 1: SMPS8 output is shorted	RO	0
4	SMPS7	0: SMPS7 is functional . No short detected (default) 1: SMPS7 output is shorted Note: This bit is un-relevant when SMPS123 is in Triple phase mode	RO	0
3	SMPS6	0: SMPS6 is functional . No short detected (default) 1: SMPS6 output is shorted	RO	0
2	SMPS45	0: SMPS45 (or SMPS457 in Triple phase mode) is functional . No short detected (default) 1: SMPS45 (or SMPS457 in Triple phase mode) output is shorted	RO	0
1	SMPS3	0: SMPS3 is functional . No short detected (default) 1: SMPS3 output is shorted Note: This bit is un-relevant when SMPS123 is in Triple phase mode	RO	0
0	SMPS12	0: SMPS12 (or SMPS123 in Triple phase mode) is functional . No short detected (default) 1: SMPS12 (or SMPS123 in Triple phase mode) output is shorted	RO	0

1.4.2.31 SMPS_NEGATIVE_CURRENT_LIMIT_EN Register

Table 1-67. SMPS_NEGATIVE_CURRENT_LIMIT_EN

Address offset	0x2A			**I2C Address**	0x48
Physical Address	0x14A	**Instance**		FUNC_SMPS	
Description	Iload Negative Current Comparator enable register (Negative Current measurement). RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	1
6	SMPS9	0: SMPS9 Negative Current comparator for measurement is not enabled 1: SMPS9 Negative Current comparator for measurement is enabled (default)	RW	1

Bits	Field Name	Description	Type	Reset
5	SMPS8	0: SMPS8 Negative Current comparator for measurement is not enabled 1: SMPS8 Negative Current comparator for measurement is enabled (default)	RW	1
4	SMPS7	0: SMPS7 Negative Current comparator for measurement is not enabled 1: SMPS7 Negative Current comparator for measurement is enabled (default)	RW	1
3	SMPS6	0: SMPS6 Negative Current comparator for measurement is not enabled 1: SMPS6 Negative Current comparator for measurement is enabled (default)	RW	1
2	SMPS45	0: SMPS45 Negative Current comparator for measurement is not enabled 1: SMPS45 Negative Current comparator for measurement is enabled (default)	RW	1
1	SMPS3	0: SMPS3 Negative Current comparator for measurement is not enabled 1: SMPS3 Negative Current comparator for measurement is enabled (default)	RW	1
0	SMPS12	0: SMPS12 Negative Current comparator for measurement is not enabled 1: SMPS12 Negative Current comparator for measurement is enabled (default)	RW	1

1.4.2.32 SMPS_POWERGOOD_MASK1 Register

Table 1-68. SMPS_POWERGOOD_MASK1

Address offset	0x2B		**I2C Address**	0x48	
Physical Address	0x14B	**Instance**	FUNC_SMPS		
Description	SMPS Power Good (POWERGOOD) mask #1 RESET register domain: POR				
Type	RW				

7	6	5	4	3	2	1	0
SMPS10	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12

Bits	Field Name	Description	Type	Reset
7	SMPS10	SMPS10 POWERGOOD Mask bit register 0: SMPS10 line is enabled. The SMPS10 state is generated on POWERGOOD line 1: SMPS10 line is masked. No SMPS10 state is generated on POWERGOOD line (default)	RW	1
6	SMPS9	SMPS9 POWERGOOD Mask bit register 0: SMPS9 line is enabled. The SMPS9 state is generated on POWERGOOD line 1: SMPS9 line is masked. No SMPS9 state is generated on POWERGOOD line (default)	RW	1
5	SMPS8	SMPS8 POWERGOOD Mask bit register 0: SMPS8 line is enabled. The SMPS8 state is generated on POWERGOOD line 1: SMPS8 line is masked. No SMPS8 state is generated on POWERGOOD line (default)	RW	1
4	SMPS7	SMPS7 POWERGOOD Mask bit register 0: SMPS7 line is enabled. The SMPS7 state is generated on POWERGOOD line 1: SMPS7 line is masked. No SMPS7 state is generated on POWERGOOD line (default)	RW	1

Bits	Field Name	Description	Type	Reset
3	SMPS6	SMPS6 POWERGOOD Mask bit register 0: SMPS6 line is enabled. The SMPS6 state is generated on POWERGOOD line 1: SMPS6 line is masked. No SMPS6 state is generated on POWERGOOD line (default)	RW	1
2	SMPS45	SMPS45 POWERGOOD Mask bit register 0: SMPS45 line is enabled. The SMPS45 state is generated on POWERGOOD line 1: SMPS45 line is masked. No SMPS45 state is generated on POWERGOOD line (default)	RW	1
1	SMPS3	SMPS3 POWERGOOD Mask bit register 0: SMPS3 line is enabled. The SMPS3 state is generated on POWERGOOD line 1: SMPS3 line is masked. No SMPS3 state is generated on POWERGOOD line (default)	RW	1
0	SMPS12	SMPS12 POWERGOOD Mask bit register 0: SMPS12 line is enabled. The SMPS12 state is generated on POWERGOOD line (default) 1: SMPS12 line is masked. No SMPS12 state is generated on POWERGOOD line	RW	0

1.4.2.33 SMPS_POWERGOOD_MASK2 Register

Table 1-69. SMPS_POWERGOOD_MASK2

Address offset	0x2C	**I2C Address**	0x48
Physical Address	0x14C **Instance**	FUNC_SMPS	
Description	SMPS Power Good (POWERGOOD) mask #2 RESET register domain: POR (excepted POWERGOOD_TYPE_SELECT which is under HWRST)		
Type	RW		

7	6	5	4	3	2	1	0
POWERGOOD_TYPE_SELECT	Reserved				GPIO_7	VBUS	ACOK

Bits	Field Name	Description	Type	Reset
7	POWERGOOD_TYPE_SELECT	Selection of the POWERGOOD type of monitoring 0: Voltage monitoring (above threshold)) AND Current monitoring (over current) (default) 1: Current monitoring only (over current)	RW	0
6:3	Reserved		RO	0x0
2	GPIO_7	GPIO_7 POWERGOOD Mask bit register 0: GPIO_7 line is enabled. The GPIO_7 state is generated on POWERGOOD line 1: GPIO_7 line is masked. No GPIO_7 state is generated on POWERGOOD line (default)	RW	1
1	VBUS	VBUS POWERGOOD Mask bit register 0: VBUS line is enabled. The VBUS state is generated on POWERGOOD line 1: VBUS line is masked. No VBUS state is generated on POWERGOOD line (default)	RW	1

Bits	Field Name	Description	Type	Reset
0	ACOK	ACOK POWERGOOD Mask bit register 0: ACOK line is enabled. The ACOK state is generated on POWERGOOD line 1: ACOK line is masked. No ACOK state is generated on POWERGOOD line (default)	RW	1

1.5 FUNC_LDO Registers

1.5.1 FUNC_LDO Registers Mapping Summary

This section provides information on the FUNC_LDO Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.5.1.1 FUNC_LDO Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
LDO1_CTRL	RW	8	0x00	0x48	0x00	0x150
LDO1_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x01	0x151
LDO2_CTRL	RW	8	0x00	0x48	0x02	0x152
LDO2_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x03	0x153
LDO3_CTRL	RW	8	0x00	0x48	0x04	0x154
LDO3_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x05	0x155
LDO4_CTRL	RW	8	0x00	0x48	0x06	0x156
LDO4_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x07	0x157
LDO5_CTRL	RW	8	0x00	0x48	0x08	0x158
LDO5_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x09	0x159
LDO6_CTRL	RW	8	0x00	0x48	0x0A	0x15A
LDO6_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x0B	0x15B
LDO7_CTRL	RW	8	0x00	0x48	0x0C	0x15C
LDO7_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x0D	0x15D
LDO8_CTRL	RW	8	0x00	0x48	0x0E	0x15E
LDO8_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x0F	0x15F
LDO9_CTRL	RW	8	0x00	0x48	0x10	0x160
LDO9_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x11	0x161
LDOLN_CTRL	RW	8	0x00	0x48	0x12	0x162
LDOLN_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x13	0x163
LDOUSB_CTRL	RW	8	0x00	0x48	0x14	0x164
LDOUSB_VOLTAGE	RW	8	0b00XX XXXX	0x48	0x15	0x165
LDO_CTRL	RW	8	0b0000 000X	0x48	0x1A	0x16A
LDO_PD_CTRL1	RW	8	0xFF	0x48	0x1B	0x16B
LDO_PD_CTRL2	RW	8	0x0F	0x48	0x1C	0x16C
LDO_SHORT_STATUS1	RO	8	0x00	0x48	0x1D	0x16D
LDO_SHORT_STATUS2	RO	8	0x00	0x48	0x1E	0x16E

1.5.2 FUNC_LDO Register Descriptions

1.5.2.1 LDO1_CTRL Register

Table 1-70. LDO1_CTRL

Address offset	0x00			**I2C Address**	0x48
Physical Address	0x150	**Instance**		FUNC_LDO	
Description	LDO1 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).				
Type	RW				

7	6	5	4	3	2	1	0
WR_S	Reserved		STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO1_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6:5	Reserved		RO	0x0
4	STATUS	LDO1 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO1 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO1 ACTIVE Mode 0: OFF 1: ON This bit can be updated by power-up sequencer	RW	0

1.5.2.2 LDO1_VOLTAGE Register

Table 1-71. LDO1_VOLTAGE

Address offset	0x01			**I2C Address**	0x48
Physical Address	0x151	**Instance**		FUNC_LDO	
Description	LDO1 Voltage selection (OTP_Config) RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	VSEL[5:0] cross table voltage (OFF,0.9V to 3.3V) 000000 0V 100000 2,45V 000001 0,9V 100001 2,5V 000010 0,95V 100010 2,55V 000011 1V 100011 2,6V 000100 1,05V 100100 2,65V 000101 1,1V 100101 2,7V 000110 1,15V 100110 2,75V 000111 1,2V 100111 2,8V 001000 1,25V 101000 2,85V 001001 1,3V 101001 2,9V 001010 1,35V 101010 2,95V 001011 1,4V 101011 3V 001100 1,45V 101100 3,05V 001101 1,5V 101101 3,1V 001110 1,55V 101110 3,15V 001111 1,6V 101111 3,2V 010000 1,65V 110000 3,25V 010001 1,7V 110001 3,3V 010010 1,75V 110010 3,3V 010011 1,8V 110011 3,3V 010100 1,85V 110100 3,3V 010101 1,9V 110101 3,3V 010110 1,95V 110110 3,3V 010111 2V 110111 3,3V 011000 2,05V 111000 3,3V 011001 2,1V 111001 3,3V 011010 2,15V 111010 3,3V 011011 2,2V 111011 3,3V 011100 2,25V 111100 3,3V 011101 2,3V 111101 3,3V 011110 2,35V 111110 3,3V 011111 2,4V 111111 3,3V	RW	0bXX XXXX

1.5.2.3 LDO2_CTRL Register

Table 1-72. LDO2_CTRL

Address offset	0x02		**I2C Address**	0x48	
Physical Address	0x152	**Instance**	FUNC_LDO		
Description	LDO2 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).				
Type	RW				

7	6	5	4	3	2	1	0
WR_S	Reserved		STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO2_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6:5	Reserved		RO	0x0

Bits	Field Name	Description	Type	Reset
4	STATUS	LDO2 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO2 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO2 ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.4 LDO2_VOLTAGE Register

Table 1-73. LDO2_VOLTAGE

Address offset	0x03	**I2C Address**	0x48
Physical Address	0x153 **Instance**	FUNC_LDO	
Description	LDO2 Voltage selection (OTP_Config) RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.5 LDO3_CTRL Register

Table 1-74. LDO3_CTRL

Address offset	0x04	**I2C Address**	0x48
Physical Address	0x154 **Instance**	FUNC_LDO	
Description	LDO3 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) MODE_SLEEP is used when NSLEEP/ENABLE1/ENABL2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP/ENABLE1/ENABL2 signals select the resource.		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	Reserved		STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO3_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6:5	Reserved		RO	0x0

Bits	Field Name	Description	Type	Reset
4	STATUS	LDO3 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO3 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO3 ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.6 LDO3_VOLTAGE Register

Table 1-75. LDO3_VOLTAGE

Address offset	0x05	**I2C Address**	0x48
Physical Address	0x155 **Instance**	FUNC_LDO	
Description	LDO3 Voltage selection (OTP_Config) RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.7 LDO4_CTRL Register

Table 1-76. LDO4_CTRL

Address offset	0x06	**I2C Address**	0x48
Physical Address	0x156 **Instance**	FUNC_LDO	
Description	LDO4 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) MODE_SLEEP is used when NSLEEP/ENABLE1/ENABL2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP/ENABLE1/ENABL2 signals select the resource.		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	Reserved		STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO4_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6:5	Reserved		RO	0x0

Bits	Field Name	Description	Type	Reset
4	STATUS	LDO4 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO4 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO4 ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.8 LDO4_VOLTAGE Register

Table 1-77. LDO4_VOLTAGE

Address offset	0x07	**I2C Address**	0x48
Physical Address	0x157 **Instance**	FUNC_LDO	
Description	LDO4 Voltage selection (OTP_Config) RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.9 LDO5_CTRL Register

Table 1-78. LDO5_CTRL

Address offset	0x08	**I2C Address**	0x48
Physical Address	0x158 **Instance**	FUNC_LDO	
Description	LDO5 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	Reserved		STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO5_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0

Bits	Field Name	Description	Type	Reset
6:5	Reserved		RO	0x0
4	STATUS	LDO5 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO5 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO5 ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.10 LDO5_VOLTAGE Register

Table 1-79. LDO5_VOLTAGE

Address offset	0x09	**I2C Address**	0x48
Physical Address	0x159 **Instance**	FUNC_LDO	
Description	LDO5 Voltage selection (OTP_Config) RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.11 LDO6_CTRL Register

Table 1-80. LDO6_CTRL

Address offset	0x0A	**I2C Address**	0x48
Physical Address	0x15A **Instance**	FUNC_LDO	
Description	LDO6 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	LDO_VIB_EN	Reserved	STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO6_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6	LDO_VIB_EN	LDO vibrator enable 0: LDO6 is configured as a standard power resource (default) 1: LDO6 is configured as a vibrator	RW	0
5	Reserved		RO	0
4	STATUS	LDO6 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO6 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO6 ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.12 LDO6_VOLTAGE Register

Table 1-81. LDO6_VOLTAGE

Address offset	0x0B			**I2C Address**	0x48
Physical Address	0x15B	**Instance**		FUNC_LDO	
Description	LDO6 Voltage selection (OTP_Config) RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.13 LDO7_CTRL Register

Table 1-82. LDO7_CTRL

Address offset	0x0C			**I2C Address**	0x48
Physical Address	0x15C	**Instance**		FUNC_LDO	
Description	LDO7 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).				
Type	RW				

7	6	5	4	3	2	1	0
WR_S	Reserved		STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO7_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6:5	Reserved		RO	0x0
4	STATUS	LDO7 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO7 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO7 ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.14 LDO7_VOLTAGE Register

Table 1-83. LDO7_VOLTAGE

Address offset	0x0D			**I2C Address**	0x48
Physical Address	0x15D	**Instance**		FUNC_LDO	
Description	LDO7 Voltage selection (OTP_Config) RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.15 LDO8_CTRL Register

Table 1-84. LDO8_CTRL

Address offset	0x0E	**I2C Address**	0x48
Physical Address	0x15E **Instance**	FUNC_LDO	
Description	LDO8 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	LDO_TRACKING_EN	Reserved	STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO8_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6	LDO_TRACKING_EN	LDO tracking enable 0: no tracking enabled 1: tracking enabled	RW	0
5	Reserved		RO	0
4	STATUS	LDO8 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO8 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO8 ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.16 LDO8_VOLTAGE Register

Table 1-85. LDO8_VOLTAGE

Address offset	0x0F	**I2C Address**	0x48
Physical Address	0x15F **Instance**	FUNC_LDO	
Description	LDO8 Voltage selection (OTP_Config) RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.17 LDO9_CTRL Register

Table 1-86. LDO9_CTRL

Address offset	0x10			**I2C Address**	0x48
Physical Address	0x160	**Instance**		FUNC_LDO	
Description	LDO9 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).				
Type	RW				

7	6	5	4	3	2	1	0
WR_S	LDO_BYPASS_EN	Reserved	STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDO9_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6	LDO_BYPASS_EN	LDO bypass enable 0: no bypass enabled (default) 1: bypass enabled	RW	0
5	Reserved		RO	0
4	STATUS	LDO9 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDO9 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDO9 ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.18 LDO9_VOLTAGE Register

Table 1-87. LDO9_VOLTAGE

Address offset	0x11			**I2C Address**	0x48
Physical Address	0x161	**Instance**		FUNC_LDO	
Description	LDO9 Voltage selection (OTP_Config) RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.19 LDOLN_CTRL Register

Table 1-88. LDOLN_CTRL

Address offset	0x12	**I2C Address**	0x48
Physical Address	0x162 **Instance**	FUNC_LDO	
Description	LDOLN control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).		
Type	RW		

7	6	5	4	3	2	1	0
WR_S	Reserved		STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDOLN_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6:5	Reserved		RO	0x0
4	STATUS	LDOLN Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDOLN SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDOLN ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.20 LDOLN_VOLTAGE Register

Table 1-89. LDOLN_VOLTAGE

Address offset	0x13			**I2C Address**	0x48
Physical Address	0x163	**Instance**		FUNC_LDO	
Description	LDOLN Voltage selection (OTP_Config) RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.21 LDOUSB_CTRL Register

Table 1-90. LDOUSB_CTRL

Address offset	0x14			**I2C Address**	0x48
Physical Address	0x164	**Instance**		FUNC_LDO	
Description	LDOUSB control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).				
Type	RW				

7	6	5	4	3	2	1	0
WR_S	Reserved		STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7	WR_S	Warm reset sensitivity 0: Re-load the default LDOUSB_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)	RW	0
6:5	Reserved		RO	0x0
4	STATUS	LDOUSB Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	LDOUSB SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	LDOUSB ACTIVE Mode 0: OFF 1: ON	RW	0

1.5.2.22 LDOUSB_VOLTAGE Register

Table 1-91. LDOUSB_VOLTAGE

Address offset	0x15			**I2C Address**	0x48
Physical Address	0x165	**Instance**		FUNC_LDO	
Description	LDOUSB Voltage selection (OTP_Config) RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		VSEL					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	VSEL	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.	RW	0bXX XXXX

1.5.2.23 LDO_CTRL Register

Table 1-92. LDO_CTRL

Address offset	0x1A			**I2C Address**	0x48
Physical Address	0x16A	**Instance**		FUNC_LDO	
Description	LDO Control register RESET register domain: SWORST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved							LDOUSB_ON_VBUS_VSYS

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RO	0x00
0	LDOUSB_ON_VBUS_VSYS	LDOUSB inputs controls. Controlled by internal switch. 0: LDOUSB_IN2 connected is connected to the LDO - Case VBUS 1: LDOUSB_IN1 connected is connected to the LDO - Case VSYS	RW	X

1.5.2.24 LDO_PD_CTRL1 Register

Table 1-93. LDO_PD_CTRL1

Address offset	0x1B			**I2C Address**	0x48
Physical Address	0x16B	**Instance**		FUNC_LDO	
Description	LDO Pull-Down enable register #1 RESET register domain: HWRST NOTES: LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements. When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.				
Type	RW				

7	6	5	4	3	2	1	0
LDO8	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1

Bits	Field Name	Description	Type	Reset
7	LDO8	0: Pull-Down is disable 1: Pull-Down is enabled when LDO8 is in OFF state	RW	1
6	LDO7	0: Pull-Down is disable 1: Pull-Down is enabled when LDO7 is in OFF state	RW	1
5	LDO6	0: Pull-Down is disable 1: Pull-Down is enabled when LDO6 is in OFF state	RW	1
4	LDO5	0: Pull-Down is disable 1: Pull-Down is enabled when LDO5 is in OFF state	RW	1
3	LDO4	0: Pull-Down is disable 1: Pull-Down is enabled when LDO4 is in OFF state	RW	1
2	LDO3	0: Pull-Down is disable 1: Pull-Down is enabled when LDO3 is in OFF state	RW	1
1	LDO2	0: Pull-Down is disable 1: Pull-Down is enabled when LDO2 is in OFF state	RW	1
0	LDO1	0: Pull-Down is disable 1: Pull-Down is enabled when LDO1 is in OFF state	RW	1

1.5.2.25 LDO_PD_CTRL2 Register

Table 1-94. LDO_PD_CTRL2

Address offset	0x1C			**I2C Address**	0x48
Physical Address	0x16C	**Instance**		FUNC_LDO	
Description	LDO Pull-Down enable register #2 RESET register domain: HWRST NOTES: LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements. When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.				
Type	RW				

7	6	5	4	3	2	1	0
Reserved				LDOVANA	LDOUSB	LDOLN	LDO9

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3	LDOVANA	LDOVANA (internal LDO - reserved) 0: Pull-Down is disable 1: Pull-Down is enabled when LDOVANA is in OFF state	RW	1

Bits	Field Name	Description	Type	Reset
2	LDOUSB	0: Pull-Down is disable 1: Pull-Down is enabled when LDOUSB is in OFF state	RW	1
1	LDOLN	0: Pull-Down is disable 1: Pull-Down is enabled when LDOLN is in OFF state	RW	1
0	LDO9	0: Pull-Down is disable 1: Pull-Down is enabled when LDO9 is in OFF state	RW	1

1.5.2.26 LDO_SHORT_STATUS1 Register

Table 1-95. LDO_SHORT_STATUS1

Address offset	0x1D		**I2C Address**	0x48	
Physical Address	0x16D	**Instance**	FUNC_LDO		
Description	LDO Short circuit status register #1 At Power-On, LDO short input informations are masked during 1 ms. This 1 ms masking is activated and re-started each time one LDO is enabled. RESET register domain: POR				
Type	RO				

7	6	5	4	3	2	1	0
LDO8	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1

Bits	Field Name	Description	Type	Reset
7	LDO8	0: LDO8 is functional. No short detected (default) 1: LDO8 output is short detected	RO	0
6	LDO7	0: LDO7 is functional. No short detected (default) 1: LDO7 output is short detected	RO	0
5	LDO6	0: LDO6 is functional. No short detected (default) 1: LDO6 output is short detected	RO	0
4	LDO5	0: LDO5 is functional. No short detected (default) 1: LDO5 output is short detected	RO	0
3	LDO4	0: LDO4 is functional. No short detected (default) 1: LDO4 output is short detected	RO	0
2	LDO3	0: LDO3 is functional. No short detected (default) 1: LDO3 output is short detected	RO	0
1	LDO2	0: LDO2 is functional. No short detected (default) 1: LDO2 output is short detected	RO	0
0	LDO1	0: LDO1 is functional. No short detected (default) 1: LDO1 output is short detected	RO	0

1.5.2.27 LDO_SHORT_STATUS2 Register

Table 1-96. LDO_SHORT_STATUS2

Address offset	0x1E		**I2C Address**	0x48	
Physical Address	0x16E	**Instance**	FUNC_LDO		
Description	LDO short circuit status register #2 RESET register domain: POR				
Type	RO				

7	6	5	4	3	2	1	0
Reserved				LDOVANA	LDOUSB	LDOLN	LDO9

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3	LDOVANA	LDOVANA (internal LDO - reserved) 0: LDOVANA is functional. No short detected (default) 1: LDOVANA output is short detected	RO	0
2	LDOUSB	0: LDOUSB is functional. No short detected (default) 1: LDOUSB output is short detected	RO	0
1	LDOLN	0: LDOLN is functional. No short detected (default) 1: LDOLN output is short detected	RO	0
0	LDO9	0: LDO9 is functional. No short detected (default) 1: LDO9 output is short detected	RO	0

1.6 FUNC_SPI Registers

1.6.1 FUNC_SPI Registers Mapping Summary

This section provides information on the FUNC_SPI Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.6.1.1 FUNC_SPI Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
SPI_PAGE_CTRL	RW	8	0x00	0x48	0x00	0x17F

1.6.2 FUNC_SPI Register Descriptions

1.6.2.1 SPI_PAGE_CTRL Register

Table 1-97. SPI_PAGE_CTRL

Address offset	0x00	**I2C Address**	0x48
Physical Address	0x17F **Instance**	FUNC_SPI	
Description	SPI Page Control register (used only when SPI interface is used). RESET register domain: SWORST MSECURE register protected : Yes		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED							SPI_PAGE_ACCESS

Bits	Field Name	Description	Type	Reset
7:1	RESERVED	This bit field is reserved.	RO	0x00
0	SPI_PAGE_ACCESS	Page selection for SPI interface only 0: page1 (ID1=48) and page2 (ID2=49) 1: page2 (ID1=49) and page3 (ID2=4A)	RW	0

1.7 FUNC_DVFS Registers

1.7.1 FUNC_DVFS Registers Mapping Summary

This section provides information on the FUNC_DVFS Module Instance within this product. Each of the registers within the Module Instance is described separately below.

ES1.0: Reserved registers

ES2.0->: DVFS registers

1.7.1.1 FUNC_DVFS Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
SMPS_DVFS1_CTRL	RW	8	0x04	0x48	0x00	0x180
SMPS_DVFS1_VOLTAGE_MAX	RW	8	0x00	0x48	0x01	0x181
SMPS_DVFS1_STATUS	RO	8	0x00	0x48	0x02	0x182
SMPS_DVFS2_CTRL	RW	8	0x04	0x48	0x03	0x183
SMPS_DVFS2_VOLTAGE_MAX	RW	8	0x00	0x48	0x04	0x184
SMPS_DVFS2_STATUS	RO	8	0x00	0x48	0x05	0x185

1.7.2 FUNC_DVFS Register Descriptions

1.7.2.1 SMPS_DVFS1_CTRL Register

Table 1-98. SMPS_DVFS1_CTRL

Address offset	0x00	**I2C Address**	0x48
Physical Address	0x180 **Instance**	FUNC_DVFS	
Description	ES1.0: Reserved register ES2.0->: SMPS DVFS1 control register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				DVFS1_RESTORE_VALUE	DVFS1_ENABLE_RST	DVFS1_OFFSET_STEP	DVFS1_ENABLE

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3	DVFS1_RESTORE_VALUE	Control the SMPS12 output voltage upon OFF to ACTIVE transition controlled with ENABLE1/ENABLE2 pins 0: upon OFF to ACTIVE transition controlled with ENABLE* pins, SMPS12 output voltage is set by SMPS12_VOLTAGE.VSEL register 1: upon OFF to ACTIVE transition controlled with ENABLE* pins, SMPS12 output voltage is set with the latest voltage (sum result of the Offset value computed on PWM_DAT signal plus SMPS12_FORCE.VSEL register) before ACTIVE to OFF. This value is restored only if DVFS1 feature was already enabled (DVFS1_ENABLE=1) before ACTIVE to OFF transition controlled with ENABLE* pins.	RW	0
2	DVFS1_ENABLE_RST	Control the DVFS1 Enable feature upon OFF to ACTIVE transition controlled with ENABLE1/ENABLE2 pins 0: DVFS1 feature is automatically re-enabled upon OFF to ACTIVE transition controlled with ENABLEx pins if the feature was already enabled ((DVFS1_ENABLE=1) before ACTIVE to OFF transition controlled with ENABLEx pins 1: DVFS1 feature is not automatically enable (DVFS1_ENABLE=0) upon OFF to ACTIVE transition controlled with ENABLEx pin. To select the DVFS1 feature, the DVFS1_ENABLE must be written to one by SW.	RW	1
1	DVFS1_OFFSET_STEP	Selection of the offset step for DVFS1 function: 0: offset step of 10mV (default) 1: offset step of 20mV	RW	0
0	DVFS1_ENABLE	Selection of the DVFS1 function: 0: DVFS1 is not enabled (default) 1: DVFS1 is enabled (Control of SMPS12 or SMPS123) DVFS1 function in link to DVFS1_CLK (I2C2_SCL_SCE mode I2C selected) and DVFS1_DAT (I2C2_SDA_SDO mode I2C selected).	RW	0

1.7.2.2 SMPS_DVFS1_VOLTAGE_MAX Register

Table 1-99. SMPS_DVFS1_VOLTAGE_MAX

Address offset	0x01	**I2C Address**	0x48
Physical Address	0x181 **Instance**	FUNC_DVFS	
Description	ES1.0: Reserved register ES2.0->: SMPS DVFS1 maximum voltage register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
LOCK	VOLTAGE_MAX						

Bits	Field Name	Description	Type	Reset
7	LOCK	Access protection of the DVFS1_VOLTAGE_MAX register 0: No protection. R/W access to these register bits 1: Protection of these registers (Read only). This bit will reset (0b0) during HWRST SWITCH-OFF	RW	0
6:0	VOLTAGE_MAX	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register with RANGE[0]=0 (x1 multiplier) and VSEL range from OFF, 0.5 to 1.65V	RW	0x00

1.7.2.3 SMPS_DVFS1_STATUS Register

Table 1-100. SMPS_DVFS1_STATUS

Address offset	0x02			**I2C Address**	0x48
Physical Address	0x182	**Instance**		FUNC_DVFS	
Description	ES1.0: Reserved register ES2.0->: SMPS DVFS1 status register RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved		OFFSET_STATUS					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	OFFSET_STATUS	Offset status register (between 0 and 32 in decimal) SMPS_DVFS_CTRL.DVFS1_OFFSET_STEP=0 (x1 multiplier, 10mv per step)/ 1(x2 multiplier), 20mV per step) 000000: no offset 000001: 10mV/20mV 000010: 20mV/40mV ... 100000: 320mV/640mV 100001: reserved/reserved .. 111111: reserved/reserved	RO	0x00

1.7.2.4 SMPS_DVFS2_CTRL Register

Table 1-101. SMPS_DVFS2_CTRL

Address offset	0x03			**I2C Address**	0x48
Physical Address	0x183	**Instance**		FUNC_DVFS	
Description	ES1.0: Reserved register ES2.0->: SMPS DVFS2 control register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved				DVFS2_RESTORE_VALUE	DVFS2_ENABLE_RST	DVFS2_OFFSET_STEP	DVFS2_ENABLE

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3	DVFS2_RESTORE_VALUE	Control the SMPS6 output voltage upon OFF to ACTIVE transition controlled with ENABLE1/ENABLE2 pins 0: upon OFF to ACTIVE transition controlled with ENABLE* pins, SMPS6 output voltage is set by SMPS6_VOLTAGE.VSEL register 1: upon OFF to ACTIVE transition controlled with ENABLE* pins, SMPS6 output voltage is set with the latest voltage (sum result of the Offset value computed on PWM_DAT signal plus SMPS6_FORCE.VSEL register) before ACTIVE to OFF. This value is restored only if DVFS2 feature was already enabled (DVFS2_ENABLE=1) before ACTIVE to OFF transition controlled with ENABLE* pins.	RW	0
2	DVFS2_ENABLE_RST	Control the DVFS2 Enable feature upon OFF to ACTIVE transition controlled with ENABLE1/ENABLE2 pins 0: DVFS2 feature is automatically re-enabled upon OFF to ACTIVE transition controlled with ENABLEx pins if the feature was already enabled ((DVFS2_ENABLE=1) before ACTIVE to OFF transition controlled with ENABLEx pins 1: DVFS2 feature is not automatically enable (DVFS2_ENABLE=0) upon OFF to ACTIVE transition controlled with ENABLEx pin. To select the DVFS2 feature, the DVFS2_ENABLE must be written to one by SW.	RW	1
1	DVFS2_OFFSET_STEP	Selection of the offset step for DVFS2 function: 0: offset step of 10mV (default) 1: offset step of 20mV	RW	0
0	DVFS2_ENABLE	Selection of the DVFS2 function: 0: DVFS2 is not enabled (default) 1: DVFS2 is enabled (Control of SMPS6) DVFS2 function in link to DVFS2_CLK (GPADC_START input) and DVFS2_DAT (GPIO_6 input mode selected).	RW	0

1.7.2.5 SMPS_DVFS2_VOLTAGE_MAX Register

Table 1-102. SMPS_DVFS2_VOLTAGE_MAX

Address offset	0x04	**I2C Address**	0x48
Physical Address	0x184 **Instance**	FUNC_DVFS	
Description	ES1.0: Reserved register ES2.0->: SMPS DVFS2 maximum voltage register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
LOCK	VOLTAGE_MAX						

Bits	Field Name	Description	Type	Reset
7	LOCK	Access protection of the DVFS1_VOLTAGE_MAX register 0: No protection. R/W access to these register bits 1: Protection of these registers (Read only). This bit will reset (0b0) during HWRST SWITCH-OFF	RW	0
6:0	VOLTAGE_MAX	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register with RANGE[0]=0 (x1 multiplier) and VSEL range from OFF, 0.5 to 1.65V	RW	0x00

1.7.2.6 SMPS_DVFS2_STATUS Register

Table 1-103. SMPS_DVFS2_STATUS

Address offset	0x05			**I2C Address**	0x48
Physical Address	0x185	**Instance**		FUNC_DVFS	
Description	ES1.0: Reserved register ES2.0->: SMPS DVFS2 status register RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved		OFFSET_STATUS					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	OFFSET_STATUS	Offset status register (between 0 and 32 in decimal) SMPS_DVFS_CTRL.DVFS2_OFFSET_STEP=0 (x1 multiplier, 10mv per step)/ 1(x2 multiplier), 20mV per step) 000000: no offset 000001: 10mV/20mV 000010: 20mV/40mV ... 100000: 320mV/640mV 100001: reserved/reserved .. 111111: reserved/reserved	RO	0x00

1.8 FUNC_PMU_CONTROL Registers

1.8.1 FUNC_PMU_CONTROL Registers Mapping Summary

This section provides information on the FUNC_PMU_CONTROL Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.8.1.1 FUNC_PMU_CONTROL Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
DEV_CTRL	RW	8	0x01	0x48	0x00	0x1A0
POWER_CTRL	RW	8	0x07	0x48	0x01	0x1A1
VSYS_LO	RO	8	0b000X XXXX	0x48	0x02	0x1A2
VSYS_MON	RW	8	0b00XX XXXX	0x48	0x03	0x1A3
VBAT_MON	RW	8	0b00XX XXXX	0x48	0x04	0x1A4
WATCHDOG	RW	8	0x07	0x48	0x05	0x1A5
BOOT_STATUS	RO	8	0x00	0x48	0x06	0x1A6
BATTERY_BOUNCE	RW	8	0x00	0x48	0x07	0x1A7
BACKUP_BATTERY_CTRL	RW	8	0bX111 1010	0x48	0x08	0x1A8
LONG_PRESS_KEY	RW	8	0b0011 11XX	0x48	0x09	0x1A9
OSC_THERM_CTRL	RW	8	0x0C	0x48	0x0A	0x1AA
BATDEBOUNCING	RW	8	0x80	0x48	0x0B	0x1AB
SWOFF_HWRST	RO	8	0xXX	0x48	0x0F	0x1AF
SWOFF_COLDRST	RW	8	0xXX	0x48	0x10	0x1B0
SWOFF_STATUS	RO	8	0x00	0x48	0x11	0x1B1
PMU_CONFIG	RW	8	0b0XXX XXXX	0x48	0x12	0x1B2
SPARE	RW	8	0xXX	0x48	0x14	0x1B4
PMU_SECONDARY_INT	RW	8	0x0X	0x48	0x15	0x1B5

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
SW_REVISION	RO	8	0xXX	0x48	0x17	0x1B7
EXT_CHRG_CTRL	RW	8	0b0000 X0XX	0x48	0x18	0x1B8
PMU_SECONDARY_INT2	RW	8	0x00	0x48	0x19	0x1B9

1.8.2 FUNC_PMU_CONTROL Register Descriptions

1.8.2.1 DEV_CTRL Register

Table 1-104. DEV_CTRL

Address offset	0x00	**I2C Address**	0x48
Physical Address	0x1A0 **Instance**	FUNC_PMU_CONTROL	
Description	Device Control Register RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				DEV_STATUS		SW_RST	DEV_ON

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:2	DEV_STATUS	Device status 00: OFF 01: ACTIVE 10: Not applicable (ACTIVE) 11: SLEEP	RO	0x0
1	SW_RST	Software Reset (SW_RST) Writing 1 will restart the device (turn-off sequence followed by turn-on sequence) This bit is cleared automatically	RW	0
0	DEV_ON	Device ON enable 1: will maintain the device in ACTIVE mode 0: allow the device to go in OFF mode	RW	1

1.8.2.2 POWER_CTRL Register

Table 1-105. POWER_CTRL

Address offset	0x01	**I2C Address**	0x48
Physical Address	0x1A1 **Instance**	FUNC_PMU_CONTROL	
Description	Power control register RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					ENABLE2_MASK	ENABLE1_MASK	NSLEEP_MASK

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2	ENABLE2_MASK	Enable of the ENABLE2 line (mask) 0: ENABLE2 is not masked (allow control of the resource with ENABLE2 pin) 1: ENABLE2 is masked (does not affect resource control) (default) Note: In QFN configuration, this ENABLE2 pin is not bounded. This register bit is still visible and it is recommanded to keep the defaut value (reset value - masked) to guaranteer the right behaviour.	RW	1
1	ENABLE1_MASK	Enable of the ENABLE1 line (mask) 0: ENABLE1 is not masked (allow control of the resource with ENABLE1 pin) 1: ENABLE1 is masked (does not affect resource control) (default)	RW	1
0	NSLEEP_MASK	Enable of the NSLEEP line (mask) 0: NSLEEP is not masked (allow control of the resource with NSLEEP pin) 1: NSLEEP is masked (does not affect resource control) (default)	RW	1

1.8.2.3 VSYS_LO Register

Table 1-106. VSYS_LO

Address offset	0x02	**I2C Address**	0x48
Physical Address	0x1A2 **Instance**	FUNC_PMU_CONTROL	
Description	VSYS Low threshold register RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
Reserved			THRESHOLD				

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:0	THRESHOLD	VSYS_LO - System voltage falling edge threshold. When VCCx input falls below VSYS_LO, device enters OFF mode and is ready for start-up event. Configured by OTP bits. From 2.5V to 3.10V per 50mV step. 00000 = 2.300 V (Reserved) 00001 = 2.050 V (Reserved) 00010 = 2.100 V (Reserved) 00011 = 2.150 V (Reserved) 00100 = 2.200 V (Reserved) 00101 = 2.250 V (Reserved) 00110 = 2.300 V (Reserved) 00111 = 2.350 V (Reserved) 01000 = 2.400 V (Reserved) 01001 = 2.450 V (Reserved) 01010 = 2.500 V 01011 = 2.550 V 01100 = 2.600 V 01101 = 2.650 V 01110 = 2.700 V 01111 = 2.750 V 10000 = 2.800 V 10001 = 2.850 V 10010 = 2.900 V 10011 = 2.950 V 10100 = 3.000 V 10101 = 3.050 V 10110 = 3.100V 10111 = Reserved .. 11111 = Reserved	RO	0bX XXXX

1.8.2.4 VSYS_MON Register

Table 1-107. VSYS_MON

Address offset	0x03	**I2C Address**	0x48
Physical Address	0x1A3 **Instance**	FUNC_PMU_CONTROL	
Description	VSYS Monitoring register. This register is initialized by OTP memory. The software can overwrite this value by a new value (VSYS_MON - from 2.3V to 4.6V). RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
ENABLE	Reserved	THRESHOLD					

Bits	Field Name	Description	Type	Reset
7	ENABLE	Enable VSYS monitoring (only in ACTIVE /SLEEP) 0: VSYS monitoring is not enabled 1: VSYS monitoring is enabled	RW	0
6	Reserved		RO	0
5:0	THRESHOLD	VSYS_HI Configured by OTP bits. By SW, from 2.3V to 4.6V per 50mV step. 000000 = 2.30 V 100000 = 3.60 V 000001 = 2.30 V 100001 = 3.65 V 000010 = 2.30 V 100010 = 3.70 V 000011 = 2.30 V 100011 = 3.75 V 000100 = 2.30 V 100100 = 3.80 V 000101 = 2.30 V 100101 = 3.85 V 000110 = 2.30 V 100110 = 3.90 V 000111 = 2.35 V 100111 = 3.95 V 001000 = 2.40 V 101000 = 4.00 V 001001 = 2.45 V 101001 = 4.05 V 001010 = 2.50 V 101010 = 4.10 V 001011 = 2.55 V 101011 = 4.15 V 001100 = 2.60 V 101100 = 4.20 V 001101 = 2.65 V 101101 = 4.25 V 001110 = 2.70 V 101110 = 4.30 V 001111 = 2.75 V 101111 = 4.35 V 010000 = 2.80 V 110000 = 4.40 V 010001 = 2.85 V 110001 = 4.45 V 010010 = 2.90 V 110010 = 4.50 V 010011 = 2.95 V 110011 = 4.55 V 010100 = 3.00 V 110100 = 4.60 V 010101 = 3.05 V 110101 = 4.60 V 010110 = 3.10 V 110110 = 4.60 V 010111 = 3.15 V 110111 = 4.60 V 011000 = 3.20 V 111000 = 4.60 V 011001 = 3.25 V 111001 = 4.60 V 011010 = 3.30 V 111010 = 4.60 V 011011 = 3.35 V 111011 = 4.60 V 011100 = 3.40 V 111100 = 4.60 V 011101 = 3.45 V 111101 = 4.60 V 011110 = 3.50 V 111110 = 4.60 V 011111 = 3.55 V 111111 = 4.60 V	RW	0bXX XXXX

1.8.2.5 VBAT_MON Register

Table 1-108. VBAT_MON

Address offset	0x04	**I2C Address**	0x48
Physical Address	0x1A4 **Instance**	FUNC_PMU_CONTROL	
Description	VBAT Monitoring register. This register is initialized by OTP memory (VBAT_HI). The software can overwrite this value by a new value (VBAT_MON). RESET register domain: HWRST (excepted ENABLE which is on SWORST)		
Type	RW		

7	6	5	4	3	2	1	0
ENABLE	Reserved	THRESHOLD					

Bits	Field Name	Description	Type	Reset
7	ENABLE	enable VBAT monitoring (only in ACTIVE /SLEEP) 0: VBAT monitoring is not enabled 1: VBAT monitoring is enabled	RW	0
6	Reserved		RO	0
5:0	THRESHOLD	VBAT_HI Configured by OTP bits. From 2.3V to 4.6V per 50mV step. 000000 = 2.30 V 100000 = 3.60 V 000001 = 2.30 V 100001 = 3.65 V 000010 = 2.30 V 100010 = 3.70 V 000011 = 2.30 V 100011 = 3.75 V 000100 = 2.30 V 100100 = 3.80 V 000101 = 2.30 V 100101 = 3.85 V 000110 = 2.30 V 100110 = 3.90 V 000111 = 2.35 V 100111 = 3.95 V 001000 = 2.40 V 101000 = 4.00 V 001001 = 2.45 V 101001 = 4.05 V 001010 = 2.50 V 101010 = 4.10 V 001011 = 2.55 V 101011 = 4.15 V 001100 = 2.60 V 101100 = 4.20 V 001101 = 2.65 V 101101 = 4.25 V 001110 = 2.70 V 101110 = 4.30 V 001111 = 2.75 V 101111 = 4.35 V 010000 = 2.80 V 110000 = 4.40 V 010001 = 2.85 V 110001 = 4.45 V 010010 = 2.90 V 110010 = 4.50 V 010011 = 2.95 V 110011 = 4.55 V 010100 = 3.00 V 110100 = 4.60 V 010101 = 3.05 V 110101 = 4.60 V 010110 = 3.10 V 110110 = 4.60 V 010111 = 3.15 V 110111 = 4.60 V 011000 = 3.20 V 111000 = 4.60 V 011001 = 3.25 V 111001 = 4.60 V 011010 = 3.30 V 111010 = 4.60 V 011011 = 3.35 V 111011 = 4.60 V 011100 = 3.40 V 111100 = 4.60 V 011101 = 3.45 V 111101 = 4.60 V 011110 = 3.50 V 111110 = 4.60 V 011111 = 3.55 V 111111 = 4.60 V	RW	0bXX XXXX

1.8.2.6 WATCHDOG Register

Table 1-109. WATCHDOG

Address offset	0x05	**I2C Address**	0x48
Physical Address	0x1A5 **Instance**	FUNC_PMU_CONTROL	
Description	Watch dog timer Register RESET register domain: SWORST NOTES: â€¢ The WATCHDOG.TIMER counter is initialized with the RESET_OUT=0 â€¢ The WATCHDOG.TIMER counter starts as soon as RESET_OUT is released.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		LOCK	ENABLE	MODE	TIMER		

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5	LOCK	Access protection of the WATCHDOG.ENABLE, WATCHDOC.MODE and WATCHDOG.LOCK bits 0: No protection. R/W access to these register bits 1: Protection of these registers (Read only). This bit will reset (0b0) during SWITCH-OFF	RW	0
4	ENABLE	Selection of the Watchdog: 0: Watchdog is not selected (disable) (default) 1: Watchdog is elected (enabled)	RW	0
3	MODE	Select type of watchdog behavior: 0: Periodic (default) 1: Interrupt mode	RW	0
2:0	TIMER	Timer delay selection: 000: 1s 001: 2s 010: 4s 011: 8s 100: 16s 101: 32s 110: 64s 111: 128s (default)	RW	0x7

1.8.2.7 BOOT_STATUS Register

Table 1-110. BOOT_STATUS

Address offset	0x06	**I2C Address**	0x48
Physical Address	0x1A6 **Instance**	FUNC_PMU_CONTROL	
Description	BOOT status register. Provide a copy of the boot pins RESET register domain: POR NOTES: This register is updated during the power transition from NOSUPPLY to WAITON state.		
Type	RO		

7	6	5	4	3	2	1	0
Reserved						BOOT1	BOOT0

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1	BOOT1	Provide a copy of the BOOT1 pin	RO	0
0	BOOT0	Provide a copy of the BOOT0 pin	RO	0

1.8.2.8 BATTERY_BOUNCE Register

Table 1-111. BATTERY_BOUNCE

Address offset	0x07	**I2C Address**	0x48
Physical Address	0x1A7 **Instance**	FUNC_PMU_CONTROL	
Description	Battery Bounce (BB) Register. If a good system voltage/battery is detected before the delay counter expiration (short disconnect), system will restart if previous state was ACTIVE or SLEEP. If previous state was WAIT-ON or if the counter delay expires, system waits for a SWITCH-ON event to restart. RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		BB_DELAY					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	BB_DELAY	Battery Bounce delay Minimum: BB_DELAY x 64 ms + 32 ms Maximum: BB_DELAY x 64 ms + 48 ms Note that the power cut accuracy is Â±16 ms 000000: 0 = 0 + 32mS (min) (default) .. 111111: 63 = 4.032s + 48ms (max) Note: Timing are specified +/- 2%	RW	0x00

1.8.2.9 BACKUP_BATTERY_CTRL Register

Table 1-112. BACKUP_BATTERY_CTRL

Address offset	0x08	**I2C Address**	0x48
Physical Address	0x1A8 **Instance**	FUNC_PMU_CONTROL	
Description	Backup Battery Control Register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
VRTC_18_15	VRTC_EN_SLP	VRTC_EN_OFF	VRTC_PWEN	BBS_BBC_LOW_ICHRG	BB_SEL		BB_CHG_EN

Bits	Field Name	Description	Type	Reset
7	VRTC_18_15	VRTC voltage selection. This bit will allow to decrease the power consumption in BACKUP mode by setting the VRCT at 1.5V. 0: 1.8V (default) 1: 1.5V ES1.0: This bit is RW ES2.0->: This bit is RO (controlled by OTP-TRIM)	RO	X
6	VRTC_EN_SLP	0: VRTC is configured in the standard power mode configuration when device is in SLEEP state (biasing also in SLEEP state). 1: VRTC is configured in a low-power mode configuration when device is in SLEEP state (biasing also in SLEEP state) (default).	RW	1

Bits	Field Name	Description	Type	Reset
5	VRTC_EN_OFF	0: ES1.0: VRTC is configured in the standard power mode configuration when device is in OFF state (biasing also in OFF state) (default). 0: ES2.0->: VRTC is configured in the standard power mode configuration when device is in OFF state (biasing also in OFF state) 1: ES1.0: VRTC is configured in a low-power mode configuration when device is in OFF state (biasing also in OFF state). 1: ES2.0->: VRTC is configured in a low-power mode configuration when device is in OFF state (biasing also in OFF state) (default).	RW	1
4	VRTC_PWEN	0: VRTC is configured in a low-power mode configuration. 1: VRTC is configured in the standard power mode configuration (default)	RW	1
3	BBS_BBC_LOW_ICHRG	Backup battery current charge selection 0: with current > 100uA 1: with current < 100uA (default)	RW	1
2:1	BB_SEL	Backup Battery (BB) end of charge voltage selection 00: 3.0V 01: 2.5V (default) 10: 3.15V 11: VBAT	RW	0x1
0	BB_CHG_EN	Backup Battery (BB) feature enabling 0: The Backup Battery (BB) charge is disabled (default) 1: The Backup Battery (BB) charge is enabled	RW	0

1.8.2.10 LONG_PRESS_KEY Register

Table 1-113. LONG_PRESS_KEY

Address offset	0x09	**I2C Address**	0x48
Physical Address	0x1A9 **Instance**	FUNC_PMU_CONTROL	
Description	Long Press Key (LPK) configuration register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
LPK_LOCK	Reserved	Reserved	LPK_INT_CLR	LPK_TIME		PWRON_DEBOUNCE	

Bits	Field Name	Description	Type	Reset
7	LPK_LOCK	Access protection of the LPK_TIME, LPK_INT_CLR, LPK_EN and LPK_LOCK registers 0: No protection. R/W access to these register bits (default) 1: Protection of these registers (Read only). This bit will reset (0b0) during SWITCH-OFF	RW	0
6	Reserved		RO	0
5	Reserved		RO	1
4	LPK_INT_CLR	Interrupt clear behavior configuration. Interrupt is generated when Long Key Press is detected. Switch OFF will occur X delay after interrupt detection. Interrupt clear will have two behavior based on bit configuration. 0: Switch OFF cannot be cancelled if both PWRON and RPWON low. It mean if only PWRON used and interrupt clear, it cancel Switch OFF. In this case, no ways to stop the switch off if PWRON and RPWRON maintained low If RPWRON is high an PWRON is low, Switch off only if interrupt is not cleared. 1: Switch OFF cannot be cancelled when PWRON maintains low (default).	RW	1

Bits	Field Name	Description	Type	Reset
3:2	LPK_TIME	Long press key duration 00: 6 second 01: 8 second 10: 10 second 11: 12 second (default)	RW	0x3
1:0	PWRON_DEBOUNCE	Key Press PWRON debounce timing selection 00= 15ms 01= 100ms 10= 500ms 11= 1s	RW	0bXX

1.8.2.11 OSC_THERM_CTRL Register

Table 1-114. OSC_THERM_CTRL

Address offset	0x0A	**I2C Address**	0x48
Physical Address	0x1AA **Instance**	FUNC_PMU_CONTROL	
Description	Oscillator and Thermal control register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
VANA_ON_IN_SLEEP	INT_MASK_IN_SLEEP	RC15MHZ_ON_IN_SLEEP	THERM_OFF_IN_SLEEP	THERM_HD_SEL		OSC_BYPASS	OSC_HPMODE

Bits	Field Name	Description	Type	Reset
7	VANA_ON_IN_SLEEP	ES1.0: Reserved bit ES2.0->: VANA LDO selection during SLEEP mode 0: VANA LDO is OFF in SLEEP mode (default) 1: VANA LDO is ON in SLEEP mode (In case some modules are used in SLEEP mode and need VANA (USB OTG, ILMON))	RW	0
6	INT_MASK_IN_SLEEP	INT masked selection during SLEEP mode (Released interrupt line only when DEVICE fully wake up) 0: INT is not masked in SLEEP mode (default) 1: INT is asserted when SLEEP2ACTIVE transition is completed (allow to wakeup platform before INT generation)	RW	0
5	RC15MHZ_ON_IN_SLEEP	RC15MHZ oscillator selection during SLEEP mode 0: RC15MHZ oscillator is OFF in SLEEP mode. Minimize consumption in SLEEP mode (default) 1: RC15MHZ oscillator is ON in SLEEP mode. It allow to make I2C/SPI access in SLEEP mode.	RW	0
4	THERM_OFF_IN_SLEEP	THERM selection during SLEEP mode (Minimization of the power consumption) 0: THERM is ON in SLEEP mode (default) 1: THERM is OFF in SLEEP mode	RW	0
3:2	THERM_HD_SEL	Hot die temperature detection selection: 00: 117 / 108 deg. 01: 121 / 112 deg. 10: 125 / 116 deg. 11: 130 / 120 deg. (default)	RW	0x3

Bits	Field Name	Description	Type	Reset
1	OSC_BYPASS	Oscillator 32KHz bypass selection (internal/external) 0: Internal Oscillator 32KHz is used (default) 1: Internal Oscillator is not used (bypassed). A square wave should be applied on OSC32KIN pin.	RW	0
0	OSC_HPMODE	Performance oscillator selection 0: Oscillator 32KHz is configured in normal mode 1: Oscillator 32KHz is configured in high performance mode	RW	0

1.8.2.12 BATDEBOUNCING Register

Table 1-115. BATDEBOUNCING

Address offset	0x0B	**I2C Address**	0x48
Physical Address	0x1AB **Instance**	FUNC_PMU_CONTROL	
Description	Battery debouncing register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
BAT_DEB_BYPASS	BINS_DEB				BEXT_DEB		

Bits	Field Name	Description	Type	Reset
7	BAT_DEB_BYPASS	0: Battery de-bouncing enabled (Duration selected by BINS_DEB / BEXT_DEB bits) 1: Battery de-bouncing bypassed (No debouncing) (default)	RW	1
6:3	BINS_DEB	Battery insertion de-bouncing time 0000: de-bouncing time 0.5ms (default state) 0001: de-bouncing time 1ms â€¦ 1111: de-bouncing time 8ms NOTE: Insertion de-bouncing step is 0.5ms WARNING: If BATDEBOUNCING.BEXT_DEB is set to 0b000, the BATDEBOUNCING.BINS_DEB will be set to 62.5us in all the case.	RW	0x0
2:0	BEXT_DEB	Battery extraction de-bouncing time 000: de-bouncing time ES1.0: 31.25us (default state) ES2.0->: 62.5us (default state) 001: de-bouncing time ES1.0: 62.5us ES2.0->: 93.75us â€¦ 111: de-bouncing time ES1.0:250us ES2.0->:281.25us NOTE: Extraction de-bouncing step is 31.25us	RW	0x0

1.8.2.13 SWOFF_HWRST Register

Table 1-116. SWOFF_HWRST

Address offset	0x0F	**I2C Address**	0x48
Physical Address	0x1AF **Instance**	FUNC_PMU_CONTROL	
Description	Qualify which switch off events generate a HW RESET (configuration of behavior of the device) RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
PWRON_LPK	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN

Bits	Field Name	Description	Type	Reset
7	PWRON_LPK	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)	RO	X
6	PWRDOWN	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)	RO	X
5	WTD	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)	RO	X
4	TSHUT	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)	RO	X
3	RESET_IN	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)	RO	X
2	SW_RST	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)	RO	X
1	VSYS_LO	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)	RO	X
0	GPADC_SHUTDOWN	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)	RO	X

1.8.2.14 SWOFF_COLDRST Register

Table 1-117. SWOFF_COLDRST

Address offset	0x10	**I2C Address**	0x48
Physical Address	0x1B0 **Instance**	FUNC_PMU_CONTROL	
Description	Qualify which switch off events generate a COLD RESET (configuration of behavior of the device) RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
PWRON_LPK	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN

Bits	Field Name	Description	Type	Reset
7	PWRON_LPK	0: Masked (Shutdown) 1: Not masked (Cold restart)	RW	X
6	PWRDOWN	0: Masked (Shutdown) 1: Not masked (Cold restart)	RW	X
5	WTD	0: Masked (Shutdown) 1: Not masked (Cold restart)	RW	X
4	TSHUT	0: Masked (Shutdown) 1: Not masked (Cold restart)	RW	X
3	RESET_IN	0: Masked (Shutdown) 1: Not masked (Cold restart)	RW	X
2	SW_RST	0: Masked (Shutdown) 1: Not masked (Cold restart)	RW	X
1	VSYS_LO	0: Masked (Shutdown) 1: Not masked (Cold restart)	RW	X
0	GPADC_SHUTDOWN	0: Masked (Shutdown) 1: Not masked (Cold restart)	RW	X

1.8.2.15 SWOFF_STATUS Register

Table 1-118. SWOFF_STATUS

Address offset	0x11	**I2C Address**	0x48
Physical Address	0x1B1 **Instance**	FUNC_PMU_CONTROL	
Description	Qualify which switch off events generate a HW RESET RESET register domain: PORRST		
Type	RO		

7	6	5	4	3	2	1	0
PWRON_LPK	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN

Bits	Field Name	Description	Type	Reset
7	PWRON_LPK		RO RtoClr	0
6	PWRDOWN		RO RtoClr	0
5	WTD		RO RtoClr	0
4	TSHUT		RO RtoClr	0
3	RESET_IN		RO RtoClr	0
2	SW_RST		RO RtoClr	0
1	VSYS_LO		RO RtoClr	0
0	GPADC_SHUTDOWN		RO RtoClr	0

1.8.2.16 PMU_CONFIG Register

Table 1-119. PMU_CONFIG

Address offset	0x12	**I2C Address**	0x48
Physical Address	0x1B2 **Instance**	FUNC_PMU_CONTROL	
Description	PMU configuration RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	MULTI_CELL_EN	SPARE5	SPARE4	SWOFF_DLY		GATE_RESET_OUT	AUTODEVON

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	MULTI_CELL_EN	MULTI Cell battery selection 0: Multi-Cell battery not enabled (one cell) 1: Multi-Cell battery enabled	RW	X
5	SPARE5		RW	X
4	SPARE4		RW	X
3:2	SWOFF_DLY	Delay before to go to SWITCH-OFF to allow host processor to save his context (device will be maintained ACTIVE until delay expiration then SWITCH-OFF) 00: no delay 01: 1 second window (+/- 250ms) 10: 2 second window (+/- 250ms) 11: 4 second window (+/- 250ms)	RW	0bXX
1	GATE_RESET_OUT	Gating of RESET_OUT with Crystal oscillator status 0: RESET_OUT not gated 1: RESET_OUT released when crystal oscillator is ready	RW	X
0	AUTODEVON	Selection of the feature Auto Device ON 0: Feature is inactive 1: Feature is active	RW	X

1.8.2.17 SPARE Register

Table 1-120. SPARE

Address offset	0x14	**I2C Address**	0x48
Physical Address	0x1B4 **Instance**	FUNC_PMU_CONTROL	
Description	SPARE register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
SPARE					REGEN3_OD	REGEN2_OD	REGEN1_OD

Bits	Field Name	Description	Type	Reset
7:3	SPARE	SPARE register	RW	0bX XXXX
2	REGEN3_OD	ES1.0: Reserved ES2.0->: REGEN3_OD implementation (Push-Pull/OD selection) 0: open drain not enable (Push-Pull enabled) 1: open drain enable (Push-Pull not enable)	RW	X

Bits	Field Name	Description	Type	Reset
1	REGEN2_OD	0: open drain not enable (Push-Pull enabled) 1: open drain enable (Push-Pull not enable)	RW	X
0	REGEN1_OD	0: open drain not enable (Push-Pull enabled) 1: open drain enable (Push-Pull not enable)	RW	X

1.8.2.18 PMU_SECONDARY_INT Register

Table 1-121. PMU_SECONDARY_INT

Address offset	0x15	**I2C Address**	0x48
Physical Address	0x1B5 **Instance**	FUNC_PMU_CONTROL	
Description	Configuration and status of the Secondary Interrupt Handler RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
VBUS_OVV_INT_SRC	CHARG_DET_N_INT_SRC	BB_INT_SRC	FBI_INT_SRC	VBUS_OVV_MASK	CHARG_DET_N_MASK	BB_MASK	FBI_MASK

Bits	Field Name	Description	Type	Reset
7	VBUS_OVV_INT_SRC	VBUS over-voltage (VBUS_OVV) interrupt status source 0: VBUS over-voltage (VBUS_OVV) is not the source of interrupt line CHARG_DET_N_USB_OVV 1: VBUS over-voltage (VBUS_OVV) is the source of interrupt line CHARG_DET_N_USB_OVV	RO RtoClr	0
6	CHARG_DET_N_INT_SRC	Charger detection (CHARG_DET_N) interrupt status source 0: Charger detection (CHARG_DET_N) is not the source of interrupt line CHARG_DET_N_USB_OVV 1: Charger detection (CHARG_DET_N) is the source of interrupt line CHARG_DET_N_USB_OVV	RO RtoClr	0
5	BB_INT_SRC	Battery Bounce (BB) interrupt status source 0: Battery Bounce (BB) is not the source of interrupt line BB_FBI 1: Battery Bounce (BB) is the source of interrupt line BB_FBI	RO RtoClr	0
4	FBI_INT_SRC	First Battery Insertion (FBI) interrupt status source 0: First Battery Insertion (FBI) is not the source of interrupt line BB_FBI 1: First Battery Insertion (FBI) is the source of interrupt line BB_FBI	RO RtoClr	0
3	VBUS_OVV_MASK	CHARG_DET_N_VBUS_OVV interrupt selection - VBUS over-voltage 0: Un-masked 1: Masked	RW	X
2	CHARG_DET_N_MASK	CHARG_DET_N_VBUS_OVV interrupt selection - CHARG_DET_N interrupt mask 0: Un-masked 1: Masked	RW	X
1	BB_MASK	Secondary level of mask for FBI_BB interrupt line. Battery Bounce (BB) Mask. 0: Un-masked 1: Masked	RW	X

Bits	Field Name	Description	Type	Reset
0	FBI_MASK	Secondary level of mask for FBI_BB interrupt line. First Battery Insertion (FBI) Mask. 0: Un-masked 1: Masked	RW	X

1.8.2.19 SW_REVISION Register

Table 1-122. SW_REVISION

Address offset	0x17	**I2C Address**	0x48
Physical Address	0x1B7 **Instance**	FUNC_PMU_CONTROL	
Description	Software (SW) revision register RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
SW_REVISION							

Bits	Field Name	Description	Type	Reset
7:0	SW_REVISION	Software (SW) revision register - This revision will be representative of the OTP version.	RO	0xXX

1.8.2.20 EXT_CHRG_CTRL Register

Table 1-123. EXT_CHRG_CTRL

Address offset	0x18	**I2C Address**	0x48
Physical Address	0x1B8 **Instance**	FUNC_PMU_CONTROL	
Description	PMU configuration #3 RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
VBUS_OVV_STATUS	CHARG_DET_N_STATUS	Reserved		VSYS_DEBOUNCE_DELAY	CHRG_DET_N	AUTO_ACA_EN	AUTO_LDOUSB_EN

Bits	Field Name	Description	Type	Reset
7	VBUS_OVV_STATUS	Status of the level of the VBUS_OVV 0: No Over-voltage 1: Over-voltage	RO	0
6	CHARG_DET_N_STATUS	Status of the level of the CHARG_DET_N input	RO	0
5:4	Reserved		RO	0x0
3	VSYS_DEBOUNCE_DELAY	Selection of VSYS_MIN_HI debounce 0: 100us in all the case 1: 1s if VBUS plug	RW	X

Bits	Field Name	Description	Type	Reset
2	CHRG_DET_N	CHRG_DET_N status bit. This bit can be force to simulate a charger presence. 0: No charger detected (default) 1: Charger detected (status) - Clear on VBUS un-plug or write '1' will force charger detection with force of USB_PSEL pin to '1' (if USB_PSEL used as secondary function)	RW	0
1	AUTO_ACA_EN	ACA selection enable on VBUS detection 0: ACA is disabled on VBUS detection 1: ACA is enabled on VBUS detection	RW	X
0	AUTO_LDOUSB_EN	LDOUSB selection enable on VBUS detection 0: LDOUSB is disabled on VBUS detection 1: LDOUSB is enabled on VBUS detection	RW	X

1.8.2.21 PMU_SECONDARY_INT2 Register

Table 1-124. PMU_SECONDARY_INT2

Address offset	0x19	**I2C Address**	0x48
Physical Address	0x1B9 **Instance**	FUNC_PMU_CONTROL	
Description	ES1.0: Reserved register ES2.0->: Configuration and status of the Secondary Interrupt Handler (Register2) RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		DVFS2_INT_SRC	DVFS1_INT_SRC	Reserved		DVFS2_MASK	DVFS1_MASK

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO RtoClr	0x0
5	DVFS2_INT_SRC	DVFS2 (Voltage plus offset over voltage max) interrupt status source 0: DVFS2 (Voltage plus offset over voltage max) is not the source of interrupt line 1: DVFS2 (Voltage plus offset over voltage max) is the source of interrupt line	RO RtoClr	0
4	DVFS1_INT_SRC	DVFS1 (Voltage plus offset over voltage max) interrupt status source 0: DVFS1 (Voltage plus offset over voltage max) is not the source of interrupt line 1: DVFS1 (Voltage plus offset over voltage max) is the source of interrupt line	RO RtoClr	0
3:2	Reserved		RO	0x0
1	DVFS2_MASK	Secondary level of mask for DVFS2 interrupt line. Voltage plus offset over voltage max mask. 0: Un-masked 1: Masked	RW	0
0	DVFS1_MASK	Secondary level of mask for DVFS1 interrupt line. Voltage plus offset over voltage max mask. 0: Un-masked 1: Masked	RW	0

1.9 FUNC_RESOURCE Registers

1.9.1 FUNC_RESOURCE Registers Mapping Summary

This section provides information on the FUNC_RESOURCE Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.9.1.1 FUNC_RESOURCE Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
CLK32KG_CTRL	RW	8	0b0000 000X	0x48	0x00	0x1D4
CLK32KGAUDIO_CTRL	RW	8	0b0000 000X	0x48	0x01	0x1D5
REGEN1_CTRL	RW	8	0b0000 000X	0x48	0x02	0x1D6
REGEN2_CTRL	RW	8	0b0000 000X	0x48	0x03	0x1D7
SYSEN1_CTRL	RW	8	0b0000 000X	0x48	0x04	0x1D8
SYSEN2_CTRL	RW	8	0b0000 000X	0x48	0x05	0x1D9
NSLEEP_RES_ASSIGN	RW	8	0x00	0x48	0x06	0x1DA
NSLEEP_SMPS_ASSIGN	RW	8	0x00	0x48	0x07	0x1DB
NSLEEP_LDO_ASSIGN1	RW	8	0x00	0x48	0x08	0x1DC
NSLEEP_LDO_ASSIGN2	RW	8	0x00	0x48	0x09	0x1DD
ENABLE1_RES_ASSIGN	RW	8	0x00	0x48	0x0A	0x1DE
ENABLE1_SMPS_ASSIGN	RW	8	0x00	0x48	0x0B	0x1DF
ENABLE1_LDO_ASSIGN1	RW	8	0x00	0x48	0x0C	0x1E0
ENABLE1_LDO_ASSIGN2	RW	8	0x00	0x48	0x0D	0x1E1
ENABLE2_RES_ASSIGN	RW	8	0x00	0x48	0x0E	0x1E2
ENABLE2_SMPS_ASSIGN	RW	8	0x00	0x48	0x0F	0x1E3
ENABLE2_LDO_ASSIGN1	RW	8	0x00	0x48	0x10	0x1E4
ENABLE2_LDO_ASSIGN2	RW	8	0x00	0x48	0x11	0x1E5
REGEN3_CTRL	RW	8	0b0000 000X	0x48	0x12	0x1E6

1.9.2 FUNC_RESOURCE Register Descriptions

1.9.2.1 CLK32KG_CTRL Register

Table 1-125. CLK32KG_CTRL

Address offset	0x00			**I2C Address**	0x48
Physical Address	0x1D4	**Instance**		FUNC_RESOURCE	
Description	CLK32KG control register RESET register domain: SWORST Note: In QFN configuration, this pin is not bounded. This register is still visible and it is recommanded to keep the defaut values (reset value)				
Type	RW				

7	6	5	4	3	2	1	0
Reserved			STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	STATUS	CLK32KG Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	CLK32KG SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	CLK32KG ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON	RW	X

1.9.2.2 CLK32KGAUDIO_CTRL Register

Table 1-126. CLK32KGAUDIO_CTRL

Address offset	0x01	**I2C Address**	0x48
Physical Address	0x1D5 **Instance**	FUNC_RESOURCE	
Description	CLK32KGAUDIO control register RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			STATUS	RESERVED	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	STATUS	CLK32KGAUDIO Status 0: OFF 1: ON	RO	0
3	RESERVED	This bit field is reserved.	RO	0
2	MODE_SLEEP	CLK32KGAUDIO SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	CLK32KGAUDIO ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON	RW	X

1.9.2.3 REGEN1_CTRL Register

Table 1-127. REGEN1_CTRL

Address offset	0x02	**I2C Address**	0x48
Physical Address	0x1D6 **Instance**	FUNC_RESOURCE	
Description	REGEN1 control register RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	STATUS	REGEN1 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	REGEN1 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	REGEN1 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON	RW	X

1.9.2.4 REGEN2_CTRL Register

Table 1-128. REGEN2_CTRL

Address offset	0x03	**I2C Address**	0x48
Physical Address	0x1D7 **Instance**	FUNC_RESOURCE	
Description	REGEN2 control register RESET register domain: SWORST Note: In QFN configuration, this pin is not bounded. This register is still visible and it is recommanded to keep the defaut values (reset value)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	STATUS	REGEN2 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0

Bits	Field Name	Description	Type	Reset
2	MODE_SLEEP	REGEN2 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	REGEN2 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON	RW	X

1.9.2.5 SYSEN1_CTRL Register

Table 1-129. SYSEN1_CTRL

Address offset	0x04	**I2C Address**	0x48
Physical Address	0x1D8 **Instance**	FUNC_RESOURCE	
Description	SYSEN1 (GPIO_4 secondary function) control register RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	STATUS	SYSEN1 Status 0: OFF 1: ON	RW	0
3	Reserved		RO	0
2	MODE_SLEEP	GPIO_4 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	GPIO_4 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON	RW	X

1.9.2.6 SYSEN2_CTRL Register

Table 1-130. SYSEN2_CTRL

Address offset	0x05	**I2C Address**	0x48
Physical Address	0x1D9 **Instance**	FUNC_RESOURCE	
Description	SYSEN1 (GPIO_6 secondary function) control register RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	STATUS	SYSEN2 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	GPIO_6 SLEEP Mode 0: OFF 1: ON	RW	0
1	Reserved		RO	0
0	MODE_ACTIVE	GPIO_6 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON	RW	X

1.9.2.7 NSLEEP_RES_ASSIGN Register

Table 1-131. NSLEEP_RES_ASSIGN

Address offset	0x06	**I2C Address**	0x48
Physical Address	0x1DA **Instance**	FUNC_RESOURCE	
Description	NSLEEP resource assignment register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	REGEN3	CLK32KGAUDIO	CLK32KG	SYSEN2	SYSEN1	REGEN2	REGEN1

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	REGEN3	ES1.0: Reserved bit ES2.0->: REGEN3 implementation 0: NSLEEP has no effect on REGEN3 1: REGEN3 is controlled by NSLEEP	RW	0
5	CLK32KGAUDIO	0: NSLEEP has no effect on CLK32KGAUDIO 1: CLK32KGAUDIO is controlled by NSLEEP	RW	0

Bits	Field Name	Description	Type	Reset
4	CLK32KG	0: NSLEEP has no effect on CLK32KG 1: CLK32KG is controlled by NSLEEP	RW	0
3	SYSEN2	0: NSLEEP has no effect on SYSEN2 1: SYSEN2 is controlled by NSLEEP	RW	0
2	SYSEN1	0: NSLEEP has no effect on SYSEN1 1: SYSEN1 is controlled by NSLEEP	RW	0
1	REGEN2	0: NSLEEP has no effect on REGEN2 1: REGEN2 is controlled by NSLEEP	RW	0
0	REGEN1	0: NSLEEP has no effect on REGEN1 1: REGEN1 is controlled by NSLEEP	RW	0

1.9.2.8 NSLEEP_SMPS_ASSIGN Register

Table 1-132. NSLEEP_SMPS_ASSIGN

Address offset	0x07	**I2C Address**	0x48
Physical Address	0x1DB **Instance**	FUNC_RESOURCE	
Description	NSLEEP input signal SMPS resource assignment register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
SMPS10	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12

Bits	Field Name	Description	Type	Reset
7	SMPS10	0: NSLEEP has no effect on SMPS10 1: SMPS10 is controlled by NSLEEP	RW	0
6	SMPS9	0: NSLEEP has no effect on SMPS9 1: SMPS9 is controlled by NSLEEP	RW	0
5	SMPS8	0: NSLEEP has no effect on SMPS8 1: SMPS8 is controlled by NSLEEP	RW	0
4	SMPS7	0: NSLEEP has no effect on SMPS7 1: SMPS7 is controlled by NSLEEP	RW	0
3	SMPS6	0: NSLEEP has no effect on SMPS6 1: SMPS6 is controlled by NSLEEP	RW	0
2	SMPS45	0: NSLEEP has no effect on SMPS45 1: SMPS45 is controlled by NSLEEP	RW	0
1	SMPS3	0: NSLEEP has no effect on SMPS3 1: SMPS3 is controlled by NSLEEP	RW	0
0	SMPS12	0: NSLEEP has no effect on SMPS12 1: SMPS12 is controlled by NSLEEP	RW	0

1.9.2.9 NSLEEP_LDO_ASSIGN1 Register

Table 1-133. NSLEEP_LDO_ASSIGN1

Address offset	0x08			**I2C Address**	0x48
Physical Address	0x1DC	**Instance**		FUNC_RESOURCE	
Description	NSLEEP input signal LDO resource assignment register #1 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
LDO8	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1

Bits	Field Name	Description	Type	Reset
7	LDO8	0: NSLEEP has no effect on LDO8 1: LDO8 is controlled by NSLEEP	RW	0
6	LDO7	0: NSLEEP has no effect on LDO7 1: LDO7 is controlled by NSLEEP	RW	0
5	LDO6	0: NSLEEP has no effect on LDO6 1: LDO6 is controlled by NSLEEP	RW	0
4	LDO5	0: NSLEEP has no effect on LDO5 1: LDO5 is controlled by NSLEEP	RW	0
3	LDO4	0: NSLEEP has no effect on LDO4 1: LDO4 is controlled by NSLEEP	RW	0
2	LDO3	0: NSLEEP has no effect on LDO3 1: LDO3 is controlled by NSLEEP	RW	0
1	LDO2	0: NSLEEP has no effect on LDO2 1: LDO2 is controlled by NSLEEP	RW	0
0	LDO1	0: NSLEEP has no effect on LDO1 1: LDO1 is controlled by NSLEEP	RW	0

1.9.2.10 NSLEEP_LDO_ASSIGN2 Register

Table 1-134. NSLEEP_LDO_ASSIGN2

Address offset	0x09			**I2C Address**	0x48
Physical Address	0x1DD	**Instance**		FUNC_RESOURCE	
Description	NSLEEP input signal LDO resource assignment register #2 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved					LDOUSB	LDOLN	LDO9

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2	LDOUSB	0: NSLEEP has no effect on LDOUSB 1: LDOUSB is controlled by NSLEEP	RW	0
1	LDOLN	0: NSLEEP has no effect on LDOLN 1: LDOLN is controlled by NSLEEP	RW	0
0	LDO9	0: NSLEEP has no effect on LDO9 1: LDO9 is controlled by NSLEEP	RW	0

1.9.2.11 ENABLE1_RES_ASSIGN Register

Table 1-135. ENABLE1_RES_ASSIGN

Address offset	0x0A	**I2C Address**	0x48
Physical Address	0x1DE **Instance**	FUNC_RESOURCE	
Description	ENABLE1 resource assignment register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	REGEN3	CLK32KGAUDIO	CLK32KG	SYSEN2	SYSEN1	REGEN2	REGEN1

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	REGEN3	ES1.0: Reserved bit ES2.0->: REGEN3 implementation 0: ENABLE1 has no effect on REGEN3 1: REGEN3 is controlled by ENABLE1	RW	0
5	CLK32KGAUDIO	0: ENABLE1 has no effect on CLK32KGAUDIO 1: CLK32KGAUDIO is controlled by ENABLE1	RW	0
4	CLK32KG	0: ENABLE1 has no effect on CLK32KG 1: CLK32KG is controlled by ENABLE1	RW	0
3	SYSEN2	0: ENABLE1 has no effect on SYSEN2 1: SYSEN2 is controlled by ENABLE1	RW	0
2	SYSEN1	0: ENABLE1 has no effect on SYSEN1 1: SYSEN1 is controlled by ENABLE1	RW	0
1	REGEN2	0: ENABLE1 has no effect on REGEN2 1: REGEN2 is controlled by ENABLE1	RW	0
0	REGEN1	0: ENABLE1 has no effect on REGEN1 1: REGEN1 is controlled by ENABLE1	RW	0

1.9.2.12 ENABLE1_SMPS_ASSIGN Register

Table 1-136. ENABLE1_SMPS_ASSIGN

Address offset	0x0B	**I2C Address**	0x48
Physical Address	0x1DF **Instance**	FUNC_RESOURCE	
Description	ENABLE1 input signal SMPS resource assignment register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
SMPS10	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12

Bits	Field Name	Description	Type	Reset
7	SMPS10	0: ENABLE1 has no effect on SMPS10 1: SMPS10 is controlled by ENABLE1	RW	0
6	SMPS9	0: ENABLE1 has no effect on SMPS9 1: SMPS9 is controlled by ENABLE1	RW	0
5	SMPS8	0: ENABLE1 has no effect on SMPS8 1: SMPS8 is controlled by ENABLE1	RW	0
4	SMPS7	0: ENABLE1 has no effect on SMPS7 1: SMPS7 is controlled by ENABLE1	RW	0

Bits	Field Name	Description	Type	Reset
3	SMPS6	0: ENABLE1 has no effect on SMPS6 1: SMPS6 is controlled by ENABLE1	RW	0
2	SMPS45	0: ENABLE1 has no effect on SMPS45 1: SMPS45 is controlled by ENABLE1	RW	0
1	SMPS3	0: ENABLE1 has no effect on SMPS3 1: SMPS3 is controlled by ENABLE1	RW	0
0	SMPS12	0: ENABLE1 has no effect on SMPS12 1: SMPS12 is controlled by ENABLE1	RW	0

1.9.2.13 ENABLE1_LDO_ASSIGN1 Register

Table 1-137. ENABLE1_LDO_ASSIGN1

Address offset	0x0C		**I2C Address**	0x48	
Physical Address	0x1E0	**Instance**	FUNC_RESOURCE		
Description	ENABLE1 input signal LDO resource assignment register #1 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
LDO8	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1

Bits	Field Name	Description	Type	Reset
7	LDO8	0: ENABLE1 has no effect on LDO8 1: LDO8 is controlled by ENABLE1	RW	0
6	LDO7	0: ENABLE1 has no effect on LDO7 1: LDO7 is controlled by ENABLE1	RW	0
5	LDO6	0: ENABLE1 has no effect on LDO6 1: LDO6 is controlled by ENABLE1	RW	0
4	LDO5	0: ENABLE1 has no effect on LDO5 1: LDO5 is controlled by ENABLE1	RW	0
3	LDO4	0: ENABLE1 has no effect on LDO4 1: LDO4 is controlled by ENABLE1	RW	0
2	LDO3	0: ENABLE1 has no effect on LDO3 1: LDO3 is controlled by ENABLE1	RW	0
1	LDO2	0: ENABLE1 has no effect on LDO2 1: LDO2 is controlled by ENABLE1	RW	0
0	LDO1	0: ENABLE1 has no effect on LDO1 1: LDO1 is controlled by ENABLE1	RW	0

1.9.2.14 ENABLE1_LDO_ASSIGN2 Register

Table 1-138. ENABLE1_LDO_ASSIGN2

Address offset	0x0D		**I2C Address**	0x48	
Physical Address	0x1E1	**Instance**	FUNC_RESOURCE		
Description	ENABLE1 input signal LDO resource assignment register #2 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved					LDOUSB	LDOLN	LDO9

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2	LDOUSB	0: ENABLE1 has no effect on LDOUSB 1: LDOUSB is controlled by ENABLE1	RW	0
1	LDOLN	0: ENABLE1 has no effect on LDOLN 1: LDOLN is controlled by ENABLE1	RW	0
0	LDO9	0: ENABLE1 has no effect on LDO9 1: LDO9 is controlled by ENABLE1	RW	0

1.9.2.15 ENABLE2_RES_ASSIGN Register

Table 1-139. ENABLE2_RES_ASSIGN

Address offset	0x0E	**I2C Address**	0x48
Physical Address	0x1E2 **Instance**	FUNC_RESOURCE	
Description	ENABLE2 resource assignment register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	REGEN3	CLK32KGAUDIO	CLK32KG	SYSEN2	SYSEN1	REGEN2	REGEN1

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	REGEN3	ES1.0: Reserved bit ES2.0->: REGEN3 implementation 0: ENABLE2 has no effect on REGEN3 1: REGEN3 is controlled by ENABLE2	RW	0
5	CLK32KGAUDIO	0: ENABLE2 has no effect on CLK32KGAUDIO 1: CLK32KGAUDIO is controlled by ENABLE2	RW	0
4	CLK32KG	0: ENABLE2 has no effect on CLK32KG 1: CLK32KG is controlled by ENABLE2	RW	0
3	SYSEN2	0: ENABLE2 has no effect on SYSEN2 1: SYSEN2 is controlled by ENABLE2	RW	0
2	SYSEN1	0: ENABLE2 has no effect on SYSEN1 1: SYSEN1 is controlled by ENABLE2	RW	0
1	REGEN2	0: ENABLE2 has no effect on REGEN2 1: REGEN2 is controlled by ENABLE2	RW	0
0	REGEN1	0: ENABLE2 has no effect on REGEN1 1: REGEN1 is controlled by ENABLE2	RW	0

1.9.2.16 ENABLE2_SMPS_ASSIGN Register

Table 1-140. ENABLE2_SMPS_ASSIGN

Address offset	0x0F			**I2C Address**	0x48
Physical Address	0x1E3	**Instance**		FUNC_RESOURCE	
Description	ENABLE2 input signal SMPS resource assignment register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
SMPS10	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12

Bits	Field Name	Description	Type	Reset
7	SMPS10	0: ENABLE2 has no effect on SMPS10 1: SMPS10 is controlled by ENABLE2	RW	0
6	SMPS9	0: ENABLE2 has no effect on SMPS9 1: SMPS9 is controlled by ENABLE2	RW	0
5	SMPS8	0: ENABLE2 has no effect on SMPS8 1: SMPS8 is controlled by ENABLE2	RW	0
4	SMPS7	0: ENABLE2 has no effect on SMPS7 1: SMPS7 is controlled by ENABLE2	RW	0
3	SMPS6	0: ENABLE2 has no effect on SMPS6 1: SMPS6 is controlled by ENABLE2	RW	0
2	SMPS45	0: ENABLE2 has no effect on SMPS45 1: SMPS45 is controlled by ENABLE2	RW	0
1	SMPS3	0: ENABLE2 has no effect on SMPS3 1: SMPS3 is controlled by ENABLE2	RW	0
0	SMPS12	0: ENABLE2 has no effect on SMPS12 1: SMPS12 is controlled by ENABLE2	RW	0

1.9.2.17 ENABLE2_LDO_ASSIGN1 Register

Table 1-141. ENABLE2_LDO_ASSIGN1

Address offset	0x10			**I2C Address**	0x48
Physical Address	0x1E4	**Instance**		FUNC_RESOURCE	
Description	ENABLE2 input signal LDO resource assignment register #1 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
LDO8	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1

Bits	Field Name	Description	Type	Reset
7	LDO8	0: ENABLE2 has no effect on LDO8 1: LDO8 is controlled by ENABLE2	RW	0
6	LDO7	0: ENABLE2 has no effect on LDO7 1: LDO7 is controlled by ENABLE2	RW	0
5	LDO6	0: ENABLE2 has no effect on LDO6 1: LDO6 is controlled by ENABLE2	RW	0
4	LDO5	0: ENABLE2 has no effect on LDO5 1: LDO5 is controlled by ENABLE2	RW	0
3	LDO4	0: ENABLE2 has no effect on LDO4 1: LDO4 is controlled by ENABLE2	RW	0
2	LDO3	0: ENABLE2 has no effect on LDO3 1: LDO3 is controlled by ENABLE2	RW	0

Bits	Field Name	Description	Type	Reset
1	LDO2	0: ENABLE2 has no effect on LDO2 1: LDO2 is controlled by ENABLE2	RW	0
0	LDO1	0: ENABLE2 has no effect on LDO1 1: LDO1 is controlled by ENABLE2	RW	0

1.9.2.18 ENABLE2_LDO_ASSIGN2 Register

Table 1-142. ENABLE2_LDO_ASSIGN2

Address offset	0x11	**I2C Address**	0x48
Physical Address	0x1E5 **Instance**	FUNC_RESOURCE	
Description	ENABLE2 input signal LDO resource assignment register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					LDOUSB	LDOLN	LDO9

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2	LDOUSB	0: ENABLE2 has no effect on LDOUSB 1: LDOUSB is controlled by ENABLE2	RW	0
1	LDOLN	0: ENABLE2 has no effect on LDOLN 1: LDOLN is controlled by ENABLE2	RW	0
0	LDO9	0: ENABLE2 has no effect on LDO9 1: LDO9 is controlled by ENABLE2	RW	0

1.9.2.19 REGEN3_CTRL Register

Table 1-143. REGEN3_CTRL

Address offset	0x12	**I2C Address**	0x48
Physical Address	0x1E6 **Instance**	FUNC_RESOURCE	
Description	ES1.0: Reserved ES2.0->: REGEN3 control register RESET register domain: SWORST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			STATUS	Reserved	MODE_SLEEP	Reserved	MODE_ACTIVE

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	STATUS	REGEN3 Status 0: OFF 1: ON	RO	0
3	Reserved		RO	0
2	MODE_SLEEP	REGEN3 SLEEP Mode 0: OFF 1: ON	RW	0

Bits	Field Name	Description	Type	Reset
1	Reserved		RO	0
0	MODE_ACTIVE	REGEN3 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON	RW	X

1.10 FUNC_PAD_CONTROL Registers

1.10.1 FUNC_PAD_CONTROL Registers Mapping Summary

This section provides information on the FUNC_PAD_CONTROL Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.10.1.1 FUNC_PU_PD_OD Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
PU_PD_INPUT_CTRL1	RW	8	0b0X01 0X10	0x48	0x00	0x1F4
PU_PD_INPUT_CTRL2	RW	8	0x16	0x48	0x01	0x1F5
PU_PD_INPUT_CTRL3	RW	8	0x55	0x48	0x02	0x1F6
OD_OUTPUT_CTRL	RW	8	0x01	0x48	0x04	0x1F8
POLARITY_CTRL	RW	8	0x0X	0x48	0x05	0x1F9
PRIMARY_SECONDARY_PAD1	RW	8	0xXX	0x48	0x06	0x1FA
PRIMARY_SECONDARY_PAD2	RW	8	0b00XX XXXX	0x48	0x07	0x1FB
I2C_SPI	RW	8	0b00XX XXXX	0x48	0x08	0x1FC
PU_PD_INPUT_CTRL4	RW	8	0x55	0x48	0x09	0x1FD
PRIMARY_SECONDARY_PAD3	RW	8	0b0000 00XX	0x48	0x0A	0x1FE

1.10.2 FUNC_PAD_CONTROL Register Descriptions

1.10.2.1 PU_PD_INPUT_CTRL1 Register

Table 1-144. PU_PD_INPUT_CTRL1

Address offset	0x00			**I2C Address**	0x48
Physical Address	0x1F4	**Instance**		FUNC_PU_PD_OD	
Description	Pull-up Pull-down control register RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	RESET_IN_PD	GPADC_START_PU	GPADC_START_PD	Reserved	PWRDOWN_PD	NRESWARM_PU	Reserved

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	RESET_IN_PD	0: Pull-down not enabled 1: Pull-down enabled	RW	X
5	GPADC_START_PU	0: Pull-up not enabled (default) 1: Pull-up enabled	RW	0
4	GPADC_START_PD	0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
3	Reserved		RO	0
2	PWRDOWN_PD	0: Pull-down not enabled 1: Pull-down enabled	RW	X
1	NRESWARM_PU	0: Pull-up not enabled 1: Pull-up enabled (default)	RW	1
0	Reserved		RO	0

1.10.2.2 PU_PD_INPUT_CTRL2 Register

Table 1-145. PU_PD_INPUT_CTRL2

Address offset	0x01	**I2C Address**	0x48
Physical Address	0x1F5 **Instance**	FUNC_PU_PD_OD	
Description	Pull-up Pull-down control register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		ENABLE2_PU	ENABLE2_PD	ENABLE1_PU	ENABLE1_PD	NSLEEP_PU	NSLEEP_PD

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5	ENABLE2_PU	0: Pull-up not enabled (default) 1: Pull-up enabled	RW	0
4	ENABLE2_PD	0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
3	ENABLE1_PU	0: Pull-up not enabled (default) 1: Pull-up enabled	RW	0
2	ENABLE1_PD	0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
1	NSLEEP_PU	0: Pull-up not enabled 1: Pull-up enabled (default)	RW	1
0	NSLEEP_PD	0: Pull-down not enabled (default) 1: Pull-down enabled	RW	0

1.10.2.3 PU_PD_INPUT_CTRL3 Register

Table 1-146. PU_PD_INPUT_CTRL3

Address offset	0x02			**I2C Address**	0x48
Physical Address	0x1F6	**Instance**		FUNC_PU_PD_OD	
Description	Pull-up Pull-down control register RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	ACOK_PD	Reserved	CHRG_DET_N_PD	Reserved	POWERHOLD_PD	Reserved	MSECURE_PD

Bits	Field Name	Description	Type	Reset
7	Reserved	-	RO	0
6	ACOK_PD	Secondary function of VAC 0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
5	Reserved		RO	0
4	CHRG_DET_N_PD	Secondary function of GPIO_3 0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
3	Reserved		RO	0
2	POWERHOLD_PD	Secondary function of GPIO_7 0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
1	Reserved		RO	0
0	MSECURE_PD	Secondary function of GPIO_7 0: Pull-down not enabled 1: Pull-down enabled	RW	1

1.10.2.4 OD_OUTPUT_CTRL Register

Table 1-147. OD_OUTPUT_CTRL

Address offset	0x04			**I2C Address**	0x48
Physical Address	0x1F8	**Instance**		FUNC_PU_PD_OD	
Description	Open Drain control register RESET register domain: HWRST Note: It is user responsibility to take care about the IO direction and type (Open drain / Push-Pull) versus the pull-up/pull-down selections				
Type	RW				

7	6	5	4	3	2	1	0
PWM_2_OD	VBUSDET_OD	PWM_1_OD	Reserved	INT_OD	Reserved	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	PWM_2_OD	Secondary function of GPIO_2 (when LED_2 is selected as secondary function, OD is enabled by default) 0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)	RW	0

Bits	Field Name	Description	Type	Reset
6	VBUSDET_OD	Secondary function of GPIO_1 0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)	RW	0
5	PWM_1_OD	Secondary function of GPIO_1 (when LED_1 is selected as secondary function, OD is enabled by default) 0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)	RW	0
4	Reserved		RW	0
3	INT_OD	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)	RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	Reserved		RW	1

1.10.2.5 POLARITY_CTRL Register

Table 1-148. POLARITY_CTRL

Address offset	0x05	**I2C Address**	0x48
Physical Address	0x1F9 **Instance**	FUNC_PU_PD_OD	
Description	Polarity control register. This register allows to invert the initial polarity of the input or output pin. RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO polarity		
Type	RW		

7	6	5	4	3	2	1	0
INT_POLARITY	ENABLE2_POLARITY	ENABLE1_POLARITY	NSLEEP_POLARITY	RESET_IN_POLARITY	GPIO_3_CHRG_DET_N_POLARITY	POWERGOOD_USB_PSEL_POLARITY	PWRDOWN_POLARITY

Bits	Field Name	Description	Type	Reset
7	INT_POLARITY	Select the polarity of the INT output line 0: Interrupt line (INT) is low when interrupt is pending (default) 1: Interrupt line (INT) is high when interrupt is pending	RW	0
6	ENABLE2_POLARITY	Select the polarity of the ENABLE2 input line 0: Resources will be enable when ENABLE2 is high (default) 1: Resources will be enable when ENABLE2 is low	RW	0
5	ENABLE1_POLARITY	Select the polarity of the ENABLE1 input line 0: Resources will be enable when ENABLE1 is high (default) 1: Resources will be enable when ENABLE1 is low	RW	0
4	NSLEEP_POLARITY	Select the polarity of the NSLEEP input line 0: Resources will go in SLEEP mode when NSLEEP is low (default) 1: Resources will go in SLEEP mode when NSLEEP is high	RW	0
3	RESET_IN_POLARITY	Select the polarity of the RESET_IN input line 0: Device is switch-off when RESET_IN is low (default) 1: Device is switch-off when RESET_IN is high	RO	X

Bits	Field Name	Description	Type	Reset
2	GPIO_3_CHRG_DET_N_POLARITY	Select the polarity of the GPIO_3/CHRG_DET_N (USB charger detection) line This polarity change will apply to the primary and secondary function. 0: inversion not enable - active high for GPIO_3, active low for CHRG_DET_N (default) 1: inversion is enabled - active low for GPIO_3, active high for CHRG_DET_N	RO	X
1	POWERGOOD_USB_PSEL_POLARITY	Select the polarity of the POWERGOOD/USB_PSEL (charge can start) output line This polarity change will apply to the primary and secondary function. 0: inversion not enable - active high (default) 1: inversion is enabled - active low	RO	X
0	PWRDOWN_POLARITY	Select the polarity of the PWRDOWN input line 0: inversion not enable - active high (default) 1: inversion is enabled - active low	RO	X

1.10.2.6 PRIMARY_SECONDARY_PAD1 Register

Table 1-149. PRIMARY_SECONDARY_PAD1

Address offset	0x06		**I2C Address**	0x48	
Physical Address	0x1FA	**Instance**	FUNC_PU_PD_OD		
Description	PAD/PIN function register (Primary vs. Secondary) RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
GPIO_3	GPIO_2		GPIO_1		GPIO_0	VAC	POWERGOOD

Bits	Field Name	Description	Type	Reset
7	GPIO_3	Selection primary or secondary function associated to GPIO_3 pin/pad 0: Primary function is selected (GPIO_3) 1: Secondary function is selected (CHRG_DET_N)	RW	X
6:5	GPIO_2	Selection primary or secondary function associated to GPIO_2 pin/pad 00: Primary function is selected (GPIO_2) 01: (ES1.0) Secondary function is selected (GPIO_2) - Reserved 01: (ES2.0->) Secondary function is selected (REGEN3) 10: Secondary function is selected (LED_2) 11: Secondary function is selected (PWM_2)	RW	0bXX
4:3	GPIO_1	Selection primary or secondary function associated to GPIO_1 pin/pad 00: Primary function is selected (GPIO_1) 01: Secondary function is selected (VBUSDET) 10: Secondary function is selected (LED_1) 11: Secondary function is selected (PWM_1)	RW	0bXX
2	GPIO_0	Selection primary or secondary function associated to GPIO_0 pin/pad 0: Primary function is selected (GPIO_0) 1: Secondary function is selected (ID)	RW	X
1	VAC	Selection primary or secondary function associated to VAC pin/pad 0: Primary function is selected (VAC) 1: Secondary function is selected (ACOK)	RW	X
0	POWERGOOD	Selection primary or secondary function associated to POWERGOOD pin/pad 0: Primary function is selected (POWERGOOD) 1: Secondary function is selected (USB_PSEL)	RW	X

1.10.2.7 PRIMARY_SECONDARY_PAD2 Register

Table 1-150. PRIMARY_SECONDARY_PAD2

Address offset	0x07			**I2C Address**	0x48
Physical Address	0x1FB	**Instance**		FUNC_PU_PD_OD	
Description	PAD/PIN function register (Primary vs. Secondary) RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		GPIO_7		GPIO_6	GPIO_5		GPIO_4

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:4	GPIO_7	Selection primary or secondary function associated to GPIO_7 pin/pad 00: Primary function is selected (GPIO_7) 01: Secondary function is selected (MSECURE) - if OTP selected to this value (MSECURE), this register is locked to this value for ever. 10: Secondary function is selected (POWERHOLD) 11: Secondary function is selected - Reserved same functionality as 00 (GPIO_7)	RW	0bXX
3	GPIO_6	Selection primary or secondary function associated to GPIO_6 pin/pad 0: Primary function is selected (GPIO_6) 1: Secondary function is selected (SYSEN2)	RW	X
2:1	GPIO_5	Selection primary or secondary function associated to GPIO_5 pin/pad 00: Primary function is selected (GPIO_5) 01: Secondary function is selected (CLK32KGAUDIO) 10: Secondary function is selected (USB_PSEL) 11: Secondary function is selected ES1.0: GPIO_5 (Reserved) ES2.2->: REGEN2	RW	0bXX
0	GPIO_4	Selection primary or secondary function associated to GPIO_4 pin/pad 0: Primary function is selected (GPIO_4) 1: Secondary function is selected (SYSEN1)	RW	X

1.10.2.8 I2C_SPI Register

Table 1-151. I2C_SPI

Address offset	0x08			**I2C Address**	0x48
Physical Address	0x1FC	**Instance**		FUNC_PU_PD_OD	
Description	Validity memory RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
I2C2OTP_EN	I2C2OTP_PAGESEL	ID_I2C2	I2C_SPI	ID_I2C1			

Bits	Field Name	Description	Type	Reset
7	I2C2OTP_EN	I2C to OTP (I2C2OTP) feature selection (EVM purpose only) 0: I2C2OTP is disable 1: I2C2OTP is enabled	RW	0
6	I2C2OTP_PAGESEL	I2C to OTP (I2C2OTP) page selection (EVM purpose only) 0: page0 is selected (OTP-page0 (Test/Trim - reserved), OTP-page1 (Sequencer - LSB), OTP-page2 (Sequencer), OTP-page3 (Sequencer)) 1: page1 is selected (OTP-page4 (Sequencer - MSB), OTP-page5 (Config))	RW	0
5	ID_I2C2	I2C_2 address for page access versus initial address (0H12) 0: Address 0H12 1: ES1.0: Address 0H22 (Reserved - do not use) ES2.0->: Address 0H22	RW	X
4	I2C_SPI	Selection of the interface 0: I2C 1: SPI	RO	X
3:0	ID_I2C1	I2C_1 address for page accesses versus initial address (0H48, 0H49, 0H4A, 0H4B (OTP)) I2C_1[0]=0: 0H48 I2C_1[0]=1: 0H58 I2C_1[1]=0: 0H49 I2C_1[1]=1: 0H59 I2C_1[2]=0: 0H4A I2C_1[2]=1: 0H5A I2C_1[3]=0: 0H4B I2C_1[3]=1: 0H5B	RW	0xX

1.10.2.9 PU_PD_INPUT_CTRL4 Register

Table 1-152. PU_PD_INPUT_CTRL4

Address offset	0x09	**I2C Address**	0x48
Physical Address	0x1FD **Instance**	FUNC_PU_PD_OD	
Description	ES1.0: Reserved register ES2.0->: Pull-up Pull-down control register RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	DVFS2_DAT_PD	Reserved	DVFS2_CLK_PD	Reserved	DVFS1_DAT_PD	Reserved	DVFS1_CLK_PD

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	DVFS2_DAT_PD	Secondary function of GPIO_6 0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
5	Reserved		RO	0
4	DVFS2_CLK_PD	Secondary function of GPADC_START 0: Pull-down not enabled 1: Pull-down enabled	RW	1
3	Reserved		RO	0

Bits	Field Name	Description	Type	Reset
2	DVFS1_DAT_PD	Secondary function of I2C2_SDA_SDO 0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
1	Reserved		RO	0
0	DVFS1_CLK_PD	Secondary function of I2C2_SCL_SCE 0: Pull-down not enabled 1: Pull-down enabled	RW	1

1.10.2.10 PRIMARY_SECONDARY_PAD3 Register

Table 1-153. PRIMARY_SECONDARY_PAD3

Address offset	0x0A	**I2C Address**	0x48
Physical Address	0x1FE **Instance**	FUNC_PU_PD_OD	
Description	ES1.0: Reserved register ES2.0->: DVFS configuration register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						DVFS2	DVFS1

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1	DVFS2	Selection primary or secondary function associated to GPADC_START and SYSEN2 pin/pad for DVFS2 interface 0: Primary function is selected (GPADC_START on GPADC_START, GPIO_6 on GPIO_6) 1: Secondary function is selected DVFS2 (DVFS2_CLK on GPADC_START, DVFS2_DAT on GPIO_6)	RW	X
0	DVFS1	Selection primary or secondary function associated to I2C2_SCL_SCE, I2C2_SDA_SDO pin/pad for DVFS1 interface 0: Primary function is selected, I2C2 (I2C2_SCL_SCE on I2C2_SCL_SCE , I2C2_SDA_SDO on I2C2_SDA_SDO) 1: Secondary function is selected DVFS1 (DVFS1_CLK on I2C2_SCL_SCE, DVFS1_DAT on I2C2_SDA_SDO)	RW	X

1.11 FUNC_LED_PWM Registers

1.11.1 FUNC_LED_PWM Registers Mapping Summary

This section provides information on the FUNC_LED_PWM Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.11.1.1 FUNC_LED Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
LED_PERIOD_CTRL	RW	8	0x00	0x49	0x00	0x200
LED_CTRL	RW	8	0x00	0x49	0x01	0x201
PWM_CTRL1	RW	8	0x00	0x49	0x02	0x202
PWM_CTRL2	RW	8	0x00	0x49	0x03	0x203

1.11.2 FUNC_LED_PWM Register Descriptions

1.11.2.1 LED_PERIOD_CTRL Register

Table 1-154. LED_PERIOD_CTRL

Address offset	0x00			**I2C Address**	0x49
Physical Address	0x200	**Instance**		FUNC_LED	
Description	LED Period Control register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		LED_2_PERIOD			LED_1_PERIOD		

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:3	LED_2_PERIOD	Period of LED_2 signal (GPIO_2) 000: LED_2 OFF 001: 0.125s 010: 0.250s ... 110: 4s 111: 8s Note: Timing are specified +/- 2%	RW	0x0
2:0	LED_1_PERIOD	Period of LED_1 signal (GPIO_1) 000: LED_1 OFF 001: 0.125s 010: 0.250s ... 110: 4s 111: 8s Note: Timing are specified +/- 2%	RW	0x0

1.11.2.2 LED_CTRL Register

Table 1-155. LED_CTRL

Address offset	0x01			**I2C Address**	0x49
Physical Address	0x201	**Instance**		FUNC_LED	
Description	LED control register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved		LED_2_SEQ	LED_1_SEQ	LED_2_ON_TIME		LED_1_ON_TIME	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5	LED_2_SEQ	0: LED_2 will generate 1 pulse: ON (ON_TIME) - OFF (ON TIME)) 5default) 1: LED_2 will repeat 2 pulse sequences: ON (ON_TIME) - OFF (ON TIME) - ON (ON TIME) - OFF remainder of the period	RW	0
4	LED_1_SEQ	0: LED_1 will generate 1 pulse: ON (ON_TIME) - OFF (ON TIME)) (default) 1: LED_1 will repeat 2 pulse sequences: ON (ON_TIME) - OFF (ON TIME) - ON (ON TIME) - OFF remainder of the period	RW	0

Bits	Field Name	Description	Type	Reset
3:2	LED_2_ON_TIME	LED_1_ON_TIME selection 00: 62.5ms 01: 125ms 10: 250ms 11: 500ms	RW	0x0
1:0	LED_1_ON_TIME	LED_1_ON_TIME selection 00: 62.5ms 01: 125ms 10: 250ms 11: 500ms	RW	0x0

1.11.2.3 PWM_CTRL1 Register

Table 1-156. PWM_CTRL1

Address offset	0x02		**I2C Address**	0x49	
Physical Address	0x202	**Instance**	FUNC_LED		
Description	Pulse Width Modulation Control register 1 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved						PWM_FREQ_EN	PWM_FREQ_SEL

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1	PWM_FREQ_EN	PWM feature selection 0: Feature is not enabled - OFF (default) 1: Feature is enabled - ON	RW	0
0	PWM_FREQ_SEL	Frequency of PWM 0: 125 Hz (default) 1: 62.5 Hz	RW	0

1.11.2.4 PWM_CTRL2 Register

Table 1-157. PWM_CTRL2

Address offset	0x03		**I2C Address**	0x49	
Physical Address	0x203	**Instance**	FUNC_LED		
Description	Pulse Width Modulation Control register 2 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
PWM_DUTY_SEL							

Bits	Field Name	Description	Type	Reset
7:0	PWM_DUTY_SEL	Duty cycle of PWM 00000000: 0/256 (default) 00000001: 1/256 .. 11111110: 254/256 11111111: 255/256	RW	0x00

1.12 FUNC_INTERRUPT Registers

1.12.1 FUNC_INTERRUPT Registers Mapping Summary

This section provides information on the FUNC_INTERRUPT Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.12.1.1 FUNC_INTERRUPT Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
INT1_STATUS	RO	8	0x00	0x49	0x00	0x210
INT1_MASK	RW	8	0xXX	0x49	0x01	0x211
INT1_LINE_STATE	RO	8	0x00	0x49	0x02	0x212
INT1_EDGE_DETECT1_RESERVED	RO	8	0x00	0x49	0x03	0x213
INT1_EDGE_DETECT2_RESERVED	RO	8	0x00	0x49	0x04	0x214
INT2_STATUS	RO	8	0x00	0x49	0x05	0x215
INT2_MASK	RW	8	0xXX	0x49	0x06	0x216
INT2_LINE_STATE	RO	8	0x00	0x49	0x07	0x217
INT2_EDGE_DETECT1_RESERVED	RO	8	0x00	0x49	0x08	0x218
INT2_EDGE_DETECT2_RESERVED	RO	8	0x00	0x49	0x09	0x219
INT3_STATUS	RO	8	0x00	0x49	0x0A	0x21A
INT3_MASK	RW	8	0xXX	0x49	0x0B	0x21B
INT3_LINE_STATE	RO	8	0x00	0x49	0x0C	0x21C
INT3_EDGE_DETECT1_RESERVED	RO	8	0x00	0x49	0x0D	0x21D
INT3_EDGE_DETECT2_RESERVED	RO	8	0x00	0x49	0x0E	0x21E
INT4_STATUS	RO	8	0x00	0x49	0x0F	0x21F
INT4_MASK	RW	8	0xXX	0x49	0x10	0x220
INT4_LINE_STATE	RO	8	0x00	0x49	0x11	0x221
INT4_EDGE_DETECT1	RW	8	0xFF	0x49	0x12	0x222
INT4_EDGE_DETECT2	RW	8	0xFF	0x49	0x13	0x223
INT_CTRL	RW	8	0x00	0x49	0x14	0x224

1.12.2 FUNC_INTERRUPT Register Descriptions

1.12.2.1 INT1_STATUS Register

Table 1-158. INT1_STATUS

Address offset	0x00	**I2C Address**	0x49
Physical Address	0x210 **Instance**	FUNC_INTERRUPT	
Description	Interrupt Status Register #1 The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR) RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
VBAT_MON	VSYS_MON	HOTDIE	PWRDOWN	RPWRON	LONG_PRESS_KEY	PWRON	CHARG_DET_N_VBUS_OVV

Bits	Field Name	Description	Type	Reset
7	VBAT_MON	VBAT_MON status bit register (internal event) 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
6	VSYS_MON	VSYS_MON status bit register (internal event) 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
5	HOTDIE	HOTDIE status bit register (internal event) 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
4	PWRDOWN	PWRDOWN status bit register associated to PWRDOWN pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
3	RPWRON	RPWRON status bit register associated to RPWRON pin 0: no detection 1: Falling edge is detected	RO RtoClr	0
2	LONG_PRESS_KEY	LONG_PRESS_KEY (Long Key press duration) status bit register 0: no detection 1: Falling edge is detected	RO RtoClr	0
1	PWRON	PWRON status bit register associated to PWRON pin 0: no detection 1: Falling edge is detected	RO RtoClr	0
0	CHARG_DET_N_VBUS_OVV	CHARG_DET_N_VBUS_OVV status bit register 0: no detection 1: Rising or Falling edge are detected To know the interrupt source (CHARG_DET_N or VBUS_OVV), you must read the PMU_SECONDARY_INT. To know the current status of the CHARG_DET_N or VBUS_OVV, you must read the EXT_CHRG_CTRL.	RO RtoClr	0

1.12.2.2 INT1_MASK Register

Table 1-159. INT1_MASK

Address offset	0x01	**I2C Address**	0x49
Physical Address	0x211 **Instance**	FUNC_INTERRUPT	
Description	Interrupt Line Mask Register #1 RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
VBAT_MON	VSYS_MON	HOTDIE	PWRDOWN	RPWRON	LONG_PRESS_KEY	PWRON	CHARG_DET_N_VBUS_OVV

Bits	Field Name	Description	Type	Reset
7	VBAT_MON	VBAT_MON Line Mask bit register 0: VBAT_MON line is enabled. An interrupt is generated on INT line 1: VBAT_MON line is masked. No interrupt is generated on INT line	RW	X
6	VSYS_MON	VSYS_MON Line Mask bit register 0: VSYS_MON line is enabled. An interrupt is generated on INT line 1: VSYS_MON line is masked. No interrupt is generated on INT line	RW	X
5	HOTDIE	HOTDIE Line Mask bit register 0: HOTDIE line is enabled. An interrupt is generated on INT line 1: HOTDIE line is masked. No interrupt is generated on INT line	RW	X
4	PWRDOWN	PWRDOWN Line Mask bit register 0: PWRDOWN line is enabled. An interrupt is generated on INT line 1: PWRDOWN line is masked. No interrupt is generated on INT line	RW	X
3	RPWRON	RPWRON Line Mask bit register 0: RPWRON line is enabled. An interrupt is generated on INT line 1: RPWRON line is masked. No interrupt is generated on INT line	RW	X
2	LONG_PRESS_KEY	LONG_PRESS_KEY Line Mask bit register 0: LONG_PRESS_KEY line is enabled. An interrupt is generated on INT line 1: LONG_PRESS_KEY line is masked. No interrupt is generated on INT line	RW	X
1	PWRON	PWRON Line Mask bit register 0: PWRON line is enabled. An interrupt is generated on INT line 1: PWRON line is masked. No interrupt is generated on INT line	RW	X
0	CHARG_DET_N_VBUS_OVV	CHARG_DET_N_VBUS_OVV Line Mask bit register 0: CHARG_DET_N_VBUS_OVV line is enabled. An interrupt is generated on INT line 1: CHARG_DET_N_VBUS_OVV line is masked. No interrupt is generated on INT line	RW	X

1.12.2.3 INT1_LINE_STATE Register

Table 1-160. INT1_LINE_STATE

Address offset	0x02	**I2C Address**	0x49
Physical Address	0x212 **Instance**	FUNC_INTERRUPT	
Description	Interrupt source line state Register #1 RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
VBAT_MON	VSYS_MON	HOTDIE	PWRDOWN	RPWRON	LONG_PRESS_KEY	PWRON	CHARG_DET_N_VBUS_OVV

Bits	Field Name	Description	Type	Reset
7	VBAT_MON	VBAT_MON line state register 0: VBAT_MON line is equal to 0 1: VBAT_MON line is equal to 1	RO	0
6	VSYS_MON	VSYS_MON line state register 0: VSYS_MON line is equal to 0 1: VSYS_MON line is equal to 1	RO	0
5	HOTDIE	HOTDIE line state register 0: HOTDIE line is equal to 0 1: HOTDIE line is equal to 1	RO	0
4	PWRDOWN	PWRDOWN line state register 0: PWRDOWN line is equal to 0 1: PWRDOWN line is equal to 1	RO	0
3	RPWRON	RPWRON line state register 0: RPWRON line is equal to 0 1: RPWRON line is equal to 1	RO	0
2	LONG_PRESS_KEY	LONG_PRESS_KEY line state register 0: LONG_PRESS_KEY line is equal to 0 1: LONG_PRESS_KEY line is equal to 1	RO	0
1	PWRON	PWRON line state register 0: PWRON line is equal to 0 1: PWRON line is equal to 1	RO	0
0	CHARG_DET_N_VBUS_OVV	CHARG_DET_N_VBUS_OVV line state register 0: CHARG_DET_N_VBUS_OVV line is equal to 0 1: CHARG_DET_N_VBUS_OVV line is equal to 1	RO	0

1.12.2.4 INT1_EDGE_DETECT1_RESERVED Register

Table 1-161. INT1_EDGE_DETECT1_RESERVED

Address offset	0x03			**I2C Address**	0x49
Physical Address	0x213	**Instance**		FUNC_INTERRUPT	
Description	Interrupt Edge Detection Register #1.1 (Reserved) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RO	0x00

1.12.2.5 INT1_EDGE_DETECT2_RESERVED Register

Table 1-162. INT1_EDGE_DETECT2_RESERVED

Address offset	0x04			**I2C Address**	0x49
Physical Address	0x214	**Instance**		FUNC_INTERRUPT	
Description	Interrupt Edge Detection Register #1.2 (Reserved) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RO	0x00

1.12.2.6 INT2_STATUS Register

Table 1-163. INT2_STATUS

Address offset	0x05			**I2C Address**	0x49
Physical Address	0x215	**Instance**		FUNC_INTERRUPT	
Description	Interrupt Status Register #2 The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
VAC_ACOK	SHORT	FBI_BB	RESET_IN	BATREMOVAL	WDT	RTC_TIMER	RTC_ALARM

Bits	Field Name	Description	Type	Reset
7	VAC_ACOK	VAC_ACOK status bit register associated to VAC pin 0: no detection 1: Rising or falling edge are detected	RO RtoClr	0
6	SHORT	SHORT status bit register associated (internal event). This bit is providing information on SHORT status (LDO and SMPS) and THERMAL status (SMPS only). Hence, normal behavior when you get a SHORT/over TEMPERATURE is: - An interrupt is generated - Interrupt routine will read interrupt status then SHORT /THERMAL status to know which resource is the source, which will clear the status (SHORT /THERMAL status register is cleared upon read) - Status is then cleared before the resource is re-enabled. 0: no detection 1: Rising or falling edge are detected	RO RtoClr	0
5	FBI_BB	First Battery Insertion (FBI) / Battery Bounce (BB) status bit register (internal event). If DVFS is enabled, interrupt source can be also from DVFS1_INT_SRC or DVFS2_INT_SRC. 0: no detection 1: Rising edge is detected To know the interrupt source (FBI First battery Insertion or BB battery bounce), you must read the PMU_SECONDARY_INT. If DVFS is enabled, interrupt source can be also from DVFS1 or DVFS2 and PMU_SECONDARY_INT2 register must be read to check interrupt source.	RO RtoClr	0
4	RESET_IN	RESET_IN status bit register associated to RESET_IN pin 0: no detection 1: Rising edge is detected	RO RtoClr	0
3	BATREMOVAL	BATREMOVAL status bit register (BATREMOVAL pin) 0: no detection 1: Rising or Falling edge are detected Note: In QFN configuration, this BATREMOVAL pin is not bounded. This register bit is still visible and functional but no hardware information will be send to BATREMOVAL pin.	RO RtoClr	0
2	WDT	WDT status bit register (internal event) 0: no detection 1: Rising edge is detected	RO RtoClr	0
1	RTC_TIMER	RTC_TIMER status bit register (internal event) 0: no detection 1: Rising edge is detected	RO RtoClr	0
0	RTC_ALARM	RTC_ALARM status bit register (internal event) 0: no detection 1: Rising edge is detected	RO RtoClr	0

1.12.2.7 INT2_MASK Register

Table 1-164. INT2_MASK

Address offset	0x06	**I2C Address**	0x49
Physical Address	0x216 **Instance**	FUNC_INTERRUPT	
Description	Interrupt Line Mask Register #2 RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
VAC_ACOK	SHORT	FBI_BB	RESET_IN	BATREMOVAL	WDT	RTC_TIMER	RTC_ALARM

Bits	Field Name	Description	Type	Reset
7	VAC_ACOK	VAC_ACOK line Mask bit register 0: VAC_ACOK line is enabled. An interrupt is generated on INT line 1: VAC_ACOK line is masked. No interrupt is generated on INT line	RW	X
6	SHORT	SHORT Line Mask bit register 0: SHORT line is enabled. An interrupt is generated on INT line 1: SHORT line is masked. No interrupt is generated on INT line	RW	X
5	FBI_BB	First Battery Insertion (FBI) / Battery Bounce (BB) Line Mask bit register 0: FBI_BB line is enabled. An interrupt is generated on INT line 1: FBI_BB line is masked. No interrupt is generated on INT line	RW	X
4	RESET_IN	RESET_IN Line Mask bit register 0: RESET_IN line is enabled. An interrupt is generated on INT line 1: RESET_IN line is masked. No interrupt is generated on INT line	RW	X
3	BATREMOVAL	BATREMOVAL Line Mask bit register 0: BATREMOVAL line is enabled. An interrupt is generated on INT line 1: BATREMOVAL line is masked. No interrupt is generated on INT line Note: In QFN configuration, this BATREMOVAL pin is not bounded. This register bit is still visible and functional but no hardware information will be send to BATREMOVAL pin.	RW	X
2	WDT	WDT (Watchdog) Line Mask bit register 0: WDT (Watchdog) line is enabled. An interrupt is generated on INT line 1: WDT (Watchdog) line is masked. No interrupt is generated on INT line	RW	X
1	RTC_TIMER	RTC_TIMER Line Mask bit register 0: RTC_TIMER line is enabled. An interrupt is generated on INT line 1: RTC_TIMER line is masked. No interrupt is generated on INT line	RW	X
0	RTC_ALARM	RTC_ALARM Line Mask bit register 0: RTC_ALARM line is enabled. An interrupt is generated on INT line 1: RTC_ALARM line is masked. No interrupt is generated on INT line	RW	X

1.12.2.8 INT2_LINE_STATE Register

Table 1-165. INT2_LINE_STATE

Address offset	0x07	**I2C Address**	0x49
Physical Address	0x217 **Instance**	FUNC_INTERRUPT	
Description	Interrupt source line state Register #2 RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
VAC_ACOK	SHORT	FBI_BB	RESET_IN	BATREMOVAL	WDT	RTC_TIMER	RTC_ALARM

Bits	Field Name	Description	Type	Reset
7	VAC_ACOK	VAC_ACOK line state register 0: VAC_ACOK line is equal to 0 1: VAC_ACOK line is equal to 1	RO	0
6	SHORT	SHORT line state register 0: SHORT line is equal to 0 1: SHORT line is equal to 1	RO	0
5	FBI_BB	First Battery Insertion (FBI) / Battery Bounce (BB) line state register 0: FBI_BB line is equal to 0 1: FBI_BB line is equal to 1	RO	0

Bits	Field Name	Description	Type	Reset
4	RESET_IN	RESET_IN line state register 0: RESET_IN line is equal to 0 1: RESET_IN line is equal to 1	RO	0
3	BATREMOVAL	BATREMOVAL line state register 0: BATREMOVAL line is equal to 0 1: BATREMOVAL line is equal to 1 Note: In QFN configuration, this BATREMOVAL pin is not bounded. This register bit is still visible and functional but no hardware information will be send to BATREMOVAL pin.	RO	0
2	WDT	WDT line state register 0: WDT line is equal to 0 1: WDT line is equal to 1	RO	0
1	RTC_TIMER	RTC_TIMER line state register 0: RTC_TIMER line is equal to 0 1: RTC_TIMER line is equal to 1	RO	0
0	RTC_ALARM	RTC_ALARM line state register 0: RTC_ALARM line is equal to 0 1: RTC_ALARM line is equal to 1	RO	0

1.12.2.9 INT2_EDGE_DETECT1_RESERVED Register

Table 1-166. INT2_EDGE_DETECT1_RESERVED

Address offset	0x08		**I2C Address**	0x49	
Physical Address	0x218	**Instance**	FUNC_INTERRUPT		
Description	Interrupt Edge Detection Register #2.1 (Reserved) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RO	0x00

1.12.2.10 INT2_EDGE_DETECT2_RESERVED Register

Table 1-167. INT2_EDGE_DETECT2_RESERVED

Address offset	0x09		**I2C Address**	0x49	
Physical Address	0x219	**Instance**	FUNC_INTERRUPT		
Description	Interrupt Edge Detection Register #2.2 (Reserved) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RO	0x00

1.12.2.11 INT3_STATUS Register

Table 1-168. INT3_STATUS

Address offset	0x0A	**I2C Address**	0x49
Physical Address	0x21A **Instance**	FUNC_INTERRUPT	
Description	Interrupt Status Register #3 The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR) RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
VBUS	VBUS_OTG	ID	ID_OTG	GPADC_EOC_RT	GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0

Bits	Field Name	Description	Type	Reset
7	VBUS	VBUS status bit register (VBUS pin) 0: no detection 1: Rising or falling edge are detected	RO RtoClr	0
6	VBUS_OTG	VBUS_OTG status bit register (Internal event) 0: no detection 1: Rising or falling edge are detected	RO RtoClr	0
5	ID	ID status bit register (ID pin - secondary function) 0: no detection 1: Rising or falling edge are detected	RO RtoClr	0
4	ID_OTG	ID_OTG status bit register (Internal event) 0: no detection 1: Rising or falling edge are detected	RO RtoClr	0
3	GPADC_EOC_RT	GPADC_EOC_RT status bit register (Internal event) 0: no detection 1: Rising or falling edge are detected	RO RtoClr	0
2	GPADC_EOC_SW	GPADC_EOC_SW status bit register associated (internal event) 0: no detection 1: Rising or falling edge are detected	RO RtoClr	0
1	GPADC_AUTO_1	GPADC_AUTO_1 status bit register (internal event) 0: no detection 1: Rising edge is detected	RO RtoClr	0
0	GPADC_AUTO_0	GPADC_AUTO_0 status bit register (Internal event) 0: no detection 1: Rising edge is detected	RO RtoClr	0

1.12.2.12 INT3_MASK Register

Table 1-169. INT3_MASK

Address offset	0x0B	**I2C Address**	0x49
Physical Address	0x21B **Instance**	FUNC_INTERRUPT	
Description	Interrupt Line Mask Register #3 RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
VBUS	VBUS_OTG	ID	ID_OTG	GPADC_EOC_RT	GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0

Bits	Field Name	Description	Type	Reset
7	VBUS	VBUS Line Mask bit register (VBUS pin) 0: VBUS line is enabled. An interrupt is generated on INT line 1: VBUS line is masked. No interrupt is generated on INT line	RW	X
6	VBUS_OTG	VBUS_OTG Line Mask bit register (Internal event) 0: VBUS_OTG line is enabled. An interrupt is generated on INT line 1: VBUS_OTG line is masked. No interrupt is generated on INT line	RW	X
5	ID	ID Line Mask bit register (ID pin) 0: ID line is enabled. An interrupt is generated on INT line 1: ID line is masked. No interrupt is generated on INT line	RW	X
4	ID_OTG	ID_OTG Line Mask bit register (Internal event) 0: ID_OTG line is enabled. An interrupt is generated on INT line 1: ID_OTG line is masked. No interrupt is generated on INT line	RW	X
3	GPADC_EOC_RT	GPADC_EOC_RT Line Mask bit register (Internal event) 0: GPADC_EOC_RT line is enabled. An interrupt is generated on INT line 1: GPADC_EOC_RT line is masked. No interrupt is generated on INT line	RW	X
2	GPADC_EOC_SW	GPADC_EOC_SW Line Mask bit register (Internal event) 0: GPADC_EOC_SW line is enabled. An interrupt is generated on INT line 1: GPADC_EOC_SW line is masked. No interrupt is generated on INT line	RW	X
1	GPADC_AUTO_1	GPADC_AUTO_1 Line Mask bit register (Internal event) 0: GPADC_AUTO_1 line is enabled. An interrupt is generated on INT line 1: GPADC_AUTO_1 line is masked. No interrupt is generated on INT line	RW	X
0	GPADC_AUTO_0	GPADC_AUTO_0 Line Mask bit register (Internal event) 0: GPADC_AUTO_0 line is enabled. An interrupt is generated on INT line 1: GPADC_AUTO_0 line is masked. No interrupt is generated on INT line	RW	X

1.12.2.13 INT3_LINE_STATE Register

Table 1-170. INT3_LINE_STATE

Address offset	0x0C	**I2C Address**	0x49
Physical Address	0x21C **Instance**	FUNC_INTERRUPT	
Description	Interrupt source line state Register #3 RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
VBUS	VBUS_OTG	ID	ID_OTG	GPADC_EOC_RT	GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0

Bits	Field Name	Description	Type	Reset
7	VBUS	VBUS line state register (VBUS pin) 0: VBUS line is equal to 0 1: VBUS line is equal to 1	RO	0
6	VBUS_OTG	VBUS_OTG line state register (Internal event) 0: VBUS_OTG line is equal to 0 1: VBUS_OTG line is equal to 1	RO	0
5	ID	ID line state register (ID pin) 0: ID line is equal to 0 1: ID line is equal to 1	RO	0
4	ID_OTG	ID_OTG line state register (Internal event) 0: ID_OTG line is equal to 0 1: ID_OTG line is equal to 1	RO	0
3	GPADC_EOC_RT	GPADC_EOC_RT line state register (Internal event) 0: GPADC_EOC_RT line is equal to 0 1: GPADC_EOC_RT line is equal to 1	RO	0
2	GPADC_EOC_SW	GPADC_EOC_SW line state register (Internal event) 0: GPADC_EOC_SW line is equal to 0 1: GPADC_EOC_SW line is equal to 1	RO	0
1	GPADC_AUTO_1	GPADC_AUTO_1 line state register (internal event) 0: GPADC_AUTO_1 line is equal to 0 1: GPADC_AUTO_1 line is equal to 1	RO	0
0	GPADC_AUTO_0	GPADC_AUTO_0 line state register (Internal event) 0: GPADC_AUTO_0 line is equal to 0 1: GPADC_AUTO_0 line is equal to 1	RO	0

1.12.2.14 INT3_EDGE_DETECT1_RESERVED Register

Table 1-171. INT3_EDGE_DETECT1_RESERVED

Address offset	0x0D	**I2C Address**	0x49
Physical Address	0x21D **Instance**	FUNC_INTERRUPT	
Description	Interrupt Edge Detection Register #3.1 (Reserved) RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RO	0x00

1.12.2.15 INT3_EDGE_DETECT2_RESERVED Register

Table 1-172. INT3_EDGE_DETECT2_RESERVED

Address offset	0x0E	**I2C Address**	0x49
Physical Address	0x21E **Instance**	FUNC_INTERRUPT	
Description	Interrupt Edge Detection Register #3.2 (Reserved) RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RO	0x00

1.12.2.16 INT4_STATUS Register

Table 1-173. INT4_STATUS

Address offset	0x0F	**I2C Address**	0x49
Physical Address	0x21F **Instance**	FUNC_INTERRUPT	
Description	Interrupt Status Register #4 The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR) RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0

Bits	Field Name	Description	Type	Reset
7	GPIO_7	GPIO_7 status bit register associated to GPIO_7 pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
6	GPIO_6	GPIO_6 status bit register associated to GPIO_6 pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
5	GPIO_5	GPIO_5 status bit register associated to GPIO_5 pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
4	GPIO_4	GPIO_4 status bit register associated to GPIO_4 pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
3	GPIO_3	GPIO_3 status bit register associated to GPIO_3 pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
2	GPIO_2	GPIO_2 status bit register associated to GPIO_2 pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
1	GPIO_1	GPIO_1 status bit register associated to GPIO_1 pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0
0	GPIO_0	GPIO_0 status bit register associated to GPIO_0 pin 0: no detection 1: Rising or Falling edge are detected	RO RtoClr	0

1.12.2.17 INT4_MASK Register

Table 1-174. INT4_MASK

Address offset	0x10	**I2C Address**	0x49
Physical Address	0x220 **Instance**	FUNC_INTERRUPT	
Description	Interrupt Line Mask Register #4 RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0

Bits	Field Name	Description	Type	Reset
7	GPIO_7	GPIO_7 Line Mask bit register 0: GPIO_7 line is enabled. An interrupt is generated on INT line 1: GPIO_7 line is masked. No interrupt is generated on INT line	RW	X
6	GPIO_6	GPIO_6 Line Mask bit register 0: GPIO_6 line is enabled. An interrupt is generated on INT line 1: GPIO_6 line is masked. No interrupt is generated on INT line	RW	X
5	GPIO_5	GPIO_5 Line Mask bit register 0: GPIO_5 line is enabled. An interrupt is generated on INT line 1: GPIO_5 line is masked. No interrupt is generated on INT line	RW	X
4	GPIO_4	GPIO_4 Line Mask bit register 0: GPIO_4 line is enabled. An interrupt is generated on INT line 1: GPIO_4 line is masked. No interrupt is generated on INT line	RW	X
3	GPIO_3	GPIO_3 Line Mask bit register 0: GPIO_3 line is enabled. An interrupt is generated on INT line 1: GPIO_3 line is masked. No interrupt is generated on INT line	RW	X
2	GPIO_2	GPIO_2 Line Mask bit register 0: GPIO_2 line is enabled. An interrupt is generated on INT line 1: GPIO_2 line is masked. No interrupt is generated on INT line	RW	X
1	GPIO_1	GPIO_1 Line Mask bit register 0: GPIO_1 line is enabled. An interrupt is generated on INT line 1: GPIO_1 line is masked. No interrupt is generated on INT line	RW	X
0	GPIO_0	GPIO_0 Line Mask bit register 0: GPIO_0 line is enabled. An interrupt is generated on INT line 1: GPIO_0 line is masked. No interrupt is generated on INT line	RW	X

1.12.2.18 INT4_LINE_STATE Register

Table 1-175. INT4_LINE_STATE

Address offset	0x11	**I2C Address**	0x49
Physical Address	0x221 **Instance**	FUNC_INTERRUPT	
Description	Interrupt source line state Register #4 RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0

Bits	Field Name	Description	Type	Reset
7	GPIO_7	GPIO_7 line state register 0: GPIO_7 line is equal to 0 1: GPIO_7 line is equal to 1	RO	0
6	GPIO_6	GPIO_6 line state register 0: GPIO_6 line is equal to 0 1: GPIO_6 line is equal to 1	RO	0

Bits	Field Name	Description	Type	Reset
5	GPIO_5	GPIO_5 line state register 0: GPIO_5 line is equal to 0 1: GPIO_5 line is equal to 1	RO	0
4	GPIO_4	GPIO_4 line state register 0: GPIO_4 line is equal to 0 1: GPIO_4 line is equal to 1	RO	0
3	GPIO_3	GPIO_3 line state register 0: GPIO_3 line is equal to 0 1: GPIO_3 line is equal to 1	RO	0
2	GPIO_2	GPIO_2 line state register 0: GPIO_2 line is equal to 0 1: GPIO_2 line is equal to 1	RO	0
1	GPIO_1	GPIO_1 line state register 0: GPIO_1 line is equal to 0 1: GPIO_1 line is equal to 1	RO	0
0	GPIO_0	GPIO_0 line state register 0: GPIO_0 line is equal to 0 1: GPIO_0 line is equal to 1	RO	0

1.12.2.19 INT4_EDGE_DETECT1 Register

Table 1-176. INT4_EDGE_DETECT1

Address offset	0x12	**I2C Address**	0x49
Physical Address	0x222 **Instance**	FUNC_INTERRUPT	
Description	Interrupt Edge Detection Register #4.1 RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_3_RISING	GPIO_3_FALLING	GPIO_2_RISING	GPIO_2_FALLING	GPIO_1_RISING	GPIO_1_FALLING	GPIO_0_RISING	GPIO_0_FALLING

Bits	Field Name	Description	Type	Reset
7	GPIO_3_RISING	0: Rising edge detection not enabled 1: Rising edge detection enable (default)	RW	1
6	GPIO_3_FALLING	0: Falling edge detection not enabled 1: Falling edge detection enable (default)	RW	1
5	GPIO_2_RISING	0: Rising edge detection not enabled 1: Rising edge detection enable (default)	RW	1
4	GPIO_2_FALLING	0: Falling edge detection not enabled 1: Falling edge detection enable (default)	RW	1
3	GPIO_1_RISING	0: Rising edge detection not enabled 1: Rising edge detection enable (default)	RW	1
2	GPIO_1_FALLING	0: Falling edge detection not enabled 1: Falling edge detection enable (default)	RW	1
1	GPIO_0_RISING	0: Rising edge detection not enabled 1: Rising edge detection enable (default)	RW	1
0	GPIO_0_FALLING	0: Falling edge detection not enabled 1: Falling edge detection enable (default)	RW	1

1.12.2.20 INT4_EDGE_DETECT2 Register

Table 1-177. INT4_EDGE_DETECT2

Address offset	0x13	**I2C Address**	0x49
Physical Address	0x223 **Instance**	FUNC_INTERRUPT	
Description	Interrupt Edge Detection Register #4.2 RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_7_RISING	GPIO_7_FALLING	GPIO_6_RISING	GPIO_6_FALLING	GPIO_5_RISING	GPIO_5_FALLING	GPIO_4_RISING	GPIO_4_FALLING

Bits	Field Name	Description	Type	Reset
7	GPIO_7_RISING	0: Rising edge detection not enabled 1: Rising edge detection enable (default)	RW	1
6	GPIO_7_FALLING	0: Falling edge detection not enabled 1: Falling edge detection enable (default)	RW	1
5	GPIO_6_RISING	0: Rising edge detection not enabled 1: Rising edge detection enable (default)	RW	1
4	GPIO_6_FALLING	0: Falling edge detection not enabled 1: Falling edge detection enable (default)	RW	1
3	GPIO_5_RISING	0: Rising edge detection not enabled 1: Rising edge detection enable (default)	RW	1
2	GPIO_5_FALLING	0: Falling edge detection not enabled 1: Falling edge detection enable (default)	RW	1
1	GPIO_4_RISING	0: Rising edge detection not enabled 1: Rising edge detection enable (default)	RW	1
0	GPIO_4_FALLING	0: Falling edge detection not enabled 1: Falling edge detection enable (default)	RW	1

1.12.2.21 INT_CTRL Register

Table 1-178. INT_CTRL

Address offset	0x14	**I2C Address**	0x49
Physical Address	0x224 **Instance**	FUNC_INTERRUPT	
Description	Interrupt control register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					INT_PENDING	Reserved	INT_CLEAR

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2	INT_PENDING	Pending interrupt latching feature selection (interrupt latched in case of new event before clearing on same line) 0: Enabled (default) 1: Not enabled	RW	0
1	Reserved		RO	0

Bits	Field Name	Description	Type	Reset
0	INT_CLEAR	Select the way to clear the interrupt bits (will be apply to ALL the bits) 0: Clear-on-Write - Interrupts cleared by writing 1. This method is bit based (default) 1: Clear-on-Read - Interrupts cleared on read	RW	0

1.13 FUNC_ID Registers

1.13.1 FUNC_ID Registers Mapping Summary

This section provides information on the FUNC_ID Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.13.1.1 FUNC_ID Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
VENDOR_ID_LSB	RO	8	0x51	0x49	0x00	0x24F
VENDOR_ID_MSB	RO	8	0x04	0x49	0x01	0x250
PRODUCT_ID_LSB	RO	8	0x35	0x49	0x02	0x251
PRODUCT_ID_MSB	RO	8	0xC0	0x49	0x03	0x252

1.13.2 FUNC_ID Register Descriptions

1.13.2.1 VENDOR_ID_LSB Register

Table 1-179. VENDOR_ID_LSB

Address offset	0x00	**I2C Address**	0x49
Physical Address	0x24F **Instance**	FUNC_ID	
Description	Vendor ID Register (LSB) RESET register domain: HWRST		
Type	RO		

7	6	5	4	3	2	1	0
VENDOR_ID							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID	Texas Instruments USB Vendor ID (8 LSBs) - Default value: 0x51	RO	0x51

1.13.2.2 VENDOR_ID_MSB Register

Table 1-180. VENDOR_ID_MSB

Address offset	0x01			**I2C Address**	0x49
Physical Address	0x250	**Instance**		FUNC_ID	
Description	Vendor ID Register (MSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
VENDOR_ID							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID	Texas Instruments USB Vendor ID (8 MSBs) - Default value: 0x04	RO	0x04

1.13.2.3 PRODUCT_ID_LSB Register

Table 1-181. PRODUCT_ID_LSB

Address offset	0x02			**I2C Address**	0x49
Physical Address	0x251	**Instance**		FUNC_ID	
Description	Product ID Register (LSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
PRODUCT_ID							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID	Texas Instruments Product ID (8 LSBs) - Default value: 0x35	RO	0x35

1.13.2.4 PRODUCT_ID_MSB Register

Table 1-182. PRODUCT_ID_MSB

Address offset	0x03			**I2C Address**	0x49
Physical Address	0x252	**Instance**		FUNC_ID	
Description	Product ID Register (MSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
PRODUCT_ID							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID	Texas Instruments Product ID (8 MSBs) - Default value: 0xC0	RO	0xC0

1.14 FUNC_USB_OTG Registers

1.14.1 FUNC_USB_OTG Registers Mapping Summary

This section provides information on the FUNC_USB_OTG Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.14.1.1 FUNC_USB_OTG Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
USB_WAKEUP	RW	8	0x00	0x49	0x00	0x253
USB_VBUS_CTRL_SET	RW	8	0x00	0x49	0x01	0x254
USB_VBUS_CTRL_CLR	RW	8	0x00	0x49	0x02	0x255
USB_ID_CTRL_SET	RW	8	0x00	0x49	0x03	0x256
USB_ID_CTRL_CLEAR	RW	8	0x00	0x49	0x04	0x257
USB_VBUS_INT_SRC	RO	8	0x01	0x49	0x05	0x258
USB_VBUS_INT_LATCH_SET	RW	8	0x00	0x49	0x06	0x259
USB_VBUS_INT_LATCH_CLR	RW	8	0x00	0x49	0x07	0x25A
USB_VBUS_INT_EN_LO_SET	RW	8	0x00	0x49	0x08	0x25B
USB_VBUS_INT_EN_LO_CLR	RW	8	0x00	0x49	0x09	0x25C
USB_VBUS_INT_EN_HI_SET	RW	8	0x00	0x49	0x0A	0x25D
USB_VBUS_INT_EN_HI_CLR	RW	8	0x00	0x49	0x0B	0x25E
USB_ID_INT_SRC	RO	8	0x00	0x49	0x0C	0x25F
USB_ID_INT_LATCH_SET	RW	8	0x00	0x49	0x0D	0x260
USB_ID_INT_LATCH_CLR	RW	8	0x00	0x49	0x0E	0x261
USB_ID_INT_EN_LO_SET	RW	8	0x00	0x49	0x0F	0x262
USB_ID_INT_EN_LO_CLR	RW	8	0x00	0x49	0x10	0x263
USB_ID_INT_EN_HI_SET	RW	8	0x00	0x49	0x11	0x264
USB_ID_INT_EN_HI_CLR	RW	8	0x00	0x49	0x12	0x265
USB_OTG_ADP_CTRL	RW	8	0x00	0x49	0x13	0x266
USB_OTG_ADP_HIGH	RW	8	0x00	0x49	0x14	0x267
USB_OTG_ADP_LOW	RW	8	0x00	0x49	0x15	0x268
USB_OTG_ADP_RISE	RO	8	0x00	0x49	0x16	0x269
USB_OTG_REVISION	RO	8	0b0000 000X	0x49	0x17	0x26A

1.14.2 FUNC_USB_OTG Register Descriptions

1.14.2.1 USB_WAKEUP Register

Table 1-183. USB_WAKEUP

Address offset	0x00			**I2C Address**	0x49
Physical Address	0x253	**Instance**		FUNC_USB_OTG	
Description	USB Wake Up register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved							ID_WK_UP_COMP

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RO	0x00
0	ID_WK_UP_COMP	0: Wake-up comparator disabled 1: Wake-up comparator enabled	RW	0

1.14.2.2 USB_VBUS_CTRL_SET Register

Table 1-184. USB_VBUS_CTRL_SET

Address offset	0x01	**I2C Address**	0x49
Physical Address	0x254 **Instance**	FUNC_USB_OTG	
Description	USB VBUS Control Set register RESET register domain: HWRST Notes: â€¢ The VBUS wake-up comparator is automatically turned on when a VAC or VBUS plug detection event occurs, in order to perform the precharge and enable the ACA feature. â€¢ The VBUS over-voltage comparator is automatically turned on when a VBUS plug is present, in order to protect the LDOUSB LDO from the CHRG_PMID input supply.		
Type	RW		

7	6	5	4	3	2	1	0
VBUS_CHRG_VSYS	Reserved	VBUS_DISCHRG	VBUS_IADP_SRC	VBUS_IADP_SINK	VBUS_ACT_COMP	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	VBUS_CHRG_VSYS	0: VBUS 2.5-kÎ© pull-up on VSYS is disabled 1: VBUS 2.5-kÎ© pull-up on VSYS is enabled (VBUS charge mode) Note: OTG1.3	RW	0
6	Reserved		RO	0
5	VBUS_DISCHRG	0: VBUS 10-kÎ© pull-down is disabled 1: VBUS 10-kÎ© pull-down is enabled (VBUS discharge mode) Note: OTG1.3	RW	0
4	VBUS_IADP_SRC	0: VBUS IADP 1.4-mA current source is disabled 1: VBUS IADP 1.4-mA current source is enabled Note: OTG2.0	RW	0
3	VBUS_IADP_SINK	0: VBUS IADP 1.5-mA current sink is disabled 1: VBUS IADP 1.5-mA current sink is enabled Note: OTG2.0	RW	0
2	VBUS_ACT_COMP	0: VBUS sleep / active comparators are disabled. 1: VBUS sleep / active comparators are enabled Note: If OTG 1.3 (OTG_REV = 0) selected & VBUS_ACT_COMP = 1, it enables: VA_VBUS_VLD, VA_SESS_VLD, VB_SESS_VLD, VB_SESS_END If OTG 2.0 (OTG_REV = 1) selected & VBUS_ACT_COMP = 1, it enables: VA_VBUS_VLD, VOTG_SESS_VLD, VADP_PRB, VADP_SNS Note: OTG1.2, OTG2.0	RW	0
1	Reserved		RO	0
0	Reserved		RO	0

1.14.2.3 USB_VBUS_CTRL_CLR Register

Table 1-185. USB_VBUS_CTRL_CLR

Address offset	0x02	**I2C Address**	0x49
Physical Address	0x255 **Instance**	FUNC_USB_OTG	
Description	USB VBUS Control Clear register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
VBUS_CHRG_VSYS	Reserved	VBUS_DISCHRG	VBUS_IADP_SRC	VBUS_IADP_SINK	VBUS_ACT_COMP	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	VBUS_CHRG_VSYS	See USB_VBUS_CTRL_SET description	RW	0
6	Reserved		RO	0
5	VBUS_DISCHRG	See USB_VBUS_CTRL_SET description	RW	0
4	VBUS_IADP_SRC	See USB_VBUS_CTRL_SET description	RW	0
3	VBUS_IADP_SINK	See USB_VBUS_CTRL_SET description	RW	0
2	VBUS_ACT_COMP	See USB_VBUS_CTRL_SET description	RW	0
1	Reserved		RO	0
0	Reserved		RO	0

1.14.2.4 USB_ID_CTRL_SET Register

Table 1-186. USB_ID_CTRL_SET

Address offset	0x03	**I2C Address**	0x49
Physical Address	0x256 **Instance**	FUNC_USB_OTG	
Description	USB ID Control Set register RESET register domain: HWRST Note: The ID wake-up comparator is controlled by the ID_WK_UP_COMP register bit, available in the USB_WAKEUP register.		
Type	RW		

7	6	5	4	3	2	1	0
ID_PU_220K	ID_PU_100K	ID_GND_DRV	ID_SRC_16U	ID_SRC_5U	ID_ACT_COMP	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	ID_PU_220K	0: ID 220-kÎ© pull-up on LDOUSB is disabled 1: ID 220-kÎ© pull-up on LDOUSB is enabled	RW	0
6	ID_PU_100K	0: ID 100-kÎ© pull-up on LDOUSB is disabled 1: ID 100-kÎ© pull-up on LDOUSB is enabled	RW	0
5	ID_GND_DRV	0: ID 10-kÎ© pull-down is disabled. 1: ID 10-kÎ© pull-down is enabled (ground drive mode)	RW	0
4	ID_SRC_16U	0: ID 16Î¼A current source is disabled 1: ID 16Î¼A current source is enabled Note: BC1.1	RW	0
3	ID_SRC_5U	0: ID 5Î¼A current source is disabled 1: ID 5Î¼A current source is enabled	RW	0

Bits	Field Name	Description	Type	Reset
2	ID_ACT_COMP	0: Sleep / active comparators disabled 1: Sleep / active comparators enabled Note: OTG1.2, OTG2.0, BC1.1	RW	0
1	Reserved		RO	0
0	Reserved		RO	0

1.14.2.5 USB_ID_CTRL_CLEAR Register

Table 1-187. USB_ID_CTRL_CLEAR

Address offset	0x04	**I2C Address**	0x49
Physical Address	0x257 **Instance**	FUNC_USB_OTG	
Description	USB ID Control Clear register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
ID_PU_220K	ID_PU_100K	ID_GND_DRV	ID_SRC_16U	ID_SRC_5U	ID_ACT_COMP	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	ID_PU_220K	See USB_ID_CTRL_SET description	RW	0
6	ID_PU_100K	See USB_ID_CTRL_SET description	RW	0
5	ID_GND_DRV	See USB_ID_CTRL_SET description	RW	0
4	ID_SRC_16U	See USB_ID_CTRL_SET description	RW	0
3	ID_SRC_5U	See USB_ID_CTRL_SET description	RW	0
2	ID_ACT_COMP	See USB_ID_CTRL_SET description	RW	0
1	Reserved		RO	0
0	Reserved		RO	0

1.14.2.6 USB_VBUS_INT_SRC Register

Table 1-188. USB_VBUS_INT_SRC

Address offset	0x05			**I2C Address**	0x49
Physical Address	0x258	**Instance**		FUNC_USB_OTG	
Description	USB VBUS Interrupt Source register RESET register domain: HWRST Notes: â€¢ The USB_VBUS_INT_SRC source register represents the debounced current status of the VBUS line. â€¢ VBUS comparators outputs status are continuously updating this source register. â€¢ The VB_SESS_END comparator polarity is inverted in the analog OTG section. â€¢ Therefore, when no VBUS plug is present, only the VB_SESS_END status of the register USB_VBUS_INT_SRC is at 1. â€¢ The USB_VBUS_INT_SRC source register is not affected by the configured low / high enables located in the USB_VBUS_INT_EN_LO_SET, USB_VBUS_INT_EN_LO_CLR, USB_VBUS_INT_EN_HI_SET, and USB_VBUS_INT_EN_HI_CLR registers. â€¢ Indeed, those enables are only affecting the latched interrupts USB_VBUS_INT_LATCH_SET and USB_VBUS_INT_LATCH_CLR registers. â€¢ VB_SESS_END polarity is always inverted, even in USB_VBUS_INT_LATCH_SET and USB_VBUS_INT_LATCH_CLR registers. â€¢ Reserved BIT_4 is used for ADP interrupt. It does not require a source or an enable low bit.				
Type	RO				

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	Reserved	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	Type	Reset
7	VOTG_SESS_VLD	0: VBUS line does not reach VOTG_SESS_VLD threshold 1: VBUS line reaches VOTG_SESS_VLD threshold Note: OTG2.0	RO	0
6	VADP_PRB	0: VBUS line does not reach VADP_PRB threshold 1: VBUS line reaches VADP_PRB threshold Note: OTG2.0	RO	0
5	VADP_SNS	0: VBUS line does not reach VADP_SNS threshold 1: VBUS line reaches VADP_SNS threshold Note: OTG2.0	RO	0
4	Reserved		RO	0
3	VA_VBUS_VLD	0: VBUS line does not reach VA_VBUS_VLD threshold 1: VBUS line reaches VA_VBUS_VLD threshold Note: OTG1.3, OTG2.0	RO	0
2	VA_SESS_VLD	0: VBUS line does not reach VA_SESS_VLD threshold 1: VBUS line reaches VA_SESS_VLD threshold Note: OTG1.3	RO	0
1	VB_SESS_VLD	0: VBUS line does not reach VB_SESS_VLD threshold 1: VBUS line reaches VB_SESS_VLD threshold Note: OTG1.3	RO	0
0	VB_SESS_END	0: VBUS line reaches VB_SESS_END threshold 1: VBUS line does not reach VB_SESS_END threshold Note: OTG1.3	RO	1

1.14.2.7 USB_VBUS_INT_LATCH_SET Register

Table 1-189. USB_VBUS_INT_LATCH_SET

Address offset	0x06	**I2C Address**	0x49
Physical Address	0x259 **Instance**	FUNC_USB_OTG	
Description	USB VBUS Interrupt Latch Set register RESET register domain: HWRST Notes: â€¢ In normal operation, this USB_VBUS_LATCH_SET register is generally used in read mode only â€¢ The VBUS wake-up comparator has its dedicated interrupt line â€¢ The VBUS over-voltage comparator has its interrupt mechanism â€¢ The interrupt mechanism is working identical for all VBUS interrupt sources, even for the specific analog inverted VB_SESS_END: - 0: No interrupt occurred - 1: An interrupt occurred, on either a rising or falling edge of the VBUS â€¢ All VBUS active interrupts present in the USB_VBUS_INT_LATCH_SET and USB_VBUS_INT_LATCH_CLR registers are ORed to the same interrupt handler line #22 (VBUS)		
Type	RW		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
6	VADP_PRB	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
5	VADP_SNS	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
4	ADP	Depending on USB_OTG_ADP_CTRL.ADP_MODE [1:0] 0: No ADP interrupt occurred (probing or sensing) 1: An ADP interrupt occurred (probing or sensing) Note: OTG2.0	RW	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3 and OTG2.0	RW	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0

1.14.2.8 USB_VBUS_INT_LATCH_CLR Register

Table 1-190. USB_VBUS_INT_LATCH_CLR

Address offset	0x07			**I2C Address**	0x49
Physical Address	0x25A	**Instance**		FUNC_USB_OTG	
Description	USB VBUS Interrupt Latch Clear register RESET register domain: HWRST Notes: â€¢ Writing 0xFF clears all captured events				
Type	RW				

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
6	VADP_PRB	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
5	VADP_SNS	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
4	ADP	See USB_VBUS_INT_LATCH_SET description Note: OTG2.0	RW	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3 and OTG2.0	RW	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0

1.14.2.9 USB_VBUS_INT_EN_LO_SET Register

Table 1-191. USB_VBUS_INT_EN_LO_SET

Address offset	0x08			**I2C Address**	0x49
Physical Address	0x25B	**Instance**		FUNC_USB_OTG	
Description	USB VBUS Interrupt Enable Low Set register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	Reserved	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
6	VADP_PRB	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
5	VADP_SNS	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
4	Reserved		RO	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3 and OTG2.0	RW	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0

1.14.2.10 USB_VBUS_INT_EN_LO_CLR Register

Table 1-192. USB_VBUS_INT_EN_LO_CLR

Address offset	0x09	**I2C Address**	0x49
Physical Address	0x25C **Instance**	FUNC_USB_OTG	
Description	USB VBUS Interrupt enable Low Set register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	Reserved	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
6	VADP_PRB	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
5	VADP_SNS	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
4	Reserved		RO	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3 and OTG2.0	RW	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0

1.14.2.11 USB_VBUS_INT_EN_HI_SET Register

Table 1-193. USB_VBUS_INT_EN_HI_SET

Address offset	0x0A			**I2C Address**	0x49
Physical Address	0x25D	**Instance**		FUNC_USB_OTG	
Description	USB VBUS Interrupt enable High Set register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
6	VADP_PRB	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
5	VADP_SNS	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
4	ADP	See USB_VBUS_INT_LATCH_SET description Note: OTG2.0	RW	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3 and OTG2.0	RW	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0

1.14.2.12 USB_VBUS_INT_EN_HI_CLR Register

Table 1-194. USB_VBUS_INT_EN_HI_CLR

Address offset	0x0B			**I2C Address**	0x49
Physical Address	0x25E	**Instance**		FUNC_USB_OTG	
Description	USB VBUS Interrupt enable High Clear register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
6	VADP_PRB	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
5	VADP_SNS	See USB_VBUS_INT_SRC description Note: OTG2.0	RW	0
4	ADP	See USB_VBUS_INT_LATCH_SET description Note: OTG2.0	RW	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3 and OTG2.0	RW	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description Note: OTG1.3	RW	0

1.14.2.13 USB_ID_INT_SRC Register

Table 1-195. USB_ID_INT_SRC

Address offset	0x0C	**I2C Address**	0x49
Physical Address	0x25F **Instance**	FUNC_USB_OTG	
Description	USB ID Interrupt register RESET register domain: HWRST Notes: â€¢ The USB_ID_INT_SRC source register represents the debounced current status of the ID line. â€¢ ID comparators outputs status are continuously updating this source register. â€¢ Only 1 comparator output at a time is showing a status at 1, the other outputs staying at 0. â€¢ Therefore, when an ID plug is present or not, only one status of the register USB_ID_INT_SRC is at 1. â€¢ The USB_ID_INT_SRC source register is not affected by the configured low / high enables located in the following registers USB_ID_INT_EN_LO_SET, USB_ID_INT_EN_LO_CLR, USB_ID_INT_EN_HI_SET, and USB_ID_INT_EN_HI_CLR. â€¢ Indeed, those enables are only affecting the latched interrupts USB_ID_INT_LATCH_SET and USB_INT_LATCH_CLR registers â€¢ All ID active interrupts present in the USB_ID_INT_LATCH_SET and USB_ID_INT_LATCH_CLR registers are ORed to the same interrupt handler line #20 (ID).		
Type	RO		

7	6	5	4	3	2	1	0
Reserved			ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	ID_FLOAT	0: ID line does not reach the ID_FLOAT threshold 1: ID line reaches ID_FLOAT threshold Note: OTG1.3, OTG2.0, BC1.1	RO	0
3	ID_A	0: ID line does not reach the ID_A threshold 1: ID line reaches ID_A threshold Note: BC1.1	RO	0
2	ID_B	0: ID line does not reach the ID_B threshold 1: ID line reaches ID_B threshold Note: BC1.1	RO	0
1	ID_C	0: ID line does not reach the ID_C threshold 1: ID line reaches ID_C threshold Note: BC1.1	RO	0
0	ID_GND	0: ID line does not reach the ID_GND threshold 1: ID line reaches ID_GND threshold Note: OTG1.3, OTG2.0, BC1.1	RO	0

1.14.2.14 USB_ID_INT_LATCH_SET Register

Table 1-196. USB_ID_INT_LATCH_SET

Address offset	0x0D	**I2C Address**	0x49
Physical Address	0x260 **Instance**	FUNC_USB_OTG	
Description	USB ID Interrupt Latch Set register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	ID_FLOAT	See USB_ID_INT_SRC description	RW	0
3	ID_A	See USB_ID_INT_SRC description	RW	0
2	ID_B	See USB_ID_INT_SRC description	RW	0
1	ID_C	See USB_ID_INT_SRC description	RW	0
0	ID_GND	See USB_ID_INT_SRC description	RW	0

1.14.2.15 USB_ID_INT_LATCH_CLR Register

Table 1-197. USB_ID_INT_LATCH_CLR

Address offset	0x0E	**I2C Address**	0x49
Physical Address	0x261 **Instance**	FUNC_USB_OTG	
Description	USB ID Interrupt Latch Clear register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	ID_FLOAT	See USB_ID_INT_SRC description	RW	0
3	ID_A	See USB_ID_INT_SRC description	RW	0
2	ID_B	See USB_ID_INT_SRC description	RW	0
1	ID_C	See USB_ID_INT_SRC description	RW	0
0	ID_GND	See USB_ID_INT_SRC description	RW	0

1.14.2.16 USB_ID_INT_EN_LO_SET Register

Table 1-198. USB_ID_INT_EN_LO_SET

Address offset	0x0F	**I2C Address**	0x49
Physical Address	0x262 **Instance**	FUNC_USB_OTG	
Description	USB ID Interrupt Enable Low Set register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	ID_FLOAT	See USB_ID_INT_SRC description	RW	0
3	ID_A	See USB_ID_INT_SRC description	RW	0
2	ID_B	See USB_ID_INT_SRC description	RW	0
1	ID_C	See USB_ID_INT_SRC description	RW	0
0	ID_GND	See USB_ID_INT_SRC description	RW	0

1.14.2.17 USB_ID_INT_EN_LO_CLR Register

Table 1-199. USB_ID_INT_EN_LO_CLR

Address offset	0x10	**I2C Address**	0x49
Physical Address	0x263 **Instance**	FUNC_USB_OTG	
Description	USB ID Interrupt Enable Low Clear register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	ID_FLOAT	See USB_ID_INT_SRC description	RW	0
3	ID_A	See USB_ID_INT_SRC description	RW	0
2	ID_B	See USB_ID_INT_SRC description	RW	0
1	ID_C	See USB_ID_INT_SRC description	RW	0
0	ID_GND	See USB_ID_INT_SRC description	RW	0

1.14.2.18 USB_ID_INT_EN_HI_SET Register

Table 1-200. USB_ID_INT_EN_HI_SET

Address offset	0x11	**I2C Address**	0x49
Physical Address	0x264 **Instance**	FUNC_USB_OTG	
Description	USB ID Interrupt Enable High Set register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	ID_FLOAT	See USB_ID_INT_SRC description	RW	0
3	ID_A	See USB_ID_INT_SRC description	RW	0
2	ID_B	See USB_ID_INT_SRC description	RW	0
1	ID_C	See USB_ID_INT_SRC description	RW	0
0	ID_GND	See USB_ID_INT_SRC description	RW	0

1.14.2.19 USB_ID_INT_EN_HI_CLR Register

Table 1-201. USB_ID_INT_EN_HI_CLR

Address offset	0x12	**I2C Address**	0x49
Physical Address	0x265 **Instance**	FUNC_USB_OTG	
Description	USB ID Interrupt Enable High Clear register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	ID_FLOAT	See USB_ID_INT_SRC description	RW	0
3	ID_A	See USB_ID_INT_SRC description	RW	0
2	ID_B	See USB_ID_INT_SRC description	RW	0
1	ID_C	See USB_ID_INT_SRC description	RW	0
0	ID_GND	See USB_ID_INT_SRC description	RW	0

1.14.2.20 USB_OTG_ADP_CTRL Register

Table 1-202. USB_OTG_ADP_CTRL

Address offset	0x13			**I2C Address**	0x49
Physical Address	0x266	**Instance**		FUNC_USB_OTG	
Description	Control USB OTG ADP register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved					ADP_EN	ADP_MODE	

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2	ADP_EN	ADP feature selection 0: ADP is disable (default) 1: ADP is enabled	RW	0
1:0	ADP_MODE	00: ADP digital module is disabled. 01: ADP sensing mode is enabled. 10: ADP probing mode as an A-device is enabled. 11: ADP probing mode as a B-device is enabled. Note: OTG2.0	RW	0x0

1.14.2.21 USB_OTG_ADP_HIGH Register

Table 1-203. USB_OTG_ADP_HIGH

Address offset	0x14			**I2C Address**	0x49
Physical Address	0x267	**Instance**		FUNC_USB_OTG	
Description	USB OTG ADP high register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
T_ADP_HIGH							

Bits	Field Name	Description	Type	Reset
7:0	T_ADP_HIGH	Timing interval value (high limit) - Number of 32-kHz clock cycles 00000000: 0 clock cycle 00000001: 1 clock cycle ... 11111110: 254 clock cycles 11111111: 255 clock cycles Note: OTG2.0	RW	0x00

1.14.2.22 USB_OTG_ADP_LOW Register

Table 1-204. USB_OTG_ADP_LOW

Address offset	0x15			**I2C Address**	0x49
Physical Address	0x268	**Instance**		FUNC_USB_OTG	
Description	USB OTG ADP Low register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
T_ADP_LOW							

Bits	Field Name	Description	Type	Reset
7:0	T_ADP_LOW	Timing interval value (high limit) - Number of 32-kHz clock cycles 00000000: 0 clock cycle 00000001: 1 clock cycle ... 11111110: 254 clock cycles 11111111: 255 clock cycles Note: OTG2.0	RW	0x00

1.14.2.23 USB_OTG_ADP_RISE Register

Table 1-205. USB_OTG_ADP_RISE

Address offset	0x16			**I2C Address**	0x49
Physical Address	0x269	**Instance**		FUNC_USB_OTG	
Description	USB OTG ADP Rise register RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
T_ADP_RISE							

Bits	Field Name	Description	Type	Reset
7:0	T_ADP_RISE	ADP charge time duration - Number of 32-kHz clock cycles 00000000: 0 clock cycle 00000001: 1 clock cycle ... 11111110: 254 clock cycles 11111111: 255 clock cycles Note: OTG2.0	RO	0x00

1.14.2.24 USB_OTG_REVISION Register

Table 1-206. USB_OTG_REVISION

Address offset	0x17			**I2C Address**	0x49
Physical Address	0x26A	**Instance**		FUNC_USB_OTG	
Description	USB OTG Revision register RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved							OTG_REV

Bits	Field Name	Description	Type	Reset
7:1	Reserved	0: OTG Revision 1.3 (associated VBUS detection features enabled) 1: OTG Revision 2.0 (associated VBUS detection features enabled)	RO	0x00
0	OTG_REV	0: OTG1.3 1: OTG2.0	RO	X

1.15 FUNC_VIBRATOR Registers

1.15.1 FUNC_VIBRATOR Registers Mapping Summary

This section provides information on the FUNC_VIBRATOR Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.15.1.1 FUNC_VIBRATOR Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
VIBRA_CTRL	RW	8	0x06	0x49	0x00	0x270

1.15.2 FUNC_VIBRATOR Register Descriptions

1.15.2.1 VIBRA_CTRL Register

Table 1-207. VIBRA_CTRL

Address offset	0x00	**I2C Address**	0x49
Physical Address	0x270 **Instance**	FUNC_VIBRATOR	
Description	Vibrator Control Register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					PWM_DUTY_SEL		PWM_FREQ_SEL

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2:1	PWM_DUTY_SEL	PWM duty cycle selection: 00: 100% duty cycle 01: 75% duty cycle 10: 50% duty cycle 11: 25% duty cycle (default)	RW	0x3
0	PWM_FREQ_SEL	PWM Frequency selection: 0: 4Hz (default) 1: Reserved for test purpose only - ES1.0: 32kHz ES2.0->: 500Hz	RW	0

1.16 FUNC_GPIO Registers

1.16.1 FUNC_GPIO Registers Mapping Summary

This section provides information on the FUNC_GPIO Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.16.1.1 FUNC_GPIO Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
GPIO_DATA_IN	RO	8	0x00	0x49	0x00	0x280
GPIO_DATA_DIR	RW	8	0x00	0x49	0x01	0x281
GPIO_DATA_OUT	RW	8	0x00	0x49	0x02	0x282
GPIO_DEBOUNCE_EN	RW	8	0x00	0x49	0x03	0x283
GPIO_CLEAR_DATA_OUT	WO	8	0x00	0x49	0x04	0x284
GPIO_SET_DATA_OUT	WO	8	0x00	0x49	0x05	0x285
PU_PD_GPIO_CTRL1	RW	8	0b0XXX XX0X	0x49	0x06	0x286
PU_PD_GPIO_CTRL2	RW	8	0b0X01 0101	0x49	0x07	0x287
OD_OUTPUT_GPIO_CTRL	RW	8	0x00	0x49	0x08	0x288

1.16.2 FUNC_GPIO Register Descriptions

1.16.2.1 GPIO_DATA_IN Register

Table 1-208. GPIO_DATA_IN

Address offset	0x00			**I2C Address**	0x49
Physical Address	0x280	**Instance**		FUNC_GPIO	
Description	GPIO Data input register RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
GPIO_7_IN	GPIO_6_IN	GPIO_5_IN	GPIO_4_IN	GPIO_3_IN	GPIO_2_IN	GPIO_1_IN	GPIO_0_IN

Bits	Field Name	Description	Type	Reset
7	GPIO_7_IN	Data read value (in) of the GPIO_7	RO	0
6	GPIO_6_IN	Data read value (in) of the GPIO_6	RO	0
5	GPIO_5_IN	Data read value (in) of the GPIO_5	RO	0
4	GPIO_4_IN	Data read value (in) of the GPIO_4	RO	0
3	GPIO_3_IN	Data read value (in) of the GPIO_3	RO	0
2	GPIO_2_IN	Data read value (in) of the GPIO_2	RO	0
1	GPIO_1_IN	Data read value (in) of the GPIO_1	RO	0
0	GPIO_0_IN	Data read value (in) of the GPIO_0	RO	0

1.16.2.2 GPIO_DATA_DIR Register

Table 1-209. GPIO_DATA_DIR

Address offset	0x01			**I2C Address**	0x49
Physical Address	0x281	**Instance**		FUNC_GPIO	
Description	GPIO data direction RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
GPIO_7_DIR	GPIO_6_DIR	GPIO_5_DIR	GPIO_4_DIR	GPIO_3_DIR	GPIO_2_DIR	GPIO_1_DIR	GPIO_0_DIR

Bits	Field Name	Description	Type	Reset
7	GPIO_7_DIR	0: buffer in input configuration (default) 1: buffer in output configuration	RW	0
6	GPIO_6_DIR	0: buffer in input configuration (default) 1: buffer in output configuration	RW	0
5	GPIO_5_DIR	0: buffer in input configuration (default) 1: buffer in output configuration	RW	0
4	GPIO_4_DIR	0: buffer in input configuration (default) 1: buffer in output configuration	RW	0
3	GPIO_3_DIR	0: buffer in input configuration (default) 1: buffer in output configuration	RW	0
2	GPIO_2_DIR	0: buffer in input configuration (default) 1: buffer in output configuration	RW	0
1	GPIO_1_DIR	0: buffer in input configuration (default) 1: buffer in output configuration	RW	0
0	GPIO_0_DIR	0: buffer in input configuration (default) 1: buffer in output configuration	RW	0

1.16.2.3 GPIO_DATA_OUT Register

Table 1-210. GPIO_DATA_OUT

Address offset	0x02			**I2C Address**	0x49
Physical Address	0x282	**Instance**		FUNC_GPIO	
Description	GPIO Data output register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
GPIO_7_OUT	GPIO_6_OUT	GPIO_5_OUT	GPIO_4_OUT	GPIO_3_OUT	GPIO_2_OUT	GPIO_1_OUT	GPIO_0_OUT

Bits	Field Name	Description	Type	Reset
7	GPIO_7_OUT	Data write value (out) of the GPIO_7	RW	0
6	GPIO_6_OUT	Data write value (out) of the GPIO_6	RW	0
5	GPIO_5_OUT	Data write value (out) of the GPIO_5	RW	0
4	GPIO_4_OUT	Data write value (out) of the GPIO_4	RW	0
3	GPIO_3_OUT	Data write value (out) of the GPIO_3	RW	0
2	GPIO_2_OUT	Data write value (out) of the GPIO_2	RW	0
1	GPIO_1_OUT	Data write value (out) of the GPIO_1	RW	0
0	GPIO_0_OUT	Data write value (out) of the GPIO_0	RW	0

1.16.2.4 GPIO_DEBOUNCE_EN Register

Table 1-211. GPIO_DEBOUNCE_EN

Address offset	0x03	**I2C Address**	0x49
Physical Address	0x283 **Instance**	FUNC_GPIO	
Description	GPIO Debounce enable register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_7_DEBOUNCE_EN	GPIO_6_DEBOUNCE_EN	GPIO_5_DEBOUNCE_EN	GPIO_4_DEBOUNCE_EN	GPIO_3_DEBOUNCE_EN	GPIO_2_DEBOUNCE_EN	GPIO_1_DEBOUNCE_EN	GPIO_0_DEBOUNCE_EN

Bits	Field Name	Description	Type	Reset
7	GPIO_7_DEBOUNCE_EN	0: No debounce (default) 1: Debounce enabled	RW	0
6	GPIO_6_DEBOUNCE_EN	0: No debounce (default) 1: Debounce enabled	RW	0
5	GPIO_5_DEBOUNCE_EN	0: No debounce (default) 1: Debounce enabled	RW	0
4	GPIO_4_DEBOUNCE_EN	0: No debounce (default) 1: Debounce enabled	RW	0
3	GPIO_3_DEBOUNCE_EN	0: No debounce (default) 1: Debounce enabled	RW	0
2	GPIO_2_DEBOUNCE_EN	0: No debounce (default) 1: Debounce enabled	RW	0
1	GPIO_1_DEBOUNCE_EN	0: No debounce (default) 1: Debounce enabled	RW	0
0	GPIO_0_DEBOUNCE_EN	0: No debounce (default) 1: Debounce enabled	RW	0

1.16.2.5 GPIO_CLEAR_DATA_OUT Register

Table 1-212. GPIO_CLEAR_DATA_OUT

Address offset	0x04	**I2C Address**	0x49
Physical Address	0x284 **Instance**	FUNC_GPIO	
Description	GPIO Clear Data Out Register RESET register domain: HWRST		
Type	WO		

7	6	5	4	3	2	1	0
GPIO_7_CLEAR_DATA_OUT	GPIO_6_CLEAR_DATA_OUT	GPIO_5_CLEAR_DATA_OUT	GPIO_4_CLEAR_DATA_OUT	GPIO_3_CLEAR_DATA_OUT	GPIO_2_CLEAR_DATA_OUT	GPIO_1_CLEAR_DATA_OUT	GPIO_0_CLEAR_DATA_OUT

Bits	Field Name	Description	Type	Reset
7	GPIO_7_CLEAR_DATA_OUT	0: no action on GPIO_7 bit 1: CLEAR GPIO_7 bit	WO	0
6	GPIO_6_CLEAR_DATA_OUT	0: no action on GPIO_6 bit 1: CLEAR GPIO_6 bit	WO	0
5	GPIO_5_CLEAR_DATA_OUT	0: no action on GPIO_5 bit 1: CLEAR GPIO_5 bit	WO	0
4	GPIO_4_CLEAR_DATA_OUT	0: no action on GPIO_4 bit 1: CLEAR GPIO_4 bit	WO	0
3	GPIO_3_CLEAR_DATA_OUT	0: no action on GPIO_3 bit 1: CLEAR GPIO_3 bit	WO	0
2	GPIO_2_CLEAR_DATA_OUT	0: no action on GPIO_2 bit 1: CLEAR GPIO_2 bit	WO	0
1	GPIO_1_CLEAR_DATA_OUT	0: no action on GPIO_1 bit 1: CLEAR GPIO_1 bit	WO	0
0	GPIO_0_CLEAR_DATA_OUT	0: no action on GPIO_0 bit 1: CLEAR GPIO_0 bit	WO	0

1.16.2.6 GPIO_SET_DATA_OUT Register

Table 1-213. GPIO_SET_DATA_OUT

Address offset	0x05	**I2C Address**	0x49
Physical Address	0x285 **Instance**	FUNC_GPIO	
Description	GPIO Set Data Out Register RESET register domain: HWRST		
Type	WO		

7	6	5	4	3	2	1	0
GPIO_7_SET_DATA_OUT	GPIO_6_SET_DATA_OUT	GPIO_5_SET_DATA_OUT	GPIO_4_SET_DATA_OUT	GPIO_3_SET_DATA_OUT	GPIO_2_SET_DATA_OUT	GPIO_1_SET_DATA_OUT	GPIO_0_SET_DATA_OUT

Bits	Field Name	Description	Type	Reset
7	GPIO_7_SET_DATA_OUT	0: no action on GPIO_7 bit 1: SET GPIO_7 bit	WO	0
6	GPIO_6_SET_DATA_OUT	0: no action on GPIO_6 bit 1: SET GPIO_6 bit	WO	0
5	GPIO_5_SET_DATA_OUT	0: no action on GPIO_5 bit 1: SET GPIO_5 bit	WO	0
4	GPIO_4_SET_DATA_OUT	0: no action on GPIO_4 bit 1: SET GPIO_4 bit	WO	0
3	GPIO_3_SET_DATA_OUT	0: no action on GPIO_3 bit 1: SET GPIO_3 bit	WO	0
2	GPIO_2_SET_DATA_OUT	0: no action on GPIO_2 bit 1: SET GPIO_2 bit	WO	0
1	GPIO_1_SET_DATA_OUT	0: no action on GPIO_1 bit 1: SET GPIO_1 bit	WO	0
0	GPIO_0_SET_DATA_OUT	0: no action on GPIO_0 bit 1: SET GPIO_0 bit	WO	0

1.16.2.7 PU_PD_GPIO_CTRL1 Register

Table 1-214. PU_PD_GPIO_CTRL1

Address offset	0x06	**I2C Address**	0x49
Physical Address	0x286 **Instance**	FUNC_GPIO	
Description	Pull-up Pull-down control register RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the GPIO direction and type (Open drain / Push-Pull)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	GPIO_3_PD	GPIO_2_PU	GPIO_2_PD	GPIO_1_PU	GPIO_1_PD	Reserved	GPIO_0_PD

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	GPIO_3_PD	0: Pull-down not enabled 1: Pull-down enabled	RW	X

Bits	Field Name	Description	Type	Reset
5	GPIO_2_PU	0: Pull-up not enabled 1: Pull-up enabled	RW	X
4	GPIO_2_PD	0: Pull-down not enabled 1: Pull-down enabled	RW	X
3	GPIO_1_PU	0: Pull-up not enabled 1: Pull-up enabled	RW	X
2	GPIO_1_PD	0: Pull-down not enabled 1: Pull-down enabled	RW	X
1	Reserved		RO	0
0	GPIO_0_PD	0: Pull-down not enabled 1: Pull-down enabled (default)	RW	X

1.16.2.8 PU_PD_GPIO_CTRL2 Register

Table 1-215. PU_PD_GPIO_CTRL2

Address offset	0x07		**I2C Address**	0x49	
Physical Address	0x287	**Instance**	FUNC_GPIO		
Description	Pull-up Pull-down control register RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the GPIO direction and type (Open drain / Push-Pull)				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	GPIO_7_PD	GPIO_6_PU	GPIO_6_PD	GPIO_5_PU	GPIO_5_PD	GPIO_4_PU	GPIO_4_PD

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	GPIO_7_PD	0: Pull-down not enabled 1: Pull-down enabled (default)	RW	X
5	GPIO_6_PU	0: Pull-up not enabled (default) 1: Pull-up enabled	RW	0
4	GPIO_6_PD	0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
3	GPIO_5_PU	0: Pull-up not enabled (default) 1: Pull-up enabled	RW	0
2	GPIO_5_PD	0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1
1	GPIO_4_PU	0: Pull-up not enabled (default) 1: Pull-up enabled	RW	0
0	GPIO_4_PD	0: Pull-down not enabled 1: Pull-down enabled (default)	RW	1

1.16.2.9 OD_OUTPUT_GPIO_CTRL Register

Table 1-216. OD_OUTPUT_GPIO_CTRL

Address offset	0x08		**I2C Address**	0x49	
Physical Address	0x288	**Instance**	FUNC_GPIO		
Description	Open Drain control register RESET register domain: HWRST Note: It is user responsibility to take care about the GPIO direction and type (Open drain / Push-Pull) versus the pull-up/pull-down selections				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	Reserved	GPIO_5_OD	Reserved	Reserved	GPIO_2_OD	GPIO_1_OD	Reserved

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	GPIO_5_OD	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)	RW	0
4	Reserved		RO	0
3	Reserved		RO	0
2	GPIO_2_OD	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)	RW	0
1	GPIO_1_OD	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)	RW	0
0	Reserved		RO	0

1.17 FUNC_USB Registers

1.17.1 FUNC_USB Registers Mapping Summary

This section provides information on the FUNC_USB Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.17.1.1 FUNC_USB Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
USB_EN	RW	8	0x00	0x49	0x02	0x292

1.17.2 FUNC_USB Register Descriptions

1.17.2.1 USB_EN Register

Table 1-217. USB_EN

Address offset	0x02		**I2C Address**	0x49	
Physical Address	0x292	**Instance**	FUNC_USB		
Description	USB enable RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved							USB_EN

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RW	0x00
0	USB_EN	0: USB Clock OCP is auto gated (default) 1: USB Clock OCP is free running	RW	0

1.18 FUNC_GPADC Registers

1.18.1 FUNC_GPADC Registers Mapping Summary

This section provides information on the FUNC_GPADC Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.18.1.1 FUNC_GPADC Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
GPADC_CTRL1	RW	8	0x00	0x49	0x00	0x2C0
GPADC_CTRL2	RW	8	0x06	0x49	0x01	0x2C1
GPADC_RT_CTRL	RW	8	0x00	0x49	0x02	0x2C2
GPADC_AUTO_CTRL	RW	8	0x00	0x49	0x03	0x2C3
GPADC_STATUS	RO	8	0x10	0x49	0x04	0x2C4
GPADC_RT_SELECT	RW	8	0x00	0x49	0x05	0x2C5
GPADC_RT_CONV0_LSB	RO	8	0x00	0x49	0x06	0x2C6
GPADC_RT_CONV0_MSB	RO	8	0x00	0x49	0x07	0x2C7
GPADC_AUTO_SELECT	RW	8	0x00	0x49	0x08	0x2C8
GPADC_AUTO_CONV0_LSB	RO	8	0x00	0x49	0x09	0x2C9
GPADC_AUTO_CONV0_MSB	RO	8	0x00	0x49	0x0A	0x2CA
GPADC_AUTO_CONV1_LSB	RO	8	0x00	0x49	0x0B	0x2CB
GPADC_AUTO_CONV1_MSB	RO	8	0x00	0x49	0x0C	0x2CC
GPADC_SW_SELECT	RW	8	0x00	0x49	0x0D	0x2CD
GPADC_SW_CONV0_LSB	RO	8	0x00	0x49	0x0E	0x2CE
GPADC_SW_CONV0_MSB	RO	8	0x00	0x49	0x0F	0x2CF
GPADC_THRES_CONV0_LSB	RW	8	0x00	0x49	0x10	0x2D0
GPADC_THRES_CONV0_MSB	RW	8	0x00	0x49	0x11	0x2D1
GPADC_THRES_CONV1_LSB	RW	8	0x00	0x49	0x12	0x2D2
GPADC_THRES_CONV1_MSB	RW	8	0x00	0x49	0x13	0x2D3
GPADC_SMPS_ILMONITOR_EN	RW	8	0x07	0x49	0x14	0x2D4
GPADC_SMPS_VSEL_MONITORING	RO	8	0x00	0x49	0x15	0x2D5

1.18.2 FUNC_GPADC Register Descriptions

1.18.2.1 GPADC_CTRL1 Register

Table 1-218. GPADC_CTRL1

Address offset	0x00			**I2C Address**	0x49
Physical Address	0x2C0	**Instance**		FUNC_GPADC	
Description	GPADC Control Register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
RESERVED	RESERVED	CURRENT_SRC_CH3		CURRENT_SRC_CH0		BAT_REMOVAL_DET	GPADC_FORCE

Bits	Field Name	Description	Type	Reset
7	RESERVED	This bit field is reserved.	RW	0
6	RESERVED	This bit field is reserved.	RW	0
5:4	CURRENT_SRC_CH3	Current Source selection for GPADC Channel 3 input 00: 0uA 01: 10uA 10: 400uA 11: 800uA	RW	0x0
3:2	CURRENT_SRC_CH0	Current Source selection for GPADC Channel 0 input 00: 0uA (default) 01: 5uA 10: 15uA 11: 20uA	RW	0x0
1	BAT_REMOVAL_DET	Enable Battery Removal detection comparator 0: Comparator not enabled (default) 1: Comparator enabled	RW	0
0	GPADC_FORCE	Force GPADC module to active (Always On) 0: GPADC OFF. The GPADC is controlled by conversion request in all modes (default) 1: GPADC ON (Always ON - will allow conversion latency)	RW	0

1.18.2.2 GPADC_CTRL2 Register

Table 1-219. GPADC_CTRL2

Address offset	0x01			**I2C Address**	0x49
Physical Address	0x2C1	**Instance**		FUNC_GPADC	
Description	GPADC Control Register RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved					RESERVED		Reserved

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2:1	RESERVED	This bit field is reserved.	RW	0x3
0	Reserved		RO	0

1.18.2.3 GPADC_RT_CTRL Register

Table 1-220. GPADC_RT_CTRL

Address offset	0x02	**I2C Address**	0x49
Physical Address	0x2C2 **Instance**	FUNC_GPADC	
Description	GPADC Real Time Control register RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						EXTEND_DELAY	START_POLARITY

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1	EXTEND_DELAY	Extended Delay. Delay before conversion in SW and Real Time 0: 0us (default) 1: +450us	RW	0
0	START_POLARITY	Polarity of the GPADC_START event 0: on rising edge event (default) 1: on falling edge event	RW	0

1.18.2.4 GPADC_AUTO_CTRL Register

Table 1-221. GPADC_AUTO_CTRL

Address offset	0x03	**I2C Address**	0x49
Physical Address	0x2C3 **Instance**	FUNC_GPADC	
Description	GPADC Automatic Control register (Periodic) RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
SHUTDOWN_CONV1	SHUTDOWN_CONV0	AUTO_CONV1_EN	AUTO_CONV0_EN	COUNTER_CONV			

Bits	Field Name	Description	Type	Reset
7	SHUTDOWN_CONV1	Shut down control based on Auto conversions (only for CONV1) 0: shut down not enabled (default) 1: enable shut down of the platform if interrupt is not clear within delay time	RW	0
6	SHUTDOWN_CONV0	Shut down control based on Auto conversions (only for CONV0) 0: shut down not enabled (default) 1: enable shut down of the platform if interrupt is not clear within delay time	RW	0
5	AUTO_CONV1_EN	Automatic Conversion 1 enabling 0: Automatic Conversion 1 is not enable (defaults) 1: Automatic Conversion 1 is enabled	RW	0
4	AUTO_CONV0_EN	Automatic Conversion 0 enabling 0: Automatic Conversion 0 is not enable (defaults) 1: Automatic Conversion 0 is enabled	RW	0
3:0	COUNTER_CONV	Time slot between conversions (RT and SW modes) or two consecutive conversions (Auto mode) 0000: 1/32s (default) 0001: 1/16s 0010: 1/8s 1110: 512s 1111: 1024s	RW	0x0

1.18.2.5 GPADC_STATUS Register

Table 1-222. GPADC_STATUS

Address offset	0x04			**I2C Address**	0x49
Physical Address	0x2C4	**Instance**		FUNC_GPADC	
Description	GPADC Status Register RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved			GPADC_AVAILABLE	Reserved			

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	GPADC_AVAILABLE	GPADC status 0: Conversions not completed. GPADC not available (busy) 1: Conversions completed. GPADC available	RO	1
3:0	Reserved		RO	0x0

1.18.2.6 GPADC_RT_SELECT Register

Table 1-223. GPADC_RT_SELECT

Address offset	0x05			**I2C Address**	0x49
Physical Address	0x2C5	**Instance**		FUNC_GPADC	
Description	GPADC Real time Channel selection for Conversion 0 and Conversion 1 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
RT_CONV_EN	Reserved			RT_CONV0_SEL			

Bits	Field Name	Description	Type	Reset
7	RT_CONV_EN	Real Time Conversion enabling 0: Real Time Conversion is not enable (defaults) 1: Real Time Conversion is enabled	RW	0
6:4	Reserved		RO	0x0
3:0	RT_CONV0_SEL	Channel selection for Conversion 0 in Real Time mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 1110: GPADC Channel 14 1111: GPADC Channel 15	RW	0x0

1.18.2.7 GPADC_RT_CONV0_LSB Register

Table 1-224. GPADC_RT_CONV0_LSB

Address offset	0x06			**I2C Address**	0x49
Physical Address	0x2C6	**Instance**		FUNC_GPADC	
Description	GPADC data results of the Real time conversion 0 (LSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
RT_CONV0_LSB							

Bits	Field Name	Description	Type	Reset
7:0	RT_CONV0_LSB	Real Time Conversion 0 data result (LSB) <7:0>	RO	0x00

1.18.2.8 GPADC_RT_CONV0_MSB Register

Table 1-225. GPADC_RT_CONV0_MSB

Address offset	0x07			**I2C Address**	0x49
Physical Address	0x2C7	**Instance**		FUNC_GPADC	
Description	GPADC data results of the Real time conversion 0 (MSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved				RT_CONV0_MSB			

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:0	RT_CONV0_MSB	Real Time Conversion 0 data result (MSB) <11:8>	RO	0x0

1.18.2.9 GPADC_AUTO_SELECT Register

Table 1-226. GPADC_AUTO_SELECT

Address offset	0x08		**I2C Address**	0x49	
Physical Address	0x2C8	**Instance**	FUNC_GPADC		
Description	GPADC Automatic (Periodic) Channel selection for Conversion 0 and Conversion 1 RESET register domain: HWRST Note: All Selected channels are queued and converted from channel 0 to 11 The first (lower) converted channel results is placed in GPADC_AUTO_CONV0 register and the second one is placed in GPADC_AUTO_CONV1 register. It is why it is recommended to put the lower channel to convert in AUTO_CONV0_SEL and the higher channel to convert in AUTO_CONV1_SEL.				
Type	RW				

7	6	5	4	3	2	1	0
AUTO_CONV1_SEL				AUTO_CONV0_SEL			

Bits	Field Name	Description	Type	Reset
7:4	AUTO_CONV1_SEL	Channel selection for Conversion 1 in Automatic mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 1110: GPADC Channel 14 1111: GPADC Channel 15	RW	0x0
3:0	AUTO_CONV0_SEL	Channel selection for Conversion 0 in Automatic mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 1110: GPADC Channel 14 1111: GPADC Channel 15	RW	0x0

1.18.2.10 GPADC_AUTO_CONV0_LSB Register

Table 1-227. GPADC_AUTO_CONV0_LSB

Address offset	0x09		**I2C Address**	0x49	
Physical Address	0x2C9	**Instance**	FUNC_GPADC		
Description	GPADC data results of the Automatic (Periodic) conversion 0 (LSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
AUTO_CONV0_LSB							

Bits	Field Name	Description	Type	Reset
7:0	AUTO_CONV0_LSB	AUTO Conversion 0 data result (LSB) <7:0>	RO	0x00

1.18.2.11 GPADC_AUTO_CONV0_MSB Register

Table 1-228. GPADC_AUTO_CONV0_MSB

Address offset	0x0A			**I2C Address**	0x49
Physical Address	0x2CA	**Instance**		FUNC_GPADC	
Description	GPADC data results of the Automatic (Periodic) conversion 0 (MSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved				AUTO_CONV0_MSB			

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:0	AUTO_CONV0_MSB	AUTO Conversion 0 data result (MSB) <11:8>	RO	0x0

1.18.2.12 GPADC_AUTO_CONV1_LSB Register

Table 1-229. GPADC_AUTO_CONV1_LSB

Address offset	0x0B			**I2C Address**	0x49
Physical Address	0x2CB	**Instance**		FUNC_GPADC	
Description	GPADC data results of the Automatic (Periodic) conversion 1 (LSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
AUTO_CONV1_LSB							

Bits	Field Name	Description	Type	Reset
7:0	AUTO_CONV1_LSB	AUTO Conversion 1 data result (LSB) <7:0>	RO	0x00

1.18.2.13 GPADC_AUTO_CONV1_MSB Register

Table 1-230. GPADC_AUTO_CONV1_MSB

Address offset	0x0C			**I2C Address**	0x49
Physical Address	0x2CC	**Instance**		FUNC_GPADC	
Description	GPADC data results of the Automatic (Periodic) conversion 1 (MSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved				AUTO_CONV1_MSB			

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:0	AUTO_CONV1_MSB	AUTO Conversion 1 data result (MSB) <11:8>	RO	0x0

1.18.2.14 GPADC_SW_SELECT Register

Table 1-231. GPADC_SW_SELECT

Address offset	0x0D			**I2C Address**	0x49
Physical Address	0x2CD	**Instance**		FUNC_GPADC	
Description	GPADC Software Channel selection for Conversion 0 RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
SW_CONV_EN	Reserved		SW_START_CONV0	SW_CONV0_SEL			

Bits	Field Name	Description	Type	Reset
7	SW_CONV_EN	Software Conversion enabling 0: Software Conversion is not enable (defaults) 1: Software Conversion is enabled	RW	0
6:5	Reserved		RO	0x0
4	SW_START_CONV0	Toggle bit used by host processor to start a conversion (Conversion0) on selected channel by SW_CONV0_SEL Writing logical 0 in this bit has no effect	RW	0
3:0	SW_CONV0_SEL	Channel selection for Conversion 0 in SW mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 1110: GPADC Channel 14 1111: GPADC Channel 15	RW	0x0

1.18.2.15 GPADC_SW_CONV0_LSB Register

Table 1-232. GPADC_SW_CONV0_LSB

Address offset	0x0E			**I2C Address**	0x49
Physical Address	0x2CE	**Instance**		FUNC_GPADC	
Description	GPADC data results of the Software conversion 0 (LSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
SW_CONV0_LSB							

Bits	Field Name	Description	Type	Reset
7:0	SW_CONV0_LSB	SW Conversion 0 data result (LSB) <7:0>	RO	0x00

1.18.2.16 GPADC_SW_CONV0_MSB Register

Table 1-233. GPADC_SW_CONV0_MSB

Address offset	0x0F			**I2C Address**	0x49
Physical Address	0x2CF	**Instance**		FUNC_GPADC	
Description	GPADC data results of the Software conversion 0 (MSB) RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
Reserved				SW_CONV0_MSB			

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:0	SW_CONV0_MSB	SW Conversion 0 data result (MSB) <11:8>	RO	0x0

1.18.2.17 GPADC_THRES_CONV0_LSB Register

Table 1-234. GPADC_THRES_CONV0_LSB

Address offset	0x10			**I2C Address**	0x49
Physical Address	0x2D0	**Instance**		FUNC_GPADC	
Description	LSB of Threshold reference to be compared to the Conversion 0 results RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
THRES_CONV0_LSB							

Bits	Field Name	Description	Type	Reset
7:0	THRES_CONV0_LSB	Threshold value for Conversion 0 (LSB) <7:0>	RW	0x00

1.18.2.18 GPADC_THRES_CONV0_MSB Register

Table 1-235. GPADC_THRES_CONV0_MSB

Address offset	0x11			**I2C Address**	0x49
Physical Address	0x2D1	**Instance**		FUNC_GPADC	
Description	MSB of Threshold reference to be compared to the Conversion 0 results RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
THRES_CONV0_POL	Reserved			THRES_CONV0_MSB			

Bits	Field Name	Description	Type	Reset
7	THRES_CONV0_POL	Threshold conversion 0 polarity 0: Interrupt generated if Conversion0 result is above threshold 1: Interrupt generated if Conversion0 result is below threshold	RW	0
6:4	Reserved		RO	0x0
3:0	THRES_CONV0_MSB	Threshold value for Conversion 0 (MSB) <11:8>	RW	0x0

1.18.2.19 GPADC_THRES_CONV1_LSB Register

Table 1-236. GPADC_THRES_CONV1_LSB

Address offset	0x12	**I2C Address**	0x49
Physical Address	0x2D2 **Instance**	FUNC_GPADC	
Description	LSB of Threshold reference to be compared to the Conversion 1 results RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
THRES_CONV1_LSB							

Bits	Field Name	Description	Type	Reset
7:0	THRES_CONV1_LSB	Threshold value for Conversion 1 (LSB) <7:0>	RW	0x00

1.18.2.20 GPADC_THRES_CONV1_MSB Register

Table 1-237. GPADC_THRES_CONV1_MSB

Address offset	0x13	**I2C Address**	0x49
Physical Address	0x2D3 **Instance**	FUNC_GPADC	
Description	MSB of Threshold reference to be compared to the Conversion 1 results RESET register domain: HWRST		
Type	RW		

7	6	5	4	3	2	1	0
THRES_CONV1_POL	Reserved			THRES_CONV1_MSB			

Bits	Field Name	Description	Type	Reset
7	THRES_CONV1_POL	Threshold conversion 1 polarity 0: Interrupt generated if Conversion0 result is above threshold 1: Interrupt generated if Conversion0 result is below threshold	RW	0
6:4	Reserved		RO	0x0
3:0	THRES_CONV1_MSB	Threshold value for Conversion 1 (MSB) <11:8>	RW	0x0

1.18.2.21 GPADC_SMPS_ILMONITOR_EN Register

Table 1-238. GPADC_SMPS_ILMONITOR_EN

Address offset	0x14			**I2C Address**	0x49
Physical Address	0x2D4	**Instance**		FUNC_GPADC	
Description	GPADC SMPS selection for current measurement RESET register domain: HWRST				
Type	RW				

7	6	5	4	3	2	1	0
Reserved	SMPS_COMPMODE	SMPS_ILMON_EN	SMPS_ILMON_VADC_MEAS_EN	SMPS_ILMON_SEL			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	SMPS_COMPMODE	ES1.0: Reserved ES2.0->: ILMON comparator enable. This bit can be written 1 ONLY if SMPS_ILMON_EN bit is already 1. If SMPS_ILMON_EN is written with 0, ILMON_COMPMODE bit will be automatically written with 0 too. 0: ILMON Comparator is disabled 1: ILMON Comparator is enabled	RW	0
5	SMPS_ILMON_EN	Selection of GPADC ILMONITOR feature 0: Feature not enabled (default) 1: Feature is enabled	RW	0
4	SMPS_ILMON_VADC_MEAS_EN	ES1.0: This bit was named SMPS_ILMON_REXT_EN Provide the capability to implement an external resistor on TESTV (secondary pad function) for the I Load Monitoring measurement (ILMONITORING) 0: Feature not enable (default) 1:External resistor on TESTV pad ES2.0->: This bit is named SMPS_ILMON_VADC_MEAS_EN Allow monitoring of the SMPS load current proflile including 100us peaks, for SW development purposes by using VPROG pin (without external resistor). In this mode also offset and gain compensation by trimming are included. 0: Feature not enable (default) 1 :Feature is enabled	RW	0
3:0	SMPS_ILMON_SEL	SMPS I Load Monitor selection (exclusive) 0000: ES1.0: SMPS12 / SMPS123 (default) ES2.0->: SMPS12 / SMPS123, no more default 0001: SMPS3 0010: SMPS45 / SMPS457 0011: SMPS6 0100: SMPS7 0101: SMPS8 - Reserved as not supported ES1.0->0110: SMPS9 - Reserved as not supported ES1.0->0111: ES1.0: SMPS12 (0000 - default) ES2.0->: No SMPS selection (default) Others: ES1.0: SMPS12 (0000 - default) ES2.0->: No SMPS selection (default)	RW	0x7

1.18.2.22 GPADC_SMPS_VSEL_MONITORING Register

Table 1-239. GPADC_SMPS_VSEL_MONITORING

Address offset	0x15			**I2C Address**	0x49
Physical Address	0x2D5	**Instance**		FUNC_GPADC	
Description	GPADC SMPS voltage monitoring related to ILMONITORING measurement RESET register domain: HWRST				
Type	RO				

7	6	5	4	3	2	1	0
ACTIVE_PHASE	SMPS_VSEL_MONITORING						

Bits	Field Name	Description	Type	Reset
7	ACTIVE_PHASE	ES1.0: Reserved bit ES2.0->: Specify the number of active phases during measurements 0: One phase 1: Multi-phases (more than one)	RO	0
6:0	SMPS_VSEL_MONITORING	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register	RO	0x00

1.19 INTERNAL_DESIGNREV Registers

1.19.1 INTERNAL_DESIGNREV Registers Mapping Summary

This section provides information on the INTERNAL_DESIGNREV Module Instance within this product. Each of the registers within the Module Instance is described separately below.

1.19.1.1 INTERNAL_DESIGNREV Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
DESIGNREV	RO	8	0x0X	0x4A	0x00	0x357

1.19.2 INTERNAL_DESIGNREV Register Descriptions

1.19.2.1 DESIGNREV Register

Table 1-240. DESIGNREV

Address offset	0x00	**I2C Address**	0x4A
Physical Address	0x357 **Instance**	INTERNAL_DESIGNREV	
Description	Silicon version number register ES1.0: Not described in RM but accessible ES2.0->: Described in RM and accessible RESET register domain: POR Test Key: KEY0		
Type	RO		

7	6	5	4	3	2	1	0
Reserved				DESIGNREV			

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:0	DESIGNREV	Value depending on silicon version number (From metal bits) 0000 - CS1.0 Revision 0001 - CS2.0 Revision 0010 - CS2.1 Revision 0011 - CS2.2 Revision	RO	0xX

1.20 INTERNAL_TRIM_GPADC Registers

1.20.1 INTERNAL_TRIM_GPADC Registers Mapping Summary

This section provides information on the INTERNAL_TRIM_GPADC Module Instance within this product. Each of the registers within the Module Instance is described separately below.

The GPADC Calibration Parameters are trimmed during the final test process. They are in Read Only mode for the user.

1.20.1.1 INTERNAL_TRIM_GPADC Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	I2C Address	Address Offset	Physical Address
GPADC_TRIM1	RW	8	0x00	0x4A	0x00	0x3CD
GPADC_TRIM2	RW	8	0x00	0x4A	0x01	0x3CE
GPADC_TRIM3	RW	8	0x00	0x4A	0x02	0x3CF
GPADC_TRIM4	RW	8	0x00	0x4A	0x03	0x3D0
GPADC_TRIM5	RW	8	0x00	0x4A	0x04	0x3D1
GPADC_TRIM6	RW	8	0x00	0x4A	0x05	0x3D2
GPADC_TRIM7	RW	8	0x00	0x4A	0x06	0x3D3
GPADC_TRIM8	RW	8	0x00	0x4A	0x07	0x3D4
GPADC_TRIM9	RW	8	0x00	0x4A	0x08	0x3D5
GPADC_TRIM10	RW	8	0x00	0x4A	0x09	0x3D6
GPADC_TRIM11	RW	8	0x00	0x4A	0x0A	0x3D7
GPADC_TRIM12	RW	8	0x00	0x4A	0x0B	0x3D8
GPADC_TRIM13	RW	8	0x00	0x4A	0x0C	0x3D9
GPADC_TRIM14	RW	8	0x00	0x4A	0x0D	0x3DA
GPADC_TRIM15	RW	8	0x00	0x4A	0x0E	0x3DB
GPADC_TRIM16	RW	8	0x00	0x4A	0x0F	0x3DC

1.20.2 INTERNAL_TRIM_GPADC Register Descriptions

1.20.2.1 GPADC_TRIM1 Register

Table 1-241. GPADC_TRIM1

Address offset	0x00	**I2C Address**	0x4A
Physical Address	0x3CD **Instance**	INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1		
Type	RW		

7	6	5	4	3	2	1	0
GPADC_IN0_TRIM1							

Bits	Field Name	Description	Type	Reset
7:0	GPADC_IN0_TRIM1	Low compensation value for channels GPADC_IN0/1/3/4/5. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.2 GPADC_TRIM2 Register

Table 1-242. GPADC_TRIM2

Address offset	0x01	**I2C Address**	0x4A
Physical Address	0x3CE **Instance**	INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1		
Type	RW		

7	6	5	4	3	2	1	0
GPADC_IN0_TRIM2							

Bits	Field Name	Description	Type	Reset
7:0	GPADC_IN0_TRIM2	High compensation value MSB for channels GPADC_IN0/1/3/4/5. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.3 GPADC_TRIM3 Register

Table 1-243. GPADC_TRIM3

Address offset	0x02	**I2C Address**	0x4A
Physical Address	0x3CF **Instance**	INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1		
Type	RW		

7	6	5	4	3	2	1	0
GPADC_IN2_TRIM1							

Bits	Field Name	Description	Type	Reset
7:0	GPADC_IN2_TRIM1	Low compensation value for GPADC_IN2 channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.4 GPADC_TRIM4 Register

Table 1-244. GPADC_TRIM4

Address offset	0x03	**I2C Address**	0x4A
Physical Address	0x3D0 **Instance**	INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1		
Type	RW		

7	6	5	4	3	2	1	0
GPADC_IN2_TRIM2							

Bits	Field Name	Description	Type	Reset
7:0	GPADC_IN2_TRIM2	High compensation value for GPADC_IN2 channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.5 GPADC_TRIM5 Register

Table 1-245. GPADC_TRIM5

Address offset	0x04	**I2C Address**	0x4A
Physical Address	0x3D1 **Instance**	INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1		
Type	RW		

7	6	5	4	3	2	1	0
VBAT_TRIM1							

Bits	Field Name	Description	Type	Reset
7:0	VBAT_TRIM1	Low compensation value for VBAT channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.6 GPADC_TRIM6 Register

Table 1-246. GPADC_TRIM6

Address offset	0x05	**I2C Address**	0x4A
Physical Address	0x3D2 **Instance**	INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1		
Type	RW		

7	6	5	4	3	2	1	0
VBAT_TRIM2							

Bits	Field Name	Description	Type	Reset
7:0	VBAT_TRIM2	High compensation value for VBAT channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.7 GPADC_TRIM7 Register

Table 1-247. GPADC_TRIM7

Address offset	0x06			**I2C Address**	0x4A
Physical Address	0x3D3	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
VCC_TRIM1							

Bits	Field Name	Description	Type	Reset
7:0	VCC_TRIM1	Low compensation value for VCC channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.8 GPADC_TRIM8 Register

Table 1-248. GPADC_TRIM8

Address offset	0x07			**I2C Address**	0x4A
Physical Address	0x3D4	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
VCC_TRIM2							

Bits	Field Name	Description	Type	Reset
7:0	VCC_TRIM2	High compensation value for VCC channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.9 GPADC_TRIM9 Register

Table 1-249. GPADC_TRIM9

Address offset	0x08			**I2C Address**	0x4A
Physical Address	0x3D5	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
VBKP_TRIM1							

Bits	Field Name	Description	Type	Reset
7:0	VBKP_TRIM1	Low compensation value for VBKP channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.10 GPADC_TRIM10 Register

Table 1-250. GPADC_TRIM10

Address offset	0x09			**I2C Address**	0x4A
Physical Address	0x3D6	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
VBKP_TRIM2							

Bits	Field Name	Description	Type	Reset
7:0	VBKP_TRIM2	High compensation value for VBKP channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.11 GPADC_TRIM11 Register

Table 1-251. GPADC_TRIM11

Address offset	0x0A			**I2C Address**	0x4A
Physical Address	0x3D7	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
VAC_TRIM1							

Bits	Field Name	Description	Type	Reset
7:0	VAC_TRIM1	Low compensation value for VAC channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.12 GPADC_TRIM12 Register

Table 1-252. GPADC_TRIM12

Address offset	0x0B			**I2C Address**	0x4A
Physical Address	0x3D8	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
VAC_TRIM2							

Bits	Field Name	Description	Type	Reset
7:0	VAC_TRIM2	High compensation value for VAC channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.13 GPADC_TRIM13 Register

Table 1-253. GPADC_TRIM13

Address offset	0x0C			**I2C Address**	0x4A
Physical Address	0x3D9	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
VBUS_TRIM1							

Bits	Field Name	Description	Type	Reset
7:0	VBUS_TRIM1	Low compensation value for VBUS channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.14 GPADC_TRIM14 Register

Table 1-254. GPADC_TRIM14

Address offset	0x0D			**I2C Address**	0x4A
Physical Address	0x3DA	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
VBUS_TRIM2							

Bits	Field Name	Description	Type	Reset
7:0	VBUS_TRIM2	High compensation value for VBUS channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.15 GPADC_TRIM15 Register

Table 1-255. GPADC_TRIM15

Address offset	0x0E			**I2C Address**	0x4A
Physical Address	0x3DB	**Instance**		INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1				
Type	RW				

7	6	5	4	3	2	1	0
ID_TRIM1							

Bits	Field Name	Description	Type	Reset
7:0	ID_TRIM1	High compensation value for ID channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

1.20.2.16 GPADC_TRIM16 Register

Table 1-256. GPADC_TRIM16

Address offset	0x0F	**I2C Address**	0x4A
Physical Address	0x3DC **Instance**	INTERNAL_TRIM_GPADC	
Description	RESET register domain: POR Test Key: KEY1		
Type	RW		

7	6	5	4	3	2	1	0
ID_TRIM2							

Bits	Field Name	Description	Type	Reset
7:0	ID_TRIM2	High compensation value for ID channel. Bit 7 to 1: absolute value. Bit 0: sign bit (0: positive; 1: negative)	RW	0x00

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