Switch-mode power converter compensation made easy

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Using this paper as a quick look-up reference can help designers compensate the most popular switch-mode power converter topologies.

Engineers have been designing switch-mode power converters for some time now. If you're new to the design field or you don't compensate converters all the time, compensation requires some research to do correctly. This paper will break the procedure down into a step-by-step process that you can follow to compensate a power converter.

We will explain the theory of compensation and why it is necessary, examine various power stages, and show how to determine where to place the poles and zeros of the compensation network to compensate a power converter. We will examine typical error amplifiers as well as transconductance amplifiers to see how each affects the control loop and work through a number of topologies/examples so that power engineers have a quick reference when they need to compensate a power converter.

Introduction

A switch-mode power supply (SMPS) regulates the output voltage against any changes in output loading or input line voltage. An SMPS accomplishes this regulation with a feedback loop, which requires compensation if it has an error amplifier with linear feedback. This paper covers the necessary definitions and theory required to understand how a linear feedback loop works. We will define poles and zeros and power-stage characteristics, along with various error amplifiers; discuss isolated feedback and optocouplers; and give examples of how to compensate various buck, boost and buck-boost topologies. We will cover voltage-mode control and current-mode control methods. Unless otherwise noted, equations and graphs depict fixed-frequency, continuous-conduction-mode (CCM) operation. We will define discontinuous-conduction-mode (DCM) versus CCM, and how each affects the feedback loop. This paper also includes a section on the practical limits of devices used in SMPSs.

Many SMPS designers would appreciate a how-to reference paper that they can use to look up compensation solutions to various topologies with various feedback modes. We are striving to provide this in a single paper.

Control-loop and compensation definitions

As stated previously, a SMPS's primary function is to regulate its output against input/output variations and transients, which requires a feedback loop. **Figure 1** shows a typical SMPS with a feedback loop.

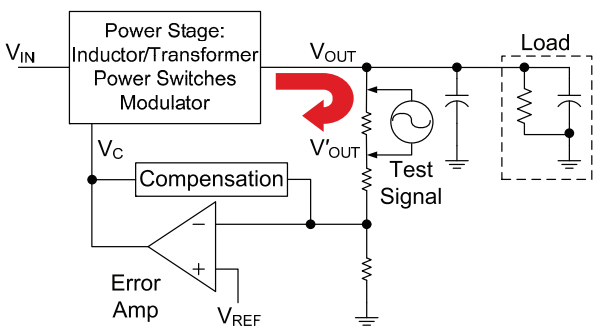


Figure 1. *A test signal injected into the feedback of the control loop measures the frequency response.*

Figure 1 contains a power stage and an error amplifier. The power stage contains all of the magnetics and power switches, as well as a pulse-width modulated (PWM) controller. The error amplifier provides the feedback mechanism and compensation. A voltage divider connected to the output provides a sample of the output voltage, which is compared to a reference voltage by the error amplifier. The error voltage coming out of the error amplifier drives the PWM duty cycle higher if the output voltage is low, or drives the PWM duty cycle lower if the output voltage is high. Thus, the feedback scheme used here is negative feedback. Loop gain is the gain around the feedback loop, comprising the product of error-amplifier gain, modulator gain and power-stage gain. The feedback loop's gain and phase response versus frequency will determine how well the SMPS will function.

The bandwidth of the control loop determines its speed in responding to a transient condition. Compensation adjusts the loop bandwidth and tailors the frequency response. Increasing the loop bandwidth increases the speed at which the SMPS reacts to a transient. Therefore, maximizing the crossover frequency will produce a quicker transient response.

Phase margin, which we discuss in the next section, also plays an important role in compensation. **Figure 2** shows the results of low phase margin. In this case there is ringing after the load transient and the loop is underdamped. This is not a desirable response.

In **Figure 3**, the phase margin has increased; therefore, the waveform does not show any ringing after the load transient. This response is well damped.

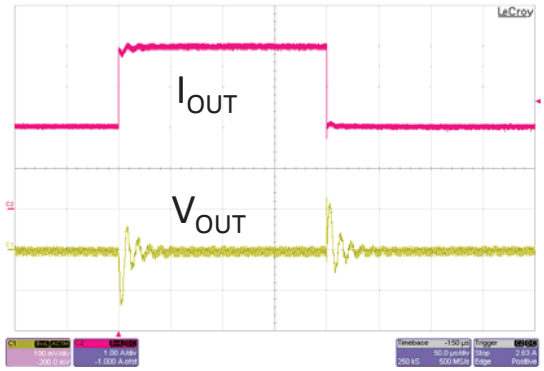


Figure 2:*.Poor transient response characterized by underdamped ringing of the output voltage when stepping the load current.*

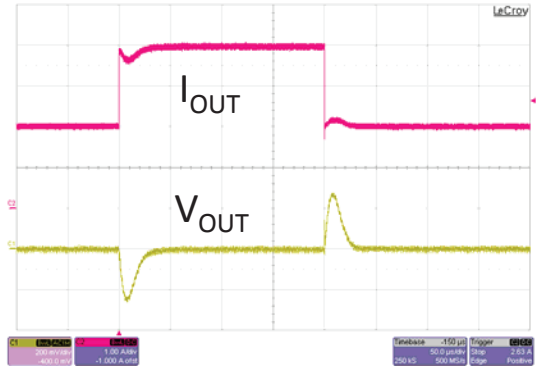


Figure 3. *Good transient response exhibits no ringing with a critically damped characteristic.*

Phase and gain-margin definitions

Phase and gain margin are parameters used to identify the health of a feedback loop. A control loop is unstable if the loop has unity gain when the phase passes through zero. Gain margin is the gain value when the phase passes through 0 degrees. This is measured in decibels and should be a negative number. Phase margin is the value of the phase measured in degrees when the gain passes through zero. This is measured in degrees and should be a positive number (**Figure 4**).

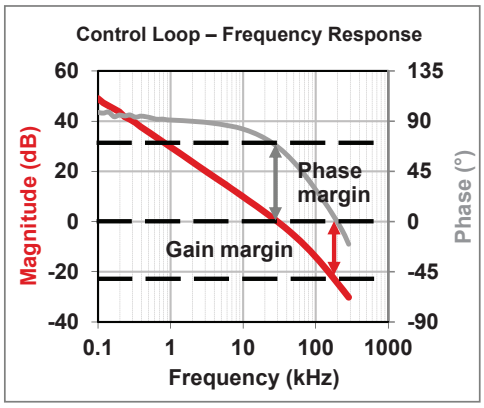


Figure 4. *Phase margin is the difference in degrees when the gain crosses zero. Gain margin is the difference in decibels when the phase crosses zero.*

Sufficient phase margin is required to prevent oscillations. A phase margin of 45 degrees or greater is the design goal. A gain margin of –6 dB is the minimum, while –10 dB is considered good.

Although higher crossovers are generally preferable, there are practical limitations. The rule of thumb is one-fifth to one-tenth the switching frequency. Attenuation at the switching frequency is also important for noise immunity to minimize jitter. The gain should ideally pass through zero with a slope of –20 dB/decade. This will maximize gain margin and will also negate the chance of the gain turning positive at a higher frequency where the phase may be going through zero. If that happens, you could have an unstable control loop.

Poles and zeros definitions

Equation 1 defines a pole where *s* is in the denominator. At the frequency of the pole the gain is –3 dB down and rolling off at a –20 dB/decade slope. The phase starts to decrease one decade before the pole frequency, is 45 degrees down at the pole frequency, and continues to decrease another 45 degrees for one more decade. The total change is –90 degrees over two decades (**Figure 5**).

$$H(s) = \frac{1}{1 + \frac{s}{\omega_P}} \quad (1)$$

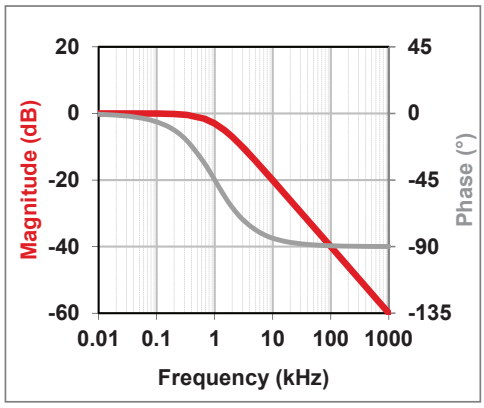


Figure 5. *The Bode plot of a pole shows the gain decreasing by –20 dB/decade, with a phase shift at higher frequencies of –90 degrees.*

Equation 2 defines a zero where *s* is in the numerator. At the frequency of the zero the gain is 3 dB up and increasing at a +20 dB/decade slope. The phase starts to increase one decade before the zero frequency, is 45 degrees up at the zero frequency, and continues to increase another 45 degrees for one more decade. The total change is 90 degrees over two decades (**Figure 6**).

$$H(s) = \frac{1 + \frac{s}{\omega_Z}}{1} \quad (2)$$

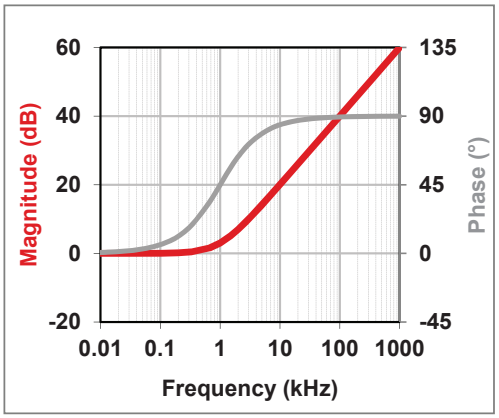


Figure 6. *The Bode plot of a zero shows the gain increasing by +20 dB/decade, with a phase shift at higher frequencies of +90 degrees.*

Figure 7 shows an inverted zero often used with a low-frequency pole when using the mid-band gain as the reference gain, defined by Equation 3. The inverted zero still has *s* in the numerator, but *s* and ω are swapped.

$$H(s) = \frac{1 + \frac{\omega_Z}{s}}{1} \quad (3)$$

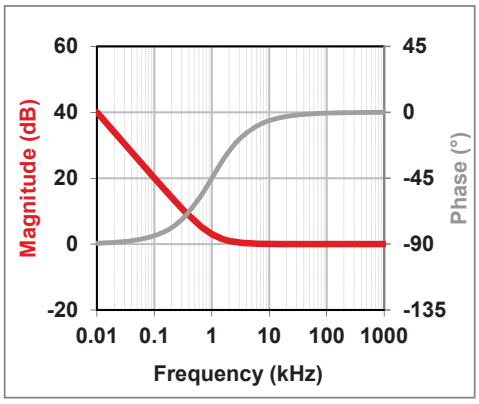


Figure 7. *The Bode plot of an inverted zero shows the gain going up and to the left of the reference gain, shown here as 0 dB. This cancels a pole at some lower frequency so that the phase changes from –90 degrees to 0 degrees.*

A right-half-plane zero is characteristic of boost and buck-boost power stages. The magnitude increases at 20 dB/decade with an associated phase lag of –90 degrees. As you can see in Equation 4, *s* is in the numerator, but it is negative. This makes compensating the converter more difficult (**Figure 8**).

$$H(s) = \frac{1 - \frac{s}{\omega_Z}}{1} \quad (4)$$

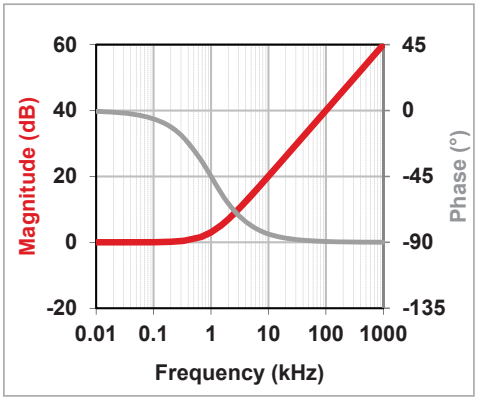


Figure 8. *The Bode plot of a right-half-plane zero shows the gain increasing by +20 dB/decade, with a phase shift at higher frequencies of –90 degrees.*

As mentioned in the introduction, we will discuss two types of loop control methods: voltage-mode control and current-mode control. The control method determines the characteristics of the of the power stage. For example, in a voltage-mode buck converter the inductor-capacitor (LC) filter exhibits a complex conjugate pole at the LC resonant frequency. This means that there are two poles at the same frequency, and the gain changes –40 dB/decade with an associated phase change of –180 degrees. A current-mode buck converter does not have a complex pole at the LC resonant frequency.

Equation 5 shows the transfer function of a complex conjugate pole with a quality factor, Q, associated with the LC filter. Q is a measure of the sensitivity or quality of the tuned circuit. A higher Q value corresponds to a narrower bandwidth of the tuned circuit. A high Q value is not so good for a power-supply output filter, however, because as Q increases the phase slope increases. This means that the phase changes much more quickly over a small band of frequencies, whereas two regular poles would change with a more gradual slope over two decades.

$$H(s) = \frac{1}{1 + \frac{s}{Q_O \cdot \omega_O} + \frac{s^2}{\omega_O^2}} \quad (5)$$

Figure 9 illustrates how phase slope increases as Q increases. Since a high Q LC filter can cause a –180 degree phase shift in the loop Bode plot, it is important to understand the Q of the LC filter in order to compensate for this phase change.

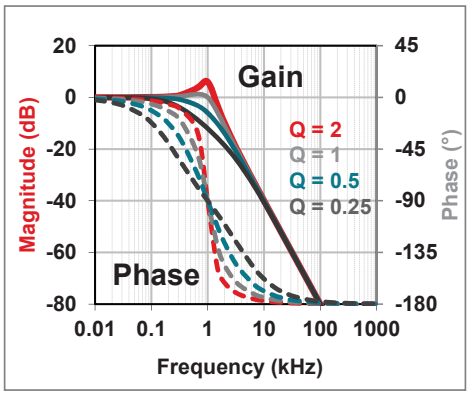


Figure 9. *The Bode plot of a complex conjugate pole shows the gain decreasing by –40 dB/decade, with a phase shift at higher frequencies of –180 degrees.*

Equivalent series resistance zero

The equivalent series resistance (ESR) zero is associated with output capacitance. Although all capacitors exhibit ESR, ceramic capacitors have very low ESR – in the order of 3-5 mΩ. Electrolytic-type capacitors have higher ESR – in the order of 10-20 mΩ for an aluminum polymer and up to hundreds of mΩ for regular electrolytic capacitors.

The ESR in an output capacitor determines the frequency at which the ESR zero occurs; see the numerator in Equation 6. **Figure 10** shows the frequency response of an LC filter with an ESR zero, which comes in at about 10 kHz. The gain transitions from a slope of –40 dB to a slope of –20 dB, and the phase turns positive for 90 degrees over two decades.

$$H(s) = \frac{1 + \frac{s}{\omega_Z}}{1 + \frac{s}{Q_O \cdot \omega_O} + \frac{s^2}{\omega_O^2}} \quad (6)$$

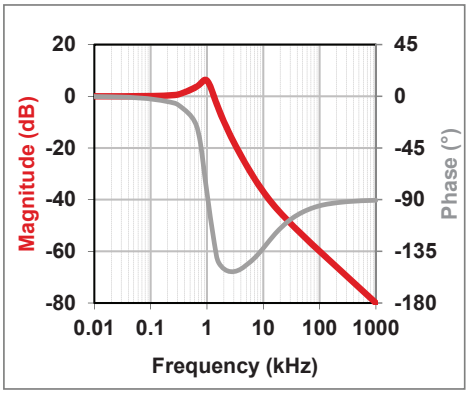


Figure 10. *An ESR zero after the complex conjugate pole causes the slope of the gain to reduce to –20 dB/decade, while the phase shift moves toward –90 degrees.*

Buck-derived topologies

Buck-derived topologies deliver power to the output after reception at the input. Buck-derived topologies running in CCM with voltage-mode feedback have an LC filter response with one complex conjugate pole and one ESR zero. **Figure 11** shows a buck converter with its associated input/output voltage transfer function. As you can see in Equation 7, the output voltage is related to the input voltage multiplied by the on-time duty cycle, D.

$$V_{OUT} = V_{IN} \cdot D \quad (7)$$

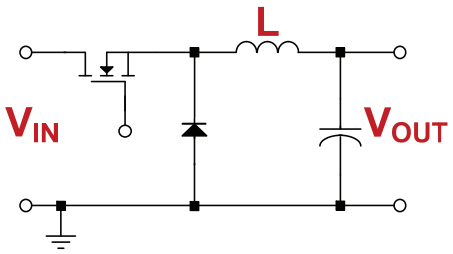


Figure 11. *A buck converter steps down the input to produce a lower output voltage.*

Forward, two-switch forward, active-clamp forward and half-bridge converters are also buck-derived topologies, but their input/output voltage transfer functions are multiplied by the transformer turns ratio. See Equation 8. Push-pull, full bridge and phase-shifted full bridge also have the same input/output voltage transfer function, but with a factor of 2 multiplier as well as the transformer turns ratio. See Equation 9.

$$V_{OUT} = V_{IN} \cdot D \cdot \frac{N_S}{N_P} \quad (8)$$

$$V_{OUT} = V_{IN} \cdot 2 \cdot D \cdot \frac{N_S}{N_P} \quad (9)$$

Boost topologies

Boost topologies deliver energy to the output 180 degrees out of phase with the energy delivered to the input. This causes a right-half-plane zero to appear in the transfer function. **Figure 12** shows a boost power stage, along with its associated input/output voltage transfer function. In Equation 10, D′ is the off-time duty cycle given by D′ = 1 – D.

$$V_{OUT} = V_{IN} \cdot \frac{1}{D'} \quad (10)$$

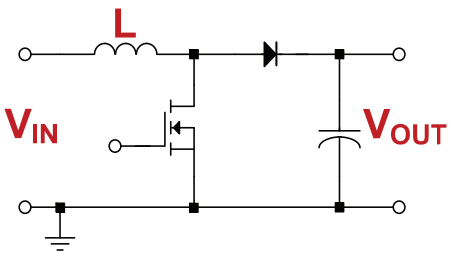


Figure 12. *A boost converter steps up the input to produce a higher output voltage.*

Buck-boost-derived topologies

Inverting buck-boost, flyback, single-ended primary inductor converter (SEPIC), Zeta and Cuk converters are examples of buck-boost-derived topologies. These topologies have the potential to buck down the input voltage or boost up the input voltage, much like the more advanced buck-derived topologies that use a transformer. The exception is the inverting buck-boost, which inverts the polarity of the voltage at the output. Buck-boost topologies store energy in the inductor on the first part of the switching period, delivering that energy to the output during the second part of the switching period. Much like a boost converter, this creates a right-half-plane zero, which as we mentioned before can complicate the compensation of the feedback loop.

Figure 13 shows a schematic of an inverting buck-boost, while Equation 11 shows the input-to-output voltage relationship. Equation 11 holds true for inverting buck-boost, Zeta, Cuk and SEPIC topologies. The flyback equation, Equation 12, has the multiplier of the coupled inductor (transformer) turns ratio.

$$V_{OUT} = V_{IN} \cdot \frac{D}{D'} \quad (11)$$

$$V_{OUT} = V_{IN} \cdot \frac{D}{D'} \cdot \frac{N_S}{N_P} \quad (12)$$

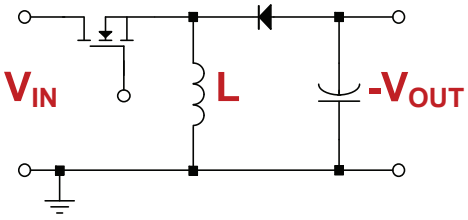


Figure 13. *A single switch buck-boost converter inverts the polarity of the input voltage. The magnitude of the output voltage can be lower or higher than the input.*

Voltage-mode buck

Operation of a voltage-mode buck modulator is very straightforward. Along with the schematic for a voltage-mode buck power stage, **Figure 14** shows how comparing the feedback error voltage, V_C, with a linear ramp, V_{RAMP}, accomplishes PWM.

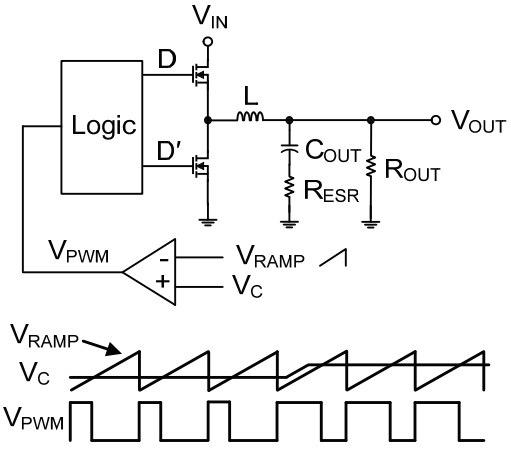


Figure 14. *This voltage-mode-controlled buck converter detail shows the control voltage intersecting the ramp modulating the PWM duty cycle.*

Equations 13 and 14 calculate the duty cycle relationship for a buck converter in CCM:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (13)$$

$$D' = \frac{V_{IN} - V_{OUT}}{V_{IN}} \quad (14)$$

Equation 15 shows the transfer function for a voltage-mode buck converter:

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} = A_{VC} \cdot \frac{1+\frac{s}{\omega_Z}}{1+\frac{s}{Q_O \cdot \omega_O}+\frac{s^2}{\omega_O{}^2}} \quad (15)$$

The transfer function comprises several parts. The first part is the PWM modulator gain. The PWM output is a pulse waveform averaged by the output filter and applied to the load as a direct current (DC) voltage. The modulator gain is the average of this pulse train divided by the control voltage. The control voltage is bounded by the ramp, while the output is bounded by zero and the input voltage. Equation 16 defines the modulator gain for a CCM voltage-mode buck, where the input voltage is divided by the peak-to-peak ramp voltage, V_{RAMP}.

The second part is a complex conjugate pole characteristic of the LC output filter. It rolls off at –40 dB/decade, with a phase change of –180 degrees. See Equation 17. This pole is followed by the ESR zero of the output capacitor in Equation 18, reducing the slope to –20 dB/decade.

$$A_{VC} = \frac{dv_{OUT}}{dv_C} = \frac{d}{dv_C} \cdot \left(v_{IN} \cdot \frac{v_C}{v_{RAMP}} \right) = \frac{V_{IN}}{V_{RAMP}} \quad (16)$$

$$\omega_O = \frac{1}{\sqrt{L \cdot C_{OUT}}} \quad (17)$$

$$\omega_Z = \frac{1}{R_{ESR} \cdot C_{OUT}} \quad (18)$$

The Q associated with the complex conjugate pole determines the slope of the phase. See Equation 19. As we discussed in the section on complex conjugate poles, Q complicates converter compensation because as Q increases, the phase slope increases. This means that the phase changes much quicker over a small band of frequencies, whereas two regular poles would change with a more gradual slope over two decades. A high-Q LC filter can cause a –180 degree phase shift in the loop Bode plot. You may be able to minimize this phase shift by moving the error-amplifier zeros to coincide with the LC resonant frequency. (We will use this method in the voltage-mode buck example.) Equation 19 for Q ignores the output capacitor's ESR and the inductor's DC resistance. Both of these effects will slightly lower the Q.

$$Q_O = \frac{R_{OUT}}{\sqrt{L/C_{OUT}}} \quad (19)$$

We typically see voltage mode used only for buck-derived topologies, because these topologies don't exhibit a right-half-plane zero in the power-stage transfer function. **Figure 15** shows the associated Bode response.

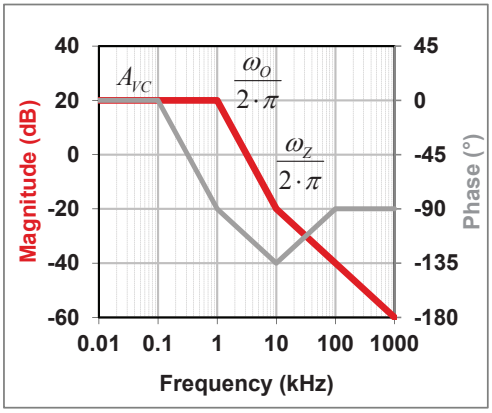


Figure 15. *The voltage-mode buck frequency response has the characteristic complex conjugate pole with ESR zero.*

Current-mode buck

The difference between voltage- and current-mode control is that for current-mode control, the PWM modulator uses the inductor ripple current as the ramp. Voltage-mode control uses a fixed ramp, which contains no information about the inductor current. Current-mode control exhibits some desirable attributes because it samples the inductor current. The inner current loop splits the complex conjugate pole of the filter into two real poles, turning

the modulator into a voltage-controlled current source. Current-mode control also provides a cycle-by-cycle current limit, which is advantageous for protecting the power stage.

Along with these advantages comes a not-so-advantageous attribute: subharmonic oscillation. Subharmonic oscillation occurs when the inductor ripple current does not return to its initial value by the start of next switching cycle. For peak current-mode control, this occurs at a duty cycle greater than 50 percent. With larger inductances, as the slope of the inductor current decreases and tends toward becoming flat, the PWM modulator can trigger on noise, making the problem worse. Subharmonic oscillation is normally characterized by alternating wide and narrow pulses at the switch node. An external ramp added to the inductor current ramp cancels the subharmonic oscillation and is known as slope compensation. This external ramp stabilizes the modulator gain.

Figure 16 shows the schematic of the current-mode buck power stage.

Equations 20 and 21 give the duty-cycle relationship for the current-mode buck in CCM, which is the same as voltage mode:

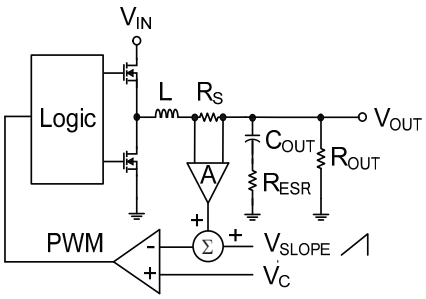


Figure 16. *The current-mode buck power stage incorporates the inductor current sense as an inner control loop. The current loop acts as a lossless damping resistor, splitting the complex conjugate pole of the output filter into two real poles. It turns the modulator into a voltage-controlled current source, where the inductor current is proportional to the control voltage at V_C.*

$$D = \frac{V_{OUT}}{V_{IN}} \tag{20}$$

$$D' = \frac{V_{IN} - V_{OUT}}{V_{IN}} \tag{21}$$

Equation 22 shows the transfer function for the current-mode buck power stage:

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)} \tag{22}$$

As you can see, in Equation 22 the transfer function is made up of gain, A_{VC}, calculated by Equation 23:

$$A_{VC} \approx \frac{R_{OUT}}{R_i} \quad \text{where } R_i = A \cdot R_S. \tag{23}$$

Equations 24 and 25 express two separate poles. The first pole (Equation 24) is related to the output capacitor and the output load:

$$\omega_P \approx \frac{1}{C_{OUT} \cdot R_{OUT}} \tag{24}$$

The second pole (Equation 25) is related to the inductance and V_{SLOPE}. The modulator voltage gain, K_m, is equal to V_{IN}/V_{SLOPE} at D = 0.5 and will have little variation with operating conditions when properly scaling V_{SLOPE}.

$$\omega_L = \frac{K_m \cdot R_i}{L} \quad \text{where } K_m \approx \frac{V_{IN}}{V_{SLOPE}} \text{ at D = 0.5.} \tag{25}$$

The transfer function also contains an ESR zero associated with the output capacitor, expressed as Equation 26:

$$\omega_Z = \frac{1}{R_{ESR} \cdot C_{OUT}} \tag{26}$$

For the peak current-mode buck, Equation 27 calculates the optimal value of slope compensation:

$$V_{SLOPE} = \frac{V_{OUT} \cdot R_i \cdot T}{L} \quad (27)$$

where R_i is the current-sense gain times the sense resistor, and *T* is equal to the switching period, $1/f_{SW}$.

Dozens of papers tackle the subject of modeling current-mode control. Simple average modeling is usually good enough for most applications. More accurate models that look at the control behavior up to and beyond half the switching frequency are becoming more common. While these are simplified, Equation 22 and the Bode plot in **Figure 17** are common for the current-mode buck power stage.

Not all data sheets have enough information to accurately calculate the control-to-output gain. Both the equivalent current-sense gain, R_i, and slope compensation, V_{SLOPE}, are required, but for internally compensated regulators, data sheets may not include the value of R_i, or may not list the value of V_{SLOPE} for switching regulators with internal power switches. Only the power stage L and C_{OUT} are available to adjust the response.

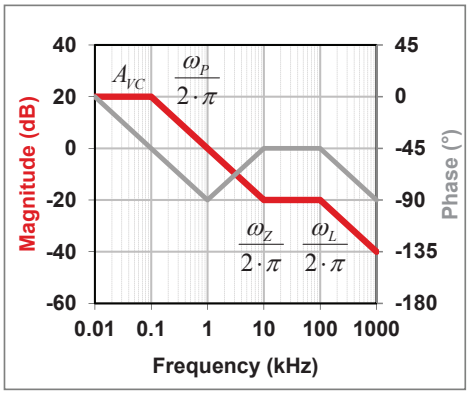


Figure 17. *The current-mode buck power stage exhibits a single pole at ω_P as the dominant characteristic*

Current-mode boost

The current-mode boost is similar to the current-mode buck, but the current-mode boost exhibits a right-half-plane zero in the transfer function. This is because energy is stored in the inductor during the switch on-time and delivered to the output during the off-time. This energy storage and delivery tends to limit the overall loop bandwidth due to the associated phase lag of the right-half-plane zero.

Figure 18 shows the schematic of the current-mode boost power stage.

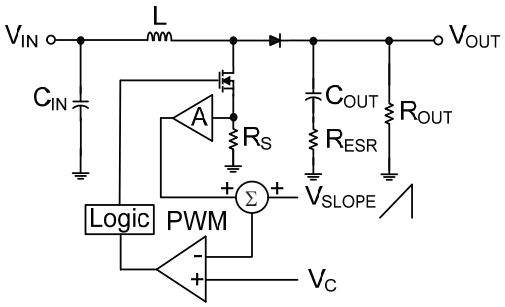


Figure 18. *In this example of a current-mode boost power stage, the inductor current is sampled in the metal-oxide semiconductor field-effect transistor (MOSFET) source resistor.*

Equations 28 and 29 give the duty-cycle relationship for the current-mode boost in CCM:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (28)$$

$$D' = \frac{V_{IN}}{V_{OUT}} \quad (29)$$

Equation 30 shows the transfer function for the current-mode boost power stage. As you can see, it contains two poles, one zero, one right-half-plane zero and an associated gain.

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)} \quad (30)$$

Equation 31 expresses the gain as:

$$A_{VC} \approx \frac{R_{OUT} \cdot D'}{2 \cdot R_i} \quad (31)$$

where $R_i = A \cdot R_S$ and $D' = 1 - D$.

Equation 32 calculates the first pole, which is related to the output capacitance and the load resistance. The effect of boosting moves the pole out by a factor of two [9].

$$\omega_P \approx \frac{2}{C_{OUT} \cdot R_{OUT}} \quad (32)$$

Equation 33 calculates the second pole, which is related to the inductance. The modulator voltage gain, K_m, is equal to V_{OUT}/V_{SLOPE} at D = 0.5 and will have little variation with operating conditions when properly scaling V_{SLOPE}.

$$\omega_L = \frac{K_m \cdot R_i}{L}$$

where $K_m \approx \frac{V_{OUT}}{V_{SLOPE}}$ at D = 0.5. (33)

Equation 34 gives the right-half-plane zero, which is related to the inductance and output resistance, while Equation 35 is related to the output capacitance ESR:

$$\omega_R = \frac{R_{OUT} \cdot D'^2}{L} \quad (34)$$

$$\omega_Z = \frac{1}{R_{ESR} \cdot C_{OUT}} \quad (35)$$

For the peak current-mode boost, Equation 36 calculates the optimal value of slope compensation:

$$V_{SLOPE} = \frac{(V_{OUT} - V_{IN}) \cdot R_i \cdot T}{L} \quad (36)$$

where R_i is the current-sense gain times the sense resistor, and *T* is equal to the switching period, $1/f_{SW}$.

Figure 19 shows the Bode plot of the current-mode boost power stage.

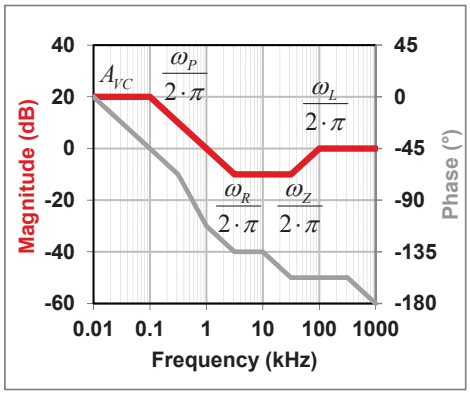


Figure 19. *The current-mode boost power stage has a right-half-plane zero at ω_R in the transfer function.*

Current-mode buck-boost

Like the current-mode boost, the current-mode buck-boost also exhibits a right-half-plane zero in the transfer function. It has the same energy storage characteristic during the switch on-time, with energy delivered to the output during the off-time. Again, this tends to limit the overall loop bandwidth due to the associated phase lag of the right-half-plane zero.

Figure 20 shows the schematic of the current-mode buck-boost power stage. For the buck-boost, the convention used here is to define either V_{IN} or V_{OUT} with its sign on the schematic. This is shown in **Figure 20** as $-V_{OUT}$. All equations use the absolute value of V_{IN} and V_{OUT}, regardless of sign.

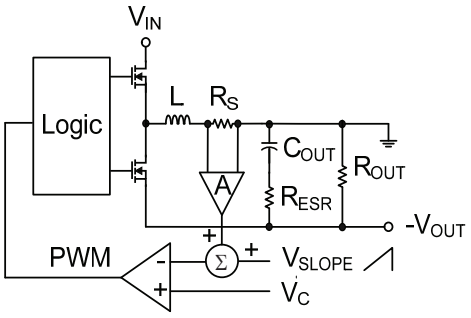


Figure 20. *This positive-to-negative current-mode buck-boost power stage is a level-shifted version of the standard buck converter.*

Equations 37 and 38 give the duty-cycle relationship for the current-mode buck-boost in CCM:

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}} \quad (37)$$

$$D' = \frac{V_{IN}}{V_{IN} + V_{OUT}} \quad (38)$$

Equation 39 shows the transfer function for the current-mode buck-boost power stage. As you can see, it contains two poles, one zero, one right-half-plane zero and an associated gain.

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)} \quad (39)$$

Equation 40 expresses the gain as:

$$A_{VC} \approx \frac{R_{OUT} \cdot D'}{(1+D) \cdot R_i} \quad (40)$$

where $R_i = A \cdot R_S$ and $D' = 1 - D$.

Equation 41 calculates the first pole, which is related to the output capacitance and the load resistance:

$$\omega_P \approx \frac{1+D}{C_{OUT} \cdot R_{OUT}} \quad (41)$$

Equation 42 calculates the second pole, which is related to the inductance. The modulator voltage gain, K_m, is equal to $(V_{IN}+V_{OUT})/V_{SLOPE}$ at D = 0.5 and will have little variation with operating conditions when properly scaling V_{SLOPE}.

$$\omega_L = \frac{K_m \cdot R_i}{L} \quad (42)$$

where $K_m \approx \frac{V_{IN} + V_{OUT}}{V_{SLOPE}}$ at D = 0.5.

Equation 43 gives the right-half-plane zero, which is related to the inductance and output resistance, while Equation 44 is related to the output capacitance ESR:

$$\omega_R = \frac{R_{OUT} \cdot D'^2}{L \cdot D} \quad (43)$$

$$\omega_Z = \frac{1}{R_{ESR} \cdot C_{OUT}} \quad (44)$$

For the peak current-mode buck-boost, Equation 45 calculates the optimal value of slope compensation:

$$V_{SLOPE} = \frac{V_{OUT} \cdot R_i \cdot T}{L} \quad (45)$$

where R_i is the current-sense gain times the sense resistor, and *T* is equal to the switching period, $1/f_{SW}$.

Figure 21 shows the Bode plot of the current-mode buck-boost power stage.

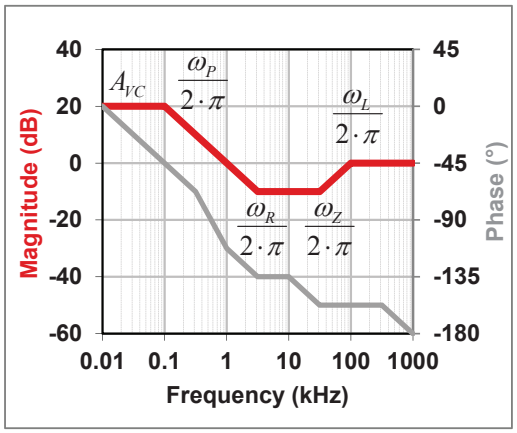


Figure 21. Like the current-mode boost, the current-mode buck-boost power stage also has a right-half-plane zero at ω_R in the transfer function.

Current-mode forward and other buck-derived topologies

The current-mode forward is similar to the current-mode buck, since energy transfers to the output during the primary switch on-time. Adjusting the transformer turns ratio provides the nominal output voltage within a practical duty-cycle range.

Figure 22 shows the schematic of the current-mode forward power stage.

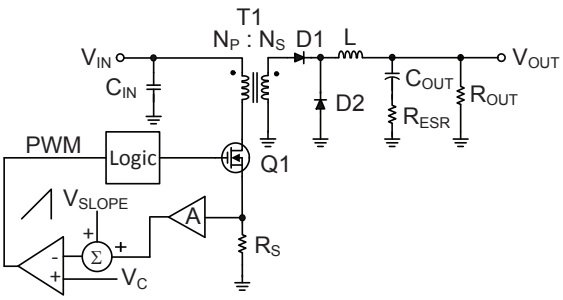


Figure 22. *A single-switch current-mode forward power stage has a buck-type output at the secondary. The inductor current is reflected into the primary and sampled in series with the switch.*

Equations 46 and 47 give the duty-cycle relationship for the current-mode forward in CCM:

$$D = \frac{V_{OUT}}{V_{IN}} \cdot \frac{N_P}{N_S} \tag{46}$$

$$D' = \frac{V_{IN} - V_{OUT} \cdot \frac{N_P}{N_S}}{V_{IN}} \tag{47}$$

Equation 48 shows the transfer function for the current-mode forward power stage. As you can see, it contains two poles, one zero and an associated gain.

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)} \tag{48}$$

Equation 49 expresses the gain as:

$$A_{VC} \approx \frac{R_{OUT}}{R_i} \cdot \frac{N_P}{N_S} \tag{49}$$

where $R_i = A \cdot R_S$.

Equation 50 calculates the first pole, which is related to the output capacitance and the load resistance:

$$\omega_P \approx \frac{1}{C_{OUT} \cdot R_{OUT}} \tag{50}$$

Equation 51 calculates the second pole, which is related to the inductance. The modulator voltage gain, K_m, is equal to V_{IN}/V_{SLOPE} at D = 0.5 and will have little variation with operating conditions when properly scaling V_{SLOPE}.

$$\omega_L = \frac{K_m \cdot R_i}{L} \cdot \left(\frac{N_S}{N_P}\right)^2 \tag{51}$$

where $K_m \approx \frac{V_{IN}}{V_{SLOPE}}$ at D = 0.5.

Equation 52 gives the zero, which is related to the output capacitance ESR:

$$\omega_Z = \frac{1}{R_{ESR} \cdot C_{OUT}} \tag{52}$$

For the peak current-mode forward, Equation 53 calculates the optimal value of slope compensation:

$$V_{SLOPE} = \frac{V_{OUT} \cdot R_i \cdot T}{L} \cdot \frac{N_S}{N_P} \tag{53}$$

where R_i is the current-sense gain times the sense resistor, and *T* is equal to the switching period, $1/f_{SW}$.

Figure 23 shows the Bode plot of the current-mode forward power stage.

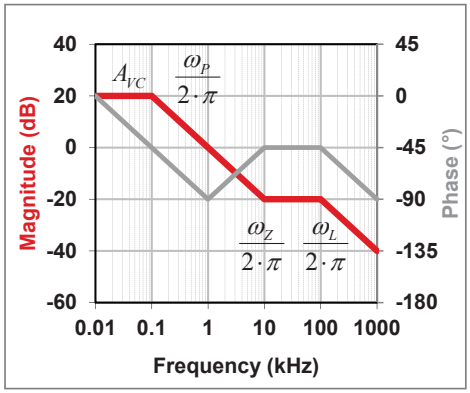


Figure 23. *The current-mode forward power-stage frequency response is similar to that of the buck.*

Current-mode flyback

The current-mode flyback has a right-half-plane zero in the transfer function. The magnetizing inductance stores energy during the switch on-time, with energy delivered to the output during the off-time. This tends to limit the overall loop bandwidth due to the associated phase lag of the right-half-plane zero.

Figure 24 shows the schematic of the current-mode flyback power stage.

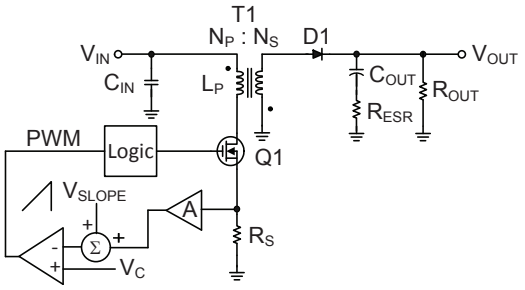


Figure 24. *For the current-mode flyback power stage, the isolation transformer also serves as the energy-storage inductor.*

Equations 54 and 55 give the duty-cycle relationship for the current-mode flyback in CCM:

$$D = \frac{V_{OUT}}{V_{IN} \cdot \frac{N_S}{N_P} + V_{OUT}} \tag{54}$$

$$D' = \frac{V_{IN}}{V_{IN} + V_{OUT} \cdot \frac{N_P}{N_S}} \tag{55}$$

Equation 56 shows the transfer function for the current-mode flyback power stage. As you can see, it contains two poles, one zero, one right-half-plane zero and an associated gain.

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)} \tag{56}$$

Equation 57 expresses the gain as:

$$A_{VC} \approx \frac{R_{OUT} \cdot D'}{(1+D) \cdot R_i} \cdot \frac{N_P}{N_S} \tag{57}$$

where $R_i = A \cdot R_S$ and $D' = 1 - D$.

Equation 58 calculates the first pole, which is related to the output capacitance and the load resistance:

$$\omega_P \approx \frac{1+D}{C_{OUT} \cdot R_{OUT}} \tag{58}$$

Equation 59 calculates the second pole, which is related to the inductance. The modulator voltage gain, K_m, is equal to $(V_{IN}+V_{OUT} \cdot N_P/N_S)/V_{SLOPE}$ at D = 0.5 and will have little variation with operating conditions when properly scaling V_{SLOPE}.

$$\omega_L = \frac{K_m \cdot R_i}{L_P} \tag{59}$$

where $K_m \approx \frac{V_{IN} + V_{OUT} \cdot \frac{N_P}{N_S}}{V_{SLOPE}}$ at D = 0.5.

Equation 60 gives the right-half-plane zero, which is related to the inductance and output resistance, while Equation 61 is related to the output capacitance ESR:

$$\omega_R = \frac{R_{OUT} \cdot D'^2}{L_P \cdot D} \cdot \left(\frac{N_P}{N_S}\right)^2 \tag{60}$$

$$\omega_Z = \frac{1}{R_{ESR} \cdot C_{OUT}} \tag{61}$$

For the peak current-mode flyback, Equation 62 calculates the optimal value of slope compensation:

$$V_{SLOPE} = \frac{V_{OUT} \cdot R_i \cdot T}{L_P} \cdot \frac{N_P}{N_S} \tag{62}$$

where R_i is the current-sense gain times the sense resistor, and *T* is equal to the switching period, $1/f_{SW}$.

Figure 25 shows the Bode plot of the current-mode flyback power stage.

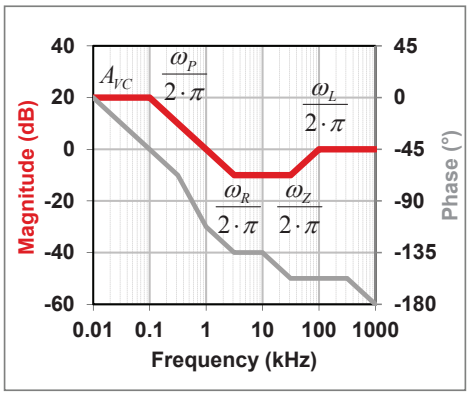


Figure 25. *The current-mode flyback power-stage frequency response is similar to that of the buck-boost.*

Type I error amplifier

Figure 26 shows a Type I error amplifier configuration, which is the simplest form of compensation; it is characterized by a single pole. You can analyze this circuit by recognizing that the error amplifier is inverting and has a virtual short between V_{FB} and V_{REF}. The feedback impedance divided by the input impedance gives you the small signal gain. Since V_{REF} can be viewed as an AC ground, you can ignore the value of R_{FBB}, as it does not affect the AC transfer function.

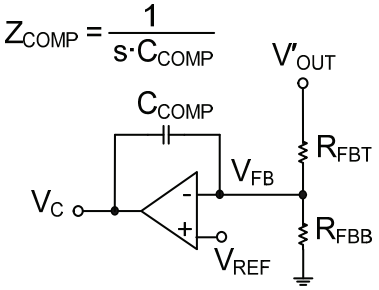


Figure 26. *Type I error amplifier compensation has a single capacitor in the feedback.*

Equation 63 is written by summing the currents at the error-amplifier inputs:

$$\frac{\hat{v}'_{OUT}}{R_{FBT}} + \frac{\hat{v}_C}{Z_{COMP}} = \hat{v}_{FB}\cdot\left(\frac{1}{R_{FBT}} + \frac{1}{Z_{COMP}}\right) \quad (63)$$

Equation 64 relates the feedback voltage to the control voltage by the open loop gain of the amplifier:

$$\hat{v}_{FB} = \frac{-\hat{v}_C}{A_{OL}} \quad (64)$$

Equation 65 combines Equations 63 and 64:

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} = -\frac{Z_{COMP}}{R_{FBT}}\cdot\left(\frac{1}{1+\frac{1}{A_{OL}}\cdot\left(1+\frac{Z_{COMP}}{R_{FBT}}\right)}\right) \quad (65)$$

Equation 66 shows that if the gain of the error amplifier is large enough

$$A_{OL}\cdot\left(\frac{R_{FBT}}{R_{FBT}+Z_{COMP}}\right) >> 1 \quad (66)$$

Then the closed-loop gain can be expressed by Equation 67 as:

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -\frac{Z_{COMP}}{R_{FBT}} = -\frac{1}{s\cdot C_{COMP}\cdot R_{FBT}} = -\frac{\omega_{EA}}{s} \quad (67)$$

Equation 68 defines the error amplifier pole frequency:

$$\omega_{EA} = \frac{1}{R_{FBT}\cdot C_{COMP}} \quad (68)$$

Examining the result reveals a single pole at the origin. In practice, this is limited at DC by the open-loop gain of the amplifier and is called dominant-pole compensation.

Figure 27 shows the straight-line approximation of the frequency response for an error amplifier with Type I compensation. Type I compensation is often

used for a constant-current type of current-mode buck, driving a light-emitting diode (LED) load with no output capacitor. While you can use this type of dominant-pole compensation for any power supply, for many systems this type of compensation does not offer the flexibility necessary to achieve optimal performance.

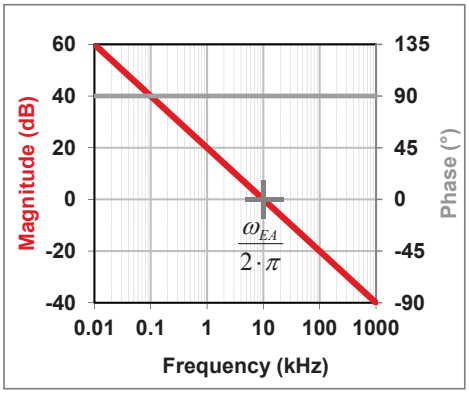


Figure 27. *A Type I error-amplifier frequency response is characterized by a single pole.*

Type II error amplifier

Figure 28 shows the schematic of a Type II error amplifier.

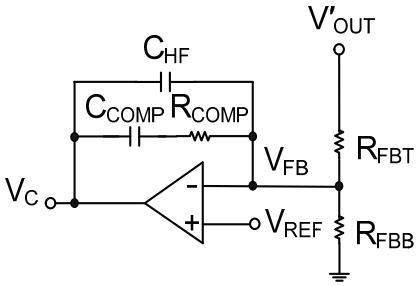


Figure 28. *Type II error-amplifier compensation adds a resistor and high-frequency capacitor to the feedback.*

Using the same derivation process as for Type I compensation, Equation 69 expresses the voltage-gain transfer function as:

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM}\cdot\frac{1+\frac{\omega_{ZEA}}{s}}{1+\frac{s}{\omega_{HF}}} \approx -\frac{A_{VM}\cdot\omega_{ZEA}}{s}\cdot\frac{1+\frac{s}{\omega_{ZEA}}}{1+\frac{s}{\omega_{HF}}} \quad (69)$$

where A_{VM} is defined as the mid-band voltage gain. Examining the result reveals that in Equation 70 the mid-band voltage gain is:

$$A_{VM} \approx \frac{R_{COMP}}{R_{FBT}} \quad (70)$$

Equation 71 reveals a zero at:

$$\omega_{ZEA} = \frac{1}{R_{COMP}\cdot C_{COMP}} \quad (71)$$

While Equation 72 reveals a high-frequency pole at:

$$\omega_{HF} \approx \frac{1}{R_{COMP}\cdot C_{HF}} \quad (72)$$

assuming $C_{COMP} >> C_{HF}$.

In practice, the open-loop gain of the amplifier will limit the error-amplifier gain at DC. Type II compensation is generally well suited for use with current-mode control. In selective cases, you can use it for voltage-mode control with a high value of ESR in the output capacitor.

Figure 29 shows the straight-line approximation of the frequency response for an error amplifier with Type II compensation.

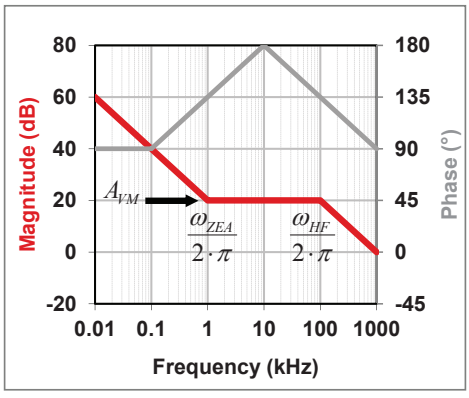


Figure 29. *A Type II compensator frequency response has a mid-band gain between the zero and pole.*

Type II transconductance amplifier

The difference between a conventional error amplifier and a transconductance amplifier is that with a transconductance amplifier, the input resistor divider network and the transconductance (g_m) parameter are now a part of the gain transfer function. Recalling the section on Type I error amplifiers, the bottom resistor of the input divider dropped out of the transfer function due to the virtual ground effect. Both pins were at the same potential and the AC contribution of the lower resistor was nonexistent. In a transconductance amplifier, there is no local feedback; therefore there is no virtual ground. You can no longer ignore the bottom resistor of the input divider, and g_m can vary depending on the integrated circuit design. A transconductance amplifier is also well suited for Type II compensation.

Figure 30 shows the schematic of a Type II transconductance error amplifier.

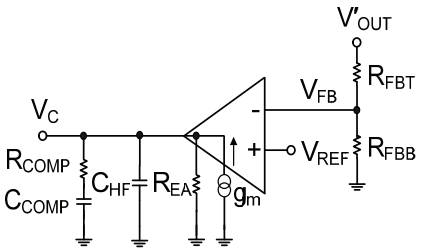


Figure 30. *Type II transconductance amplifier compensation components are referenced to ground at the output.*

The voltage-gain transfer function for a Type II transconductance amplifier is the same as for a regular error amplifier, as you would expect. Equation 73 is identical to Equation 69:

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{1+\frac{\omega_{ZEA}}{s}}{1+\frac{s}{\omega_{HF}}} \approx -\frac{A_{VM} \cdot \omega_{ZEA}}{s} \cdot \frac{1+\frac{s}{\omega_{ZEA}}}{1+\frac{s}{\omega_{HF}}} \quad (73)$$

The difference is in the mid-band voltage gain, given by Equation 74:

$$A_{VM} = K_{FB} \cdot g_m \cdot R_{COMP} \quad (74)$$

where $K_{FB} = \frac{R_{FBB}}{R_{FBB} + R_{FBT}}$.

As you can see from Equation 73, a Type II error amplifier has a pole at the origin, a zero and a second high-frequency pole. Equations 75 and 76 are identical to Equations 71 and 72:

$$\omega_{ZEA} = \frac{1}{R_{COMP} \cdot C_{COMP}} \quad (75)$$

$$\omega_{HF} \approx \frac{1}{R_{COMP} \cdot C_{HF}} \quad (76)$$

assuming $C_{COMP} >> C_{HF}$ and $R_{EA} >> R_{COMP}$.

The transconductance and output resistance of the amplifier set the open-loop gain, which will limit the error-amplifier gain at DC. Equation 77 expresses the open-loop gain as:

$$A_{OL} = g_m \cdot R_{EA} \quad (77)$$

You can use the transconductance amplifier for current-mode control. We do not recommend its use for Type III operation with voltage-mode control because of the feedback divider limitation on phase boost for low-voltage outputs.

Figure 31 shows the straight-line approximation of the frequency response for a transconductance error amplifier with Type II compensation.

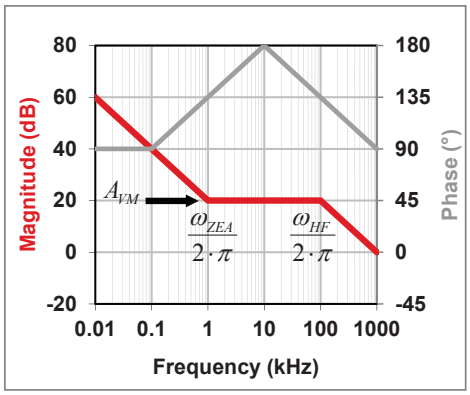


Figure 31. *A transconductance error amplifier with Type II compensation has a frequency response equivalent to a standard operational amplifier.*

Type III error amplifier

Type III compensation is generally the most useful technique for compensating voltage-mode-control converters, but it requires two additional components not present in Type II compensation, shown in **Figure 32**.

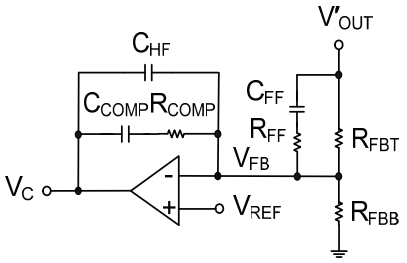


Figure 32. *Type III error-amplifier compensation adds a lead network across the top divider resistor.*

This compensation network provides a pole at the origin, two zeros and two higher-frequency poles in the feedback path. The two zeros offset the complex conjugate pole of the voltage-mode buck. Type III compensation can increase both the bandwidth and phase margin of a closed-loop system.

Equation 78 expresses the voltage-gain transfer function for Type III compensation as:

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} = -A_{VM}\cdot\frac{\left(1+\frac{\omega_{ZEA}}{s}\right)\cdot\left(1+\frac{s}{\omega_{FZ}}\right)}{\left(1+\frac{s}{\omega_{FP}}\right)\cdot\left(1+\frac{s}{\omega_{HF}}\right)} = -\frac{A_{VM}\cdot\omega_{ZEA}}{s}\cdot\frac{\left(1+\frac{s}{\omega_{ZEA}}\right)\cdot\left(1+\frac{s}{\omega_{FZ}}\right)}{\left(1+\frac{s}{\omega_{FP}}\right)\cdot\left(1+\frac{s}{\omega_{HF}}\right)} \quad (78)$$

The mid-band gain is the same as it is for a Type II error amplifier. Equation 79 is identical to Equation 70:

$$A_{VM} \approx \frac{R_{COMP}}{R_{FBT}} \quad (79)$$

Examining the Type III transfer function reveals two zeros: one zero set by R_{COMP} and C_{COMP} (Equation 80) and another zero set by R_{FBT} and C_{FF} (see Equation 81) to help offset the complex conjugate poles:

$$\omega_{ZEA} = \frac{1}{R_{COMP}\cdot C_{COMP}} \quad (80)$$

$$\omega_{FZ} \approx \frac{1}{R_{FBT}\cdot C_{FF}} \quad (81)$$

R_{FF} and C_{FF} along with R_{COMP} and C_{HF} determine the poles in the system, usually occurring after the output filter's complex conjugate pole. The examples will reveal more on the exact placement of these poles and zeros. See Equations 82 and 83:

$$\omega_{FP} = \frac{1}{R_{FF}\cdot C_{FF}} \quad (82)$$

$$\omega_{HF} \approx \frac{1}{R_{COMP}\cdot C_{HF}} \quad (83)$$

assuming $C_{COMP} >> C_{HF}$ and $R_{FBT} >> R_{FF}$.

Type III compensation is useful in power supplies where the output capacitor ESR is very low, such as in converters with ceramic output capacitors.

The reason for this is that low-ESR capacitors push the ESR zero higher in frequency than high-ESR capacitors. Thus, your converter will not benefit from the phase boost at lower frequencies, but Type III compensation can make up for that.

Figure 33 shows the straight-line approximation of the frequency response for an error amplifier with Type III compensation.

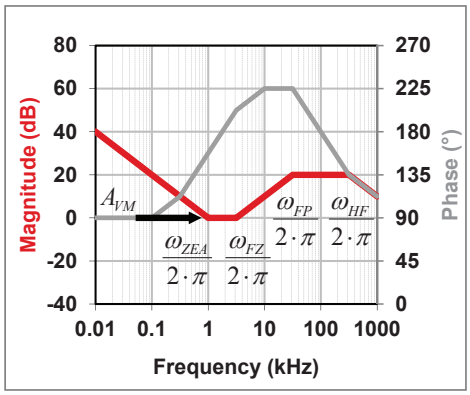


Figure 33. *A Type III compensator frequency response boosts the gain and phase in the mid band.*

Isolated feedback with optocoupler

Figure 34 shows Type II compensation using an optocoupler and the TL431 shunt regulator. The current-transfer ratio and resistors set the mid-band gain through the optocoupler. Bias currents and the diode forward voltage can limit the dynamic range. The reference voltage for a standard TL431 is 2.5 V, which can work for 5-V outputs and higher. For lower output voltages, the TLV431 has a 1.24-V reference.

In **Figure 34**, C_P includes the parasitic capacitance of the optocoupler's output transistor. Parasitic capacitance is often the limiting factor of the bandwidth in this configuration. The associated phase shift can go to –180 degrees, making compensation at higher frequencies challenging.

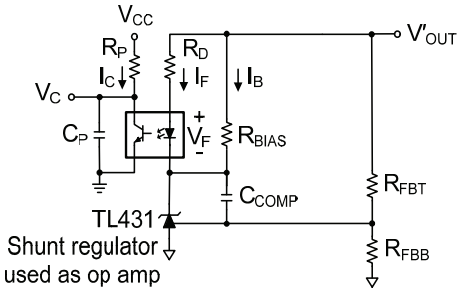


Figure 34. *This isolated feedback with an optocoupler uses a shunt regulator for secondary-side voltage control.*

Adding R_{BIAS} maintains a minimum current through the TL431 for regulation. It is not part of the frequency compensation network. Equation 84 expresses the voltage-gain transfer function as:

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM}\cdot\frac{1+\frac{\omega_{ZEA}}{s}}{1+\frac{s}{\omega_{HF}}} \approx -\frac{A_{VM}\cdot\omega_{ZEA}}{s}\cdot\frac{1+\frac{s}{\omega_{ZEA}}}{1+\frac{s}{\omega_{HF}}} \quad (84)$$

In Equation 85 the mid-band voltage gain is:

$$A_{VM} = CTR\cdot\frac{R_P}{R_D} \quad (85)$$

Equation 86 defines the current transfer ratio:

$$CTR = \frac{I_C}{I_F} \quad (86)$$

As you can see from Equation 84, this isolated feedback with an optocoupler is configured as a Type II error amplifier, which has a pole at the origin, a zero and a second high-frequency pole. See Equations 87 and 88:

$$\omega_{ZEA} = \frac{1}{R_{FBT}\cdot C_{COMP}} \quad (87)$$

$$\omega_{HF} = \frac{1}{R_P\cdot C_P} \quad (88)$$

Figure 35 shows the frequency-response plot.

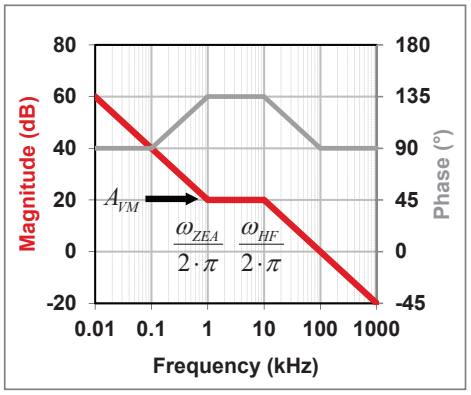


Figure 35. *The frequency response of this optocoupler feedback has a Type II characteristic.*

Voltage-mode buck example

Figure 36 is the complete voltage-mode buck regulator model, showing the modulator, output filter and error amplifier. For Type III compensation, use a standard voltage-type operational amplifier.

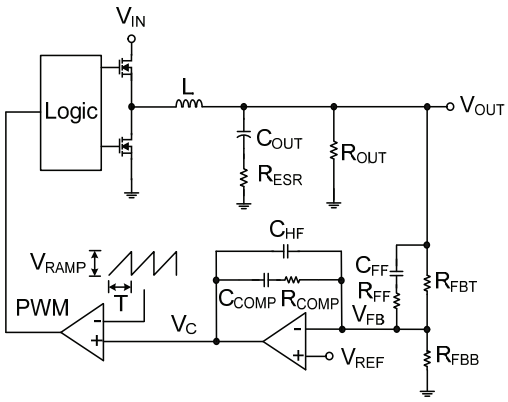


Figure 36. *The complete voltage-mode buck converter with power stage and error amplifier. The fixed ramp shown could be proportional, depending upon the controller.*

Voltage-mode buck compensation strategy

We will now outline the compensation guidelines for a voltage-mode buck with Type III compensation. This is an approximate method. Choose a large value for R_{FBT}; typical values for R_{FBT} are between 2 kΩ and 200 kΩ. A_{VM}, the mid-band voltage gain, is one of the design parameters; by changing this parameter, you can change the performance of the system. The value of A_{VM} that gives you the desired performance will vary with modulator gain.

For voltage-mode control, set the system bandwidth typically at 10 percent of the switching frequency. The two zeros, ω_{ZEA} and ω_{FZ}, should cancel the output filter's complex conjugate pole. Set the pole frequency, ω_{FP}, to cancel the output-filter zero caused by the output capacitor ESR. Set the high-frequency pole, ω_{HF}, equal to half the switching frequency. For higher bandwidth, set ω_{HF} equal to the switching frequency.

Once you have selected A_{VM} and calculated the pole/zero location, you can solve for the compensation component values using the equations below. We recommend that you verify the system crossover frequency and phase margin on the bench to confirm your desired performance.

Use the following simplified design method for the voltage-mode buck:

- Choose a value for R_{FBT} based on the bias current and power dissipation.
- Pick a target bandwidth; typically, $f_{SW}/10$: $\omega_C = 2 \cdot \pi \cdot f_C$.
- Find A_{VM} to achieve the target bandwidth.
- Set ω_{ZEA} and ω_{FZ} equal to the output-filter complex conjugate pole ω_0: $\omega_{ZEA} = \omega_{FZ} = \omega_0$.
- Set ω_{FP} equal to the output-filter zero, ω_Z: $\omega_{FP} = \omega_Z$.
- Set ω_{HF} equal to half the switching frequency: $\omega_{HF} = 2 \cdot \pi \cdot f_{SW}/2$.

Solve Equations 89 through 93 to find the component values:

$$A_{VM} = \frac{\omega_C}{A_{VC} \cdot \omega_O} \tag{89}$$

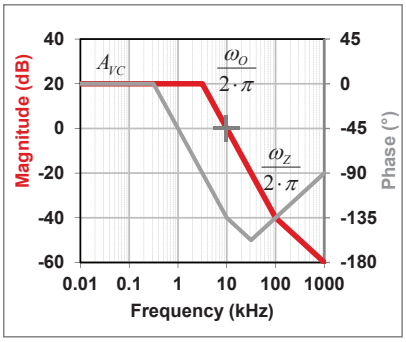
$$R_{COMP} = A_{VM} \cdot R_{FBT} \tag{90}$$

$$C_{FF} = \frac{1}{\omega_{FZ} \cdot R_{FBT}} \tag{91}$$

$$C_{COMP} = \frac{1}{\omega_{ZEA} \cdot R_{COMP}} \tag{92}$$

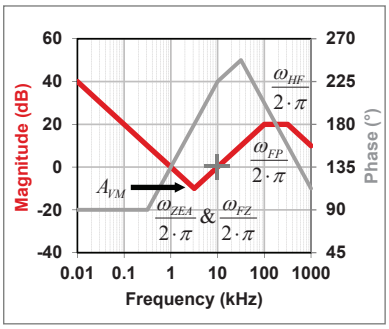
$$C_{HF} = \frac{1}{\omega_{HF} \cdot R_{COMP}} \tag{93}$$

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1+\frac{s}{\omega_Z}}{1+\frac{s}{Q_O \cdot \omega_O}+\frac{s^2}{\omega_O{}^2}}$$



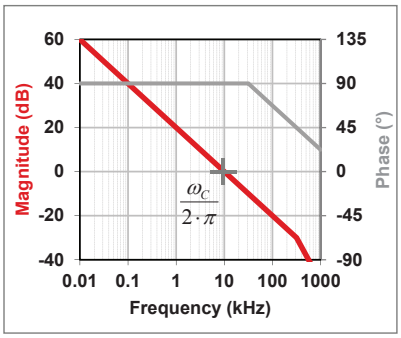
Power stage (a)

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{\left(1+\frac{\omega_{ZEA}}{s}\right)\cdot\left(1+\frac{s}{\omega_{FZ}}\right)}{\left(1+\frac{s}{\omega_{FP}}\right)\cdot\left(1+\frac{s}{\omega_{HF}}\right)}$$



Error amplifier (b)

$$\frac{\hat{v}_{OUT}}{\hat{v}'_{OUT}} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}'_{OUT}}$$



Control loop (c)

Figure 37. *The power-stage (a) and error-amplifier (b) plots sum to produce the control-loop plot (c) for the voltage-mode buck frequency response.*

Voltage-mode buck compensation results

Figure 37 shows the voltage-mode buck idealized straight-line plots of the power stage, error amplifier and control loop. The overall control loop is the product of the power-stage and error-amplifier transfer functions. On the Bode plots, the overall loop gain is the sum in decibels of the power-stage gain and error-amplifier gain. Adjust the mid-band gain of the error amplifier to meet the target loop bandwidth.

Current-mode buck example

Figure 38 is the complete current-mode buck regulator model, showing the modulator, output filter and error amplifier. For Type II compensation, this example uses a transconductance amplifier.

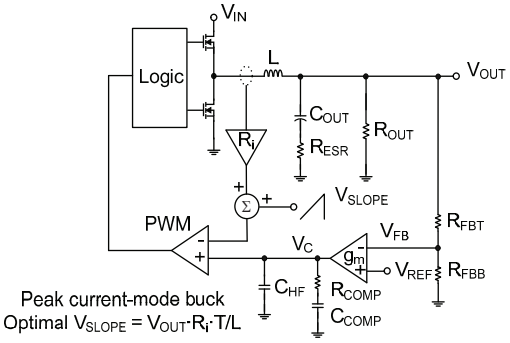


Figure 38. *This current-mode buck shows idealized current sensing in series with the inductor.*

Current-mode buck compensation strategy

We will now outline the compensation guidelines for a current-mode buck with Type II compensation. At frequencies after the output-filter pole, the modulator transconductance and output-filter capacitor set the power-stage gain.

You can adjust the mid-band voltage gain, A_{VM}, to achieve the target loop bandwidth, typically one-tenth the switching frequency.

To give the maximum amount of phase boost, place the error-amplifier zero, ω_{ZEA}, a decade below the target crossover frequency. An alternate strategy

is to place the error-amplifier zero at the load pole of ω_O, which will give you an equivalent result. The high-frequency pole, ω_{HF}, should cancel the ESR zero of the output capacitor. For capacitors with very low ESR, set the pole to 10 times the crossover frequency. If the error amplifier has a relatively low unity-gain bandwidth, C_{HF} may not be required.

For an ideal current-mode buck, the upper limit for the loop bandwidth is $f_{SW}/5$. For nonideal parameters – such as a relatively high amount of slope compensation – you may need to lower the loop bandwidth to less than $f_{SW}/20$. A Type III feedback network could compensate for this, but is not effective with a transconductance amplifier.

Use the following simplified design method for the current-mode buck:

- Choose a value for R_{FBT} based on the bias current and power dissipation.
- Find the modulator transconductance in A/V.
- Pick a target bandwidth; typically, $f_{SW}/10$: $\omega_C = 2 \cdot \pi \cdot f_C$.
- Find A_{VM} to achieve the target bandwidth.
- Set ω_{ZEA} equal to one-tenth the target crossover frequency: $\omega_{ZEA} = \omega_C/10$.
- Set ω_{HF} equal to the ESR zero frequency: $\omega_{HF} = \omega_Z$.

Solve Equations 94 through 99 to find the component values:

$$G_m(\text{mod}) = \frac{1}{R_i} \quad (94)$$

$$A_{VM} = \frac{\omega_C \cdot C_{OUT}}{G_m(\text{mod})} \quad (95)$$

$$R_{COMP} = A_{VM} \cdot R_{FBT} \ \ (op\ amp) \quad (96)$$

$$R_{COMP} = \frac{A_{VM}}{g_m \cdot K_{FB}} \ \ (g_m\ amp) \quad (97)$$

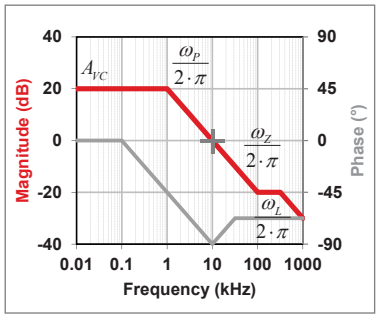
$$C_{COMP} = \frac{1}{\omega_{ZEA} \cdot R_{COMP}} \quad (98)$$

$$C_{HF} = \frac{1}{\omega_{HF} \cdot R_{COMP}} \quad (99)$$

Current-mode buck compensation results

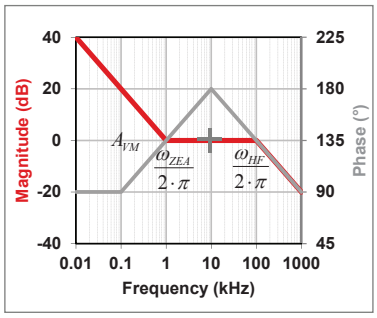
Figure 39 shows the current-mode buck idealized straight-line plots of the power stage, error amplifier and control loop.

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1+\frac{s}{\omega_Z}}{\left(1+\frac{s}{\omega_P}\right)\cdot\left(1+\frac{s}{\omega_L}\right)}$$



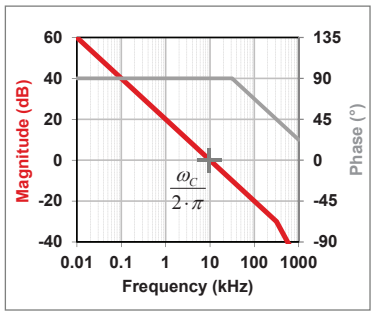
Power stage (a)

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{1+\frac{\omega_{ZEA}}{s}}{1+\frac{s}{\omega_{HF}}}$$



Error amplifier (b)

$$\frac{\hat{v}_{OUT}}{\hat{v}'_{OUT}} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}'_{OUT}}$$



Control loop (c)

Figure 39. *The power-stage (a) and error-amplifier (b) plots sum to produce the control-loop plot (c) for the current-mode buck frequency response.*

Current-mode boost example

Figure 40 is the complete current-mode boost regulator model, showing the modulator, output filter and error amplifier. For Type II compensation, this example uses a transconductance amplifier.

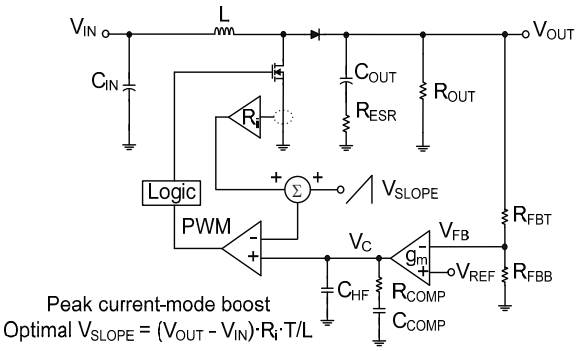


Figure 40. *This current-mode boost senses the current in series with the switch.*

Current-mode boost compensation strategy

We will now outline the compensation guidelines for a current-mode boost with Type II compensation. At frequencies after the output-filter pole, the modulator transconductance and output-filter capacitor set the power-stage gain. The overall loop bandwidth is typically limited to one-fourth the right-half-plane zero frequency. You can adjust A_{VM} to achieve the target loop bandwidth. To give the maximum amount of phase boost, place the error-amplifier zero, ω_{ZEA}, a decade below the target crossover frequency. The high-frequency pole, ω_{HF}, should cancel the lower of the right-half-plane or ESR zero frequency.

Some sets of operating conditions and parameter values may require additional phase margin. In such cases, the crossover frequency may be limited to one-fifth or one-sixth the right-half-plane zero frequency.

Use the following simplified design method for the current-mode boost:

- Choose a value for R_{FBT} based on the bias current and power dissipation.
- Find the modulator transconductance in A/V.
- Find the right-half-plane zero frequency at the minimum input voltage and maximum load current.
- Set the target bandwidth to one-fourth the right-half-plane zero frequency: $\omega_C = 2 \cdot \pi \cdot f_C = \omega_R/4$.
- Find A_{VM} to achieve the target bandwidth.
- Set ω_{ZEA} equal to one-tenth the target crossover frequency: $\omega_{ZEA} = \omega_C/10$.
- Set ω_{HF} equal to the lower of the right-half-plane or ESR zero frequency: $\omega_{HF} = \omega_R$ or ω_Z.

Solve Equations 100 through 106 to find the component values:

$$G_m(\text{mod}) = \frac{D'}{R_i} \tag{100}$$

$$\omega_R = \frac{R_{OUT} \cdot D'^2}{L} \tag{101}$$

$$A_{VM} = \frac{\omega_C \cdot C_{OUT}}{G_m(\text{mod})} \tag{102}$$

$$R_{COMP} = A_{VM} \cdot R_{FBT} \ \ (op\ amp) \tag{103}$$

$$R_{COMP} = \frac{A_{VM}}{g_m \cdot K_{FB}} \ \ (g_m\ amp) \tag{104}$$

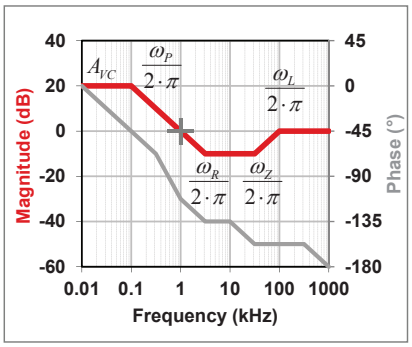
$$C_{COMP} = \frac{1}{\omega_{ZEA} \cdot R_{COMP}} \tag{105}$$

$$C_{HF} = \frac{1}{\omega_{HF} \cdot R_{COMP}} \tag{106}$$

Current-mode boost compensation results

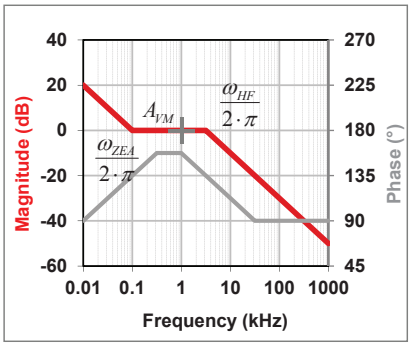
Figure 41 shows the current-mode boost idealized straight-line plots of the power stage, error amplifier and control loop.

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{\left(1-\frac{s}{\omega_R}\right)\cdot\left(1+\frac{s}{\omega_Z}\right)}{\left(1+\frac{s}{\omega_P}\right)\cdot\left(1+\frac{s}{\omega_L}\right)}$$



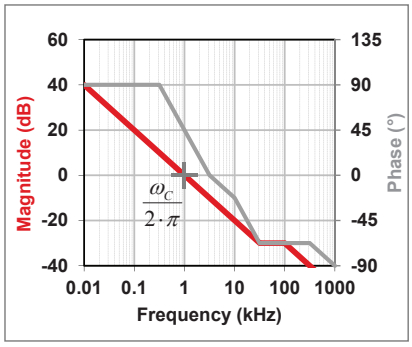
Power stage (a)

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{1+\frac{\omega_{ZEA}}{s}}{1+\frac{s}{\omega_{HF}}}$$



Error amplifier (b)

$$\frac{\hat{v}_{OUT}}{\hat{v}'_{OUT}} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}'_{OUT}}$$



Control loop (c)

Figure 41. *The power-stage (a) and error-amplifier (b) plots sum to produce the control-loop plot (c) for the current-mode boost frequency response.*

Current-mode buck-boost example

Figure 42 is the complete current-mode buck-boost regulator model, showing the modulator, output filter and error amplifier. For Type II compensation, this example uses a transconductance amplifier.

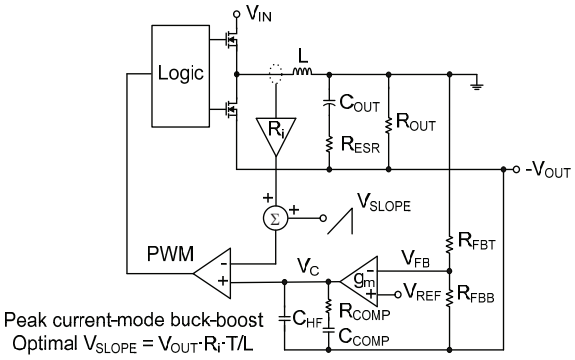


Figure 42. *The error amplifier is referenced to -V_{OUT} for this current-mode buck-boost.*

Current-mode buck-boost compensation strategy

We will now outline the compensation guidelines for the current-mode buck-boost with Type II compensation. At frequencies after the output-filter pole, the modulator transconductance and output-filter capacitor set the power-stage gain.

The overall loop bandwidth is typically limited to one-fourth the right-half-plane zero frequency. Adjust A_{VM} to achieve the target loop bandwidth.

To give the maximum amount of phase boost, place the error-amplifier zero, ω_{ZEA}, a decade below the target crossover frequency. The high-frequency pole, ω_{HF}, should cancel the lower of the right-half-plane or ESR zero frequency.

Some sets of operating conditions and parameter values may require additional phase margin.

In such cases, the crossover frequency may be limited to one-fifth or one-sixth the right-half-plane zero frequency.

Use the following simplified design method for the current-mode buck-boost:

- Choose a value for R_{FBT} based on the bias current and power dissipation.
- Find the modulator transconductance in A/V.
- Find the right-half-plane zero frequency at the minimum input voltage and maximum load current.
- Set the target bandwidth to one-fourth the right-half-plane zero frequency: $\omega_C = 2 \cdot \pi \cdot f_C = \omega_R/4$.
- Find A_{VM} to achieve the target bandwidth.
- Set ω_{ZEA} equal to one-tenth the target crossover frequency: $\omega_{ZEA} = \omega_C/10$.
- Set ω_{HF} equal to the lower of the right-half-plane or ESR zero frequency: $\omega_{HF} = \omega_R$ or ω_Z.

Solve Equations 107 through 113 to find the component values:

$$G_m(\text{mod}) = \frac{D'}{R_i} \quad (107)$$

$$\omega_R = \frac{R_{OUT} \cdot D'^2}{L \cdot D} \quad (108)$$

$$A_{VM} = \frac{\omega_C \cdot C_{OUT}}{G_m(\text{mod})} \quad (109)$$

$$R_{COMP} = A_{VM} \cdot R_{FBT} \ \ (op\ amp) \quad (110)$$

$$R_{COMP} = \frac{A_{VM}}{g_m \cdot K_{FB}} \ \ (g_m\ amp) \quad (111)$$

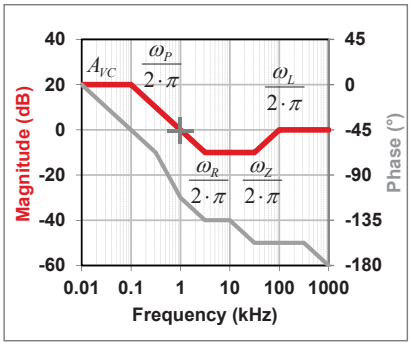
$$C_{COMP} = \frac{1}{\omega_{ZEA} \cdot R_{COMP}} \quad (112)$$

$$C_{HF} = \frac{1}{\omega_{HF} \cdot R_{COMP}} \quad (113)$$

Current-mode buck-boost compensation results

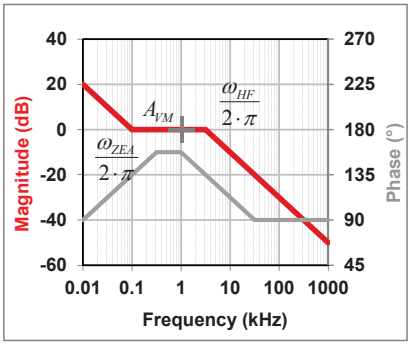
Figure 43 shows the current-mode buck-boost idealized straight-line plots of the power stage, error amplifier and control loop.

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)}$$



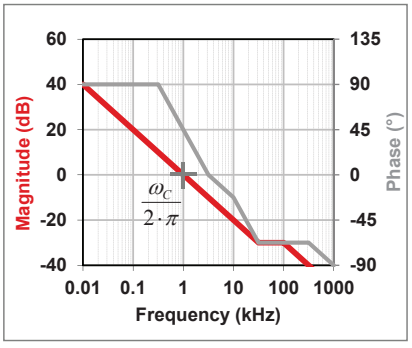
Power stage (a)

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{1 + \frac{\omega_{ZEA}}{s}}{1 + \frac{s}{\omega_{HF}}}$$



Error amplifier (b)

$$\frac{\hat{v}_{OUT}}{\hat{v}'_{OUT}} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}'_{OUT}}$$



Control loop (c)

Figure 43. *The power-stage (a) and error-amplifier (b) plots sum to produce the control-loop plot (c) for the current-mode buck-boost frequency response.*

Isolated current-mode forward example

Figure 44 is the complete isolated current-mode forward converter model, showing the modulator, output filter and error amplifier. For Type II compensation, this example uses a TL431 shunt regulator and optocoupler.

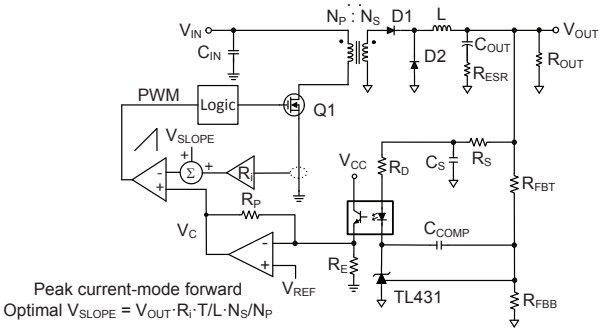


Figure 44. *This isolated current-mode forward converter uses the primary-side error amplifier as part of the feedback.*

Current-mode forward compensation strategy

We will now outline the compensation guidelines for a current-mode forward with Type II compensation. At frequencies after the output-filter pole, the modulator transconductance and output-filter capacitor set the power-stage gain. Adjust A_{VM} to achieve the target loop bandwidth, typically one-tenth the switching frequency. The selection of R_D and R_P for DC bias considerations may limit A_{VM}. In such cases, you may need to increase C_{OUT} to meet the desired crossover frequency. To give the maximum amount of phase boost, place the error-amplifier zero, ω_{ZEA}, a decade below the target crossover frequency. The high-frequency pole,ω_{HF}, should cancel the ESR zero of the output capacitor.

For capacitors with very low ESR, you can set the pole to 10 times the crossover frequency. This example uses a high-bandwidth configuration for the optocoupler feedback, which incorporates the primary-side amplifier. In this configuration, the optocoupler emitter is at a virtual ground of V_{REF}. This minimizes the pole due to the optocoupler's parasitic capacitance, since the collector-to-emitter voltage does not change.

For an ideal current-mode forward, the upper limit for the loop bandwidth is $f_{SW}/5$. For nonideal parameters such as a relatively high amount of slope compensation, you may need to lower the loop bandwidth to less than $f_{SW}/20$.

Use the following simplified design method for the current-mode forward:

- Choose a value for R_{FBT} based on the bias current and power dissipation.
- Find the modulator transconductance in A/V.
- Pick the target bandwidth; typically, $f_{SW}/10$: $\omega_C = 2 \cdot \pi \cdot f_C$.
- Find A_{VM} to achieve the target bandwidth.
- Adjust R_D, R_P and C_{OUT} as required.
- Set ω_{ZEA} equal to one-tenth the target crossover frequency: $\omega_{ZEA} = \omega_C/10$.
- Set ω_{HF} equal to the ESR zero frequency: $\omega_{HF} = \omega_Z$.

Solve Equations 114 through 118 to find the component values:

$$G_m(\text{mod}) = \frac{1}{R_i} \cdot \frac{N_P}{N_S} \quad (114)$$

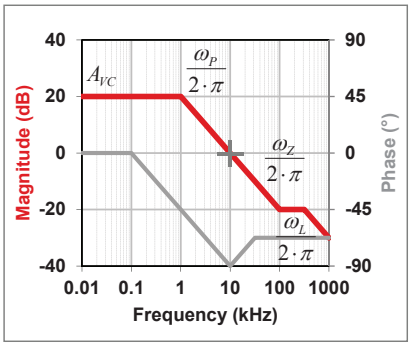
$$A_{VM} = \frac{\omega_C \cdot C_{OUT}}{G_m(\text{mod})} \quad (115)$$

$$R_D = CTR \cdot \frac{R_P}{A_{VM}} \quad (116)$$

$$C_{COMP} = \frac{1}{R_{FBT} \cdot \omega_{ZEA}} \quad (117)$$

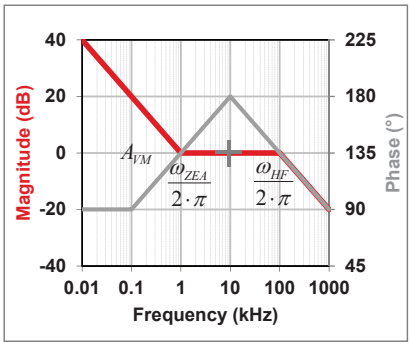
$$C_S = \frac{1}{R_S \cdot \omega_{HF}} \quad (118)$$

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1+\frac{s}{\omega_Z}}{\left(1+\frac{s}{\omega_P}\right)\cdot\left(1+\frac{s}{\omega_L}\right)}$$



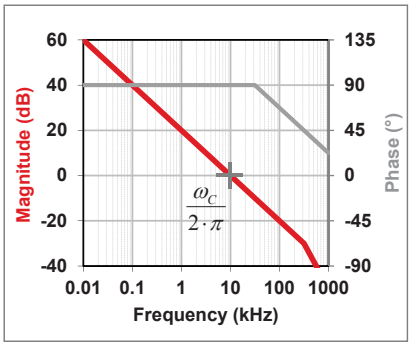
Power stage (a)

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{1+\frac{\omega_{ZEA}}{s}}{1+\frac{s}{\omega_{HF}}}$$



Error amplifier (b)

$$\frac{\hat{v}_{OUT}}{\hat{v}'_{OUT}} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}'_{OUT}}$$



Control loop (c)

Figure 45. *The power-stage (a) and error-amplifier (b) plots sum to produce the control-loop plot (c) for the current-mode forward frequency response.*

Current-mode forward compensation results

Figure 45 shows the current-mode forward idealized straight-line plots of the power stage, error amplifier and control loop.

Isolated current-mode flyback example

Figure 46 is the complete current-mode flyback regulator model showing the modulator, output filter and error amplifier. For Type II compensation, this example uses a TL431 shunt regulator and optocoupler.

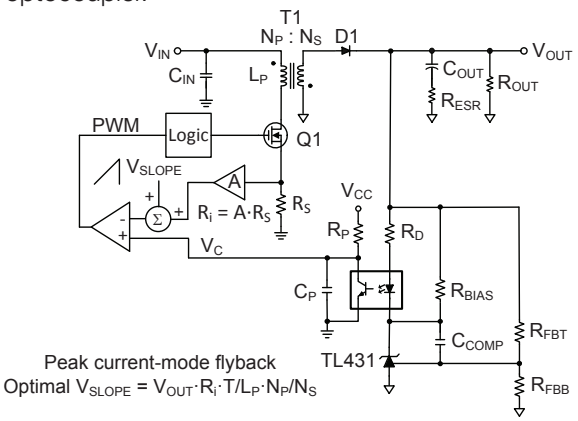


Figure 46. *The optocoupler feedback for this isolated current-mode flyback is implemented with a minimum of components.*

Current-mode flyback compensation strategy

We will now outline the compensation guidelines for the current-mode flyback with Type II compensation. At frequencies after the output-filter pole, the modulator transconductance and output-filter capacitor set the power-stage gain. The overall loop bandwidth is typically limited to one-fourth the right-half-plane zero frequency. Adjust A_{VM} to achieve the target loop bandwidth. The selection of R_D and R_P for DC bias considerations may limit A_{VM}. In such cases, you may need to increase C_{OUT} to meet the desired crossover frequency. To give the maximum amount of phase boost, place the error-amplifier zero, ω_{ZEA}, a decade below the target crossover frequency. The high-frequency pole, ω_{HF}, should cancel the lower of the right-half-plane or ESR zero frequency.

Some sets of operating conditions and parameter values may require additional phase margin. In such cases, the crossover frequency may be limited to one-fifth or one-sixth the right-half-plane zero frequency.

Use the following simplified design method for the current-mode flyback:

- Choose a value for R_{FBT} based on the bias current and power dissipation.
- Find the modulator transconductance in A/V.
- Find the right-half-plane zero frequency at the minimum input voltage and maximum load current.
- Set the target bandwidth to one-fourth the right-half-plane zero frequency: $\omega_C = 2 \cdot \pi \cdot f_C = \omega_R/4$.
- Find A_{VM} to achieve the target bandwidth.
- Adjust R_D, R_P and C_{OUT} as required.
- Set ω_{ZEA} equal to one-tenth the target crossover frequency: $\omega_{ZEA} = \omega_C/10$.
- Set ω_{HF} equal to the lower of the right-half-plane or ESR zero frequency: $\omega_{HF} = \omega_R$ or ω_Z.

Solve Equations 119 through 124 to find the component values:

$$G_m(\text{mod}) = \frac{D'}{R_i} \cdot \frac{N_P}{N_S} \quad (119)$$

$$\omega_R = \frac{R_{OUT} \cdot D'^2}{L_P \cdot D} \cdot \left(\frac{N_P}{N_S}\right)^2 \quad (120)$$

$$A_{VM} = \frac{\omega_C \cdot C_{OUT}}{G_m(\text{mod})} \quad (121)$$

$$R_D = CTR \cdot \frac{R_P}{A_{VM}} \quad (122)$$

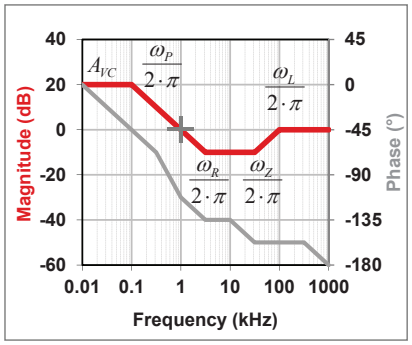
$$C_{COMP} = \frac{1}{R_{FBT} \cdot \omega_{ZEA}} \quad (123)$$

$$C_P = \frac{1}{R_P \cdot \omega_{HF}} \quad (124)$$

Current-mode flyback compensation results

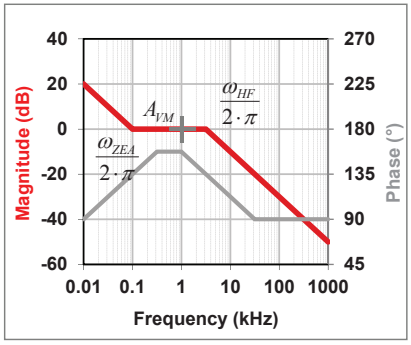
Figure 47 shows the current-mode flyback idealized straight-line plots of the power stage, error amplifier and control loop.

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)}$$



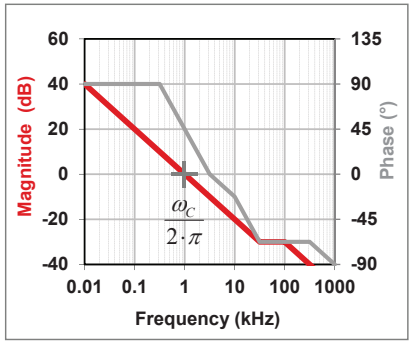
Power stage (a)

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{1 + \frac{\omega_{ZEA}}{s}}{1 + \frac{s}{\omega_{HF}}}$$



Error amplifier (b)

$$\frac{\hat{v}_{OUT}}{\hat{v}'_{OUT}} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}'_{OUT}}$$



Control loop (c)

Figure 47. The power-stage (a) and error-amplifier (b) plots sum to produce the control-loop plot (c) for the current-mode flyback frequency response.

Bandwidth versus transient response

Transient response is directly related to the bandwidth of the control loop. With no ESR, slew rate or duty-cycle limiting, the initial response time is one-fourth the effective control-loop period. This is the equivalent first quarter of a sinusoidal response at the unity-gain frequency. The peak voltage will vary based on the topology and damping, but is easily predictable with a surprising degree of accuracy.

It is important to verify the performance over all operating conditions. Duty-cycle limiting can cause a significant droop when operating the control loop outside its linear range. Reference [11] is an Applied Power Electronics Conference and Exhibition (APEC) paper on the topic, which includes design methods to meet transient response. **Figure 48** shows a typical frequency-response plot, while **Figure 49** shows the transient response.

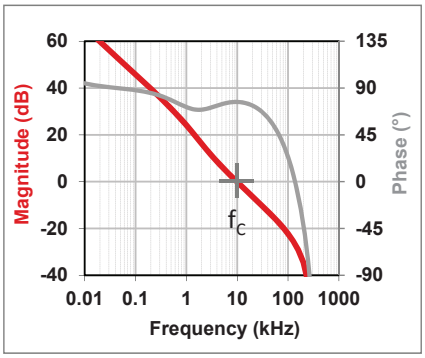


Figure 48. *The current-mode bandwidth is set at 10 kHz for this example.*

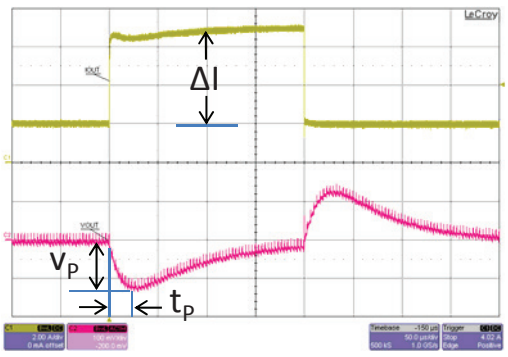


Figure 49. *The corresponding current-mode transient response shows t_P = 25 µs and V_P = 130 mV for a load step of ΔI = 5 A.*

With no ESR, slew rate or duty-cycle limiting, Equation 125 calculates t_P as:

$$t_P = \frac{1}{4 \cdot f_C}$$

$$t_P = \frac{1}{4 \cdot 10kHz} = 25\mu s \quad (125)$$

Current-mode single-pole approximation with Equation 126 calculates V_P as:

$$V_P = \frac{\Delta I}{2 \cdot \pi \cdot f_C \cdot C_{OUT}}$$

$$V_P = \frac{5A}{2 \cdot \pi \cdot 10kHz \cdot 440\mu F} = 180mV \quad (126)$$

Current-mode critically damped (as shown in **Figure 49**) with Equation 127 calculates V_P as:

$$V_P = \frac{\Delta I}{e \cdot \pi \cdot f_C \cdot C_{OUT}}$$

$$V_P = \frac{5A}{e \cdot \pi \cdot 10kHz \cdot 440\mu F} = 130mV \quad (127)$$

Voltage-mode control with Equation 128 calculates V_P as:

$$V_P = \frac{\Delta I}{8 \cdot f_C \cdot C_{OUT}}$$

$$V_P = \frac{5A}{8 \cdot 10kHz \cdot 440\mu F} = 140mV \quad (128)$$

Practical limitations of error amplifiers

The error-amplifier bandwidth can limit the maximum loop-crossover frequency. As you can see from Figure 50, where the closed-loop gain intersects the open-loop gain plot, the phase drops quickly. You will need a wider-bandwidth op amp for voltage mode due to Type III compensation.

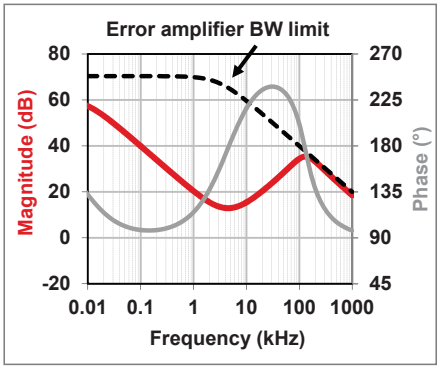


Figure 50: The error amplifier's open-loop gain and bandwidth set a hard limit for the closed-loop response.

Practical limitations of optocouplers

Resistance in series with the output transistor forms a pole in the kilohertz range. The pole is dependent on bias current and output resistance. As you can see in **Figure 51**, higher output resistance causes the pole to occur at a lower frequency. In a simplified analysis, we used a single pole with an external capacitor. With no external capacitor the roll-off approaches –40 dB/decade, with phase shift at higher frequencies of –180 degrees. This is more of an issue for forward- or other buck-derived topologies with higher crossover frequencies.

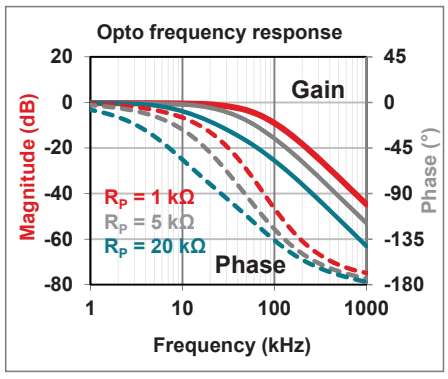


Figure 51. *The optocoupler pole moves toward lower frequencies at lower bias currents using higher resistor values.*

Practical limitations due to the switching frequency

The maximum crossover frequency is some fraction of the switching frequency. **Figure 52** shows the control-loop phase margin going quickly negative at the switching frequency. With a sufficient error-amplifier bandwidth, a voltage-mode converter can approach one-third the switching frequency and have adequate phase and gain margin. An ideal current-mode buck can achieve one-fifth the switching frequency with critical damping. Higher crossover frequency results in higher noise sensitivity and possible switching jitter. A general rule of thumb is one-fifth to one-tenth the switching frequency. The right-half-plane zero usually limits boost and buck-boost converters operating in CCM.

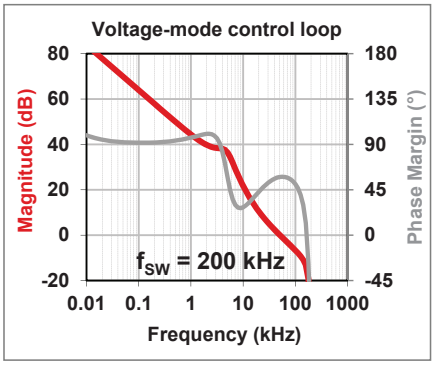


Figure 52. *The voltage-mode control loop shows the phase going to zero near the switching frequency. The available gain and phase margin set an upper limit on the control-loop bandwidth.*

Discontinuous versus continuous conduction-mode

DCM occurs when the inductor current dwells at zero before the end of the switching cycle. DCM is a normal condition for diode-rectified circuits when the load drops to a light level. DCM causes a reduction in bandwidth, which you can clearly see in **Figure 53** for the current-mode response. In general, if the control loop is stable in CCM, it will also be stable in DCM.

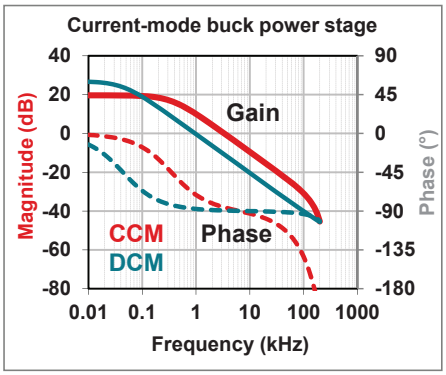


Figure 53. *The current-mode power-stage bandwidth is reduced in DCM.*

For the voltage-mode response shown in **Figure 54**, the order of the filter is reduced in DCM, since the inductor now acts as a current source.

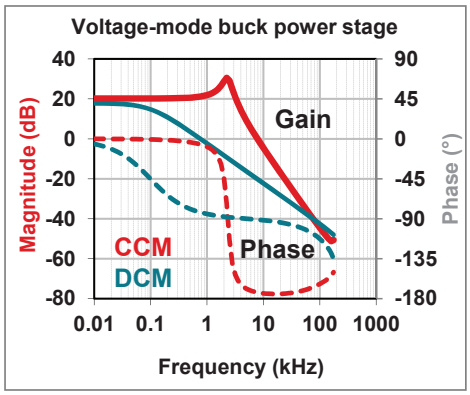


Figure 54. *The voltage-mode power-stage bandwidth is also reduced in DCM.*

DCM duty cycle

Equations 129 through 131 show the duty-cycle equations for DCM. To determine the mode boundary, you can set the CCM and DCM duty-cycle equations equal to each other.

$$\text{Buck: } D = \sqrt{\frac{2 \cdot L \cdot f_{SW} \cdot I_{OUT} \cdot V_{OUT}}{V_{IN} \cdot (V_{IN} - V_{OUT})}} \quad (129)$$

$$\text{Boost: } D = \frac{\sqrt{2 \cdot L \cdot f_{SW} \cdot I_{OUT} \cdot (V_{OUT} - V_{IN})}}{V_{IN}} \quad (130)$$

$$\text{Buck-boost: } D = \frac{\sqrt{2 \cdot L \cdot f_{SW} \cdot I_{OUT} \cdot V_{OUT}}}{V_{IN}} \quad (131)$$

Input-filter stability and second-stage filters

Input-filter stability

The line impedance and input capacitors form a resonant circuit when connecting the converter to a remote input power source through a wiring harness, as shown in Figure 55. Typical wiring inductance is on the order of 0.5 µH/m. An input inductor reduces reflected ripple current back to the source. In order to minimize overshoot, make $C_{IN} > 10 \cdot L_{IN}$.

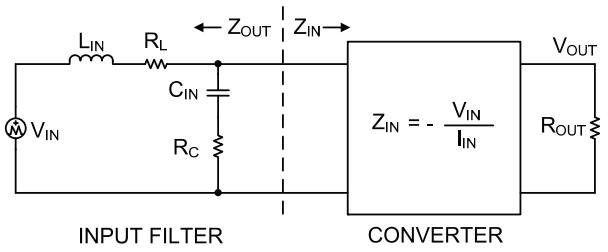


Figure 55. *The converter acts as a load on the input filter. For stability, filter Z_{OUT} << converter Z_{IN}.*

Equations 132 and 133 calculate the characteristic source impedance and resonant frequency, respectively:

$$Z_S = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (132)$$

$$f_S = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{IN} \cdot C_{IN}}} \quad (133)$$

The converter exhibits a negative input impedance, which is lowest at the minimum input voltage (Equation 134):

$$Z_{IN} = -\frac{V_{IN}}{I_{IN}} = -\frac{V_{IN}^2}{P_{OUT}} \quad (134)$$

Equation 135 gives the damping factor for the input filter as:

$$\zeta = \frac{1}{2} \cdot \left(\frac{R_L + R_C}{Z_S} + \frac{Z_S}{Z_{IN}} \right) \quad (135)$$

where R_L is the input wiring resistance and R_C is the series resistance of the input capacitors. The term Z_S/Z_{IN} will always be negative due to Z_{IN}.

When $\zeta = 1$, the input filter is critically damped, but this value may be difficult to achieve with practical component values. When $\zeta < 0.2$, the input filter will exhibit significant ringing. If ζ is zero or negative, there is not enough resistance in the circuit and the input filter will sustain an oscillation.

The general guidelines are:

- Converter input impedance – switching regulators exhibit a negative input impedance, which is lowest at the minimum input voltage.
- Filter output impedance – an underdamped LC filter exhibits a high output impedance at resonance.
- Relative impedance – for stability, the filter's output impedance must be much less than the converter's input impedance.

When operating near the minimum input voltage, you may need an aluminum electrolytic capacitor across C_{IN} to damp the input. You should evaluate any parallel capacitor for its root-mean-square (RMS) current rating. The current will split between the ceramic and aluminum capacitors based on the relative impedance at the switching frequency.

Second-stage filter

Figure 56 shows the power stage of a buck regulator followed by a second-stage filter. The first-stage capacitor is sized to handle the output RMS current, while the second-stage capacitor reduces the ripple voltage and provides energy storage for the load transient. This method is particularly useful for boost- or buck-boost-type outputs, which have high ripple voltage due to the pulsing rectifier current.

You must include the effect of the second-stage filter in the control-loop analysis. Account for the total output capacitance and use the capacitance to determine the loop bandwidth. A second-stage resonance at too low a frequency can cause the control loop to go unstable, even when taking feedback at the first-stage output.

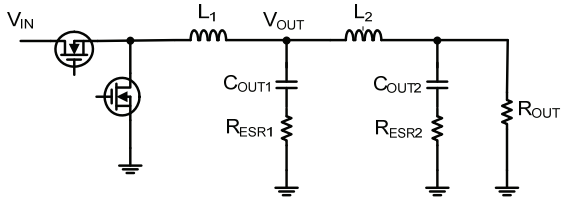


Figure 56. *A buck regulator with second-stage filter.*

The general guidelines are:

- Filter capacitors – make C_{OUT1} smaller than C_{OUT2}. C_{OUT1} is typically ceramic.
- Filter inductors – make L_2 smaller than L_1. Make sure that I_{SAT} is greater than I_{OUT} max.
- Filter resonance – make the second-stage filter resonance three times larger than the crossover frequency.
- Damping – damp the second-stage filter to a Q of 1.

Primary-side compensation considerations

Primary-side compensation

Figure 57 illustrates a method that uses the primary-side inverting amplifier to implement frequency compensation. Though not often used alone, it can complement secondary-side compensation. If the output-voltage accuracy is not critical, a series Zener and resistor can directly drive the optocoupler from the output voltage.

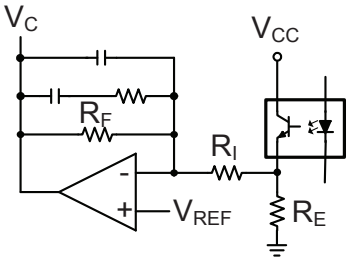


Figure 57. *Primary-side compensation can provide additional control of the frequency response.*

High-bandwidth configuration

Figure 58 shows a configuration where the optocoupler emitter is at a virtual ground of V_{REF}. This configuration minimizes the pole due to the optocoupler's parasitic capacitance, since the collector-to-emitter voltage does not change. This configuration is also particularly useful in forward converters to achieve high bandwidth; we used it in the section covering the isolated current-mode forward example.

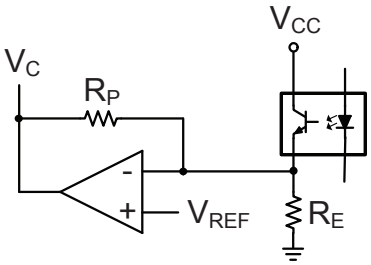


Figure 58. *The optocoupler emitter is biased at V_{REF} of the primary-side amplifier in the high-bandwidth configuration.*

Secondary-side compensation considerations

ESR zero compensation

Figure 59 shows how a resistor-capacitor (RC) pole to the optocoupler can cancel the ESR zero of the output capacitor, which is helpful when using aluminum electrolytic output capacitors with high ESR. We used this configuration in the section covering the isolated current-mode forward example.

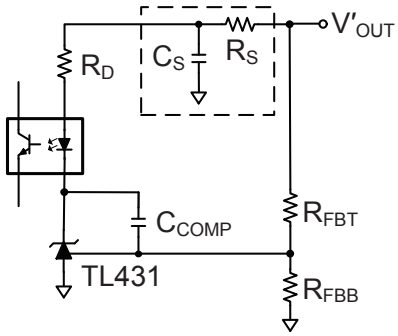


Figure 59. *A simple RC to the optocoupler allows for ESR zero compensation.*

Phase boost

Figure 60 shows how a feed-forward network across R_D adds phase boost for increased bandwidth. This method cancels the inherent pole of the optocoupler.

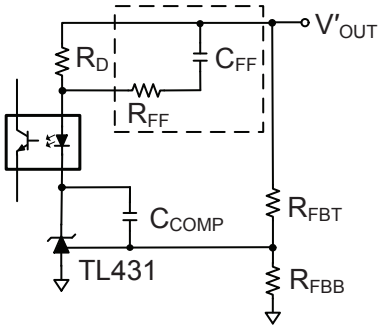


Figure 60. *Placing a lead network across the optocoupler's gain-setting resistor adds phase boost.*

Zener bias

Figure 61 shows how Zener bias for R_D eliminates the high-frequency feedback path for secondary-side compensation. This method is common for higher output voltages to prevent exceeding the TL431's voltage rating. R_S and Z_S can also bias the optocoupler from the rectified secondary voltage.

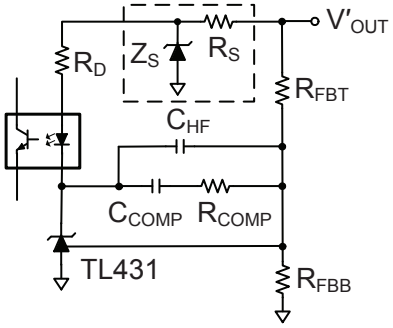


Figure 61. *A Zener biases the optocoupler with a fixed voltage.*

Real-world compensation example

Switching regulator with poor compensation

Figure 62 shows a basic current-mode buck regulator, which uses a transconductance amplifier. After building the circuit, it showed a fairly high crossover frequency with low phase margin.

DC bias of the output ceramic capacitors reduced the effective capacitance substantially. A switched resistive load exercised the loop at its maximum bandwidth. Bench measurements of the control loop agreed with the transient response shown in **Figure 63**, where low phase margin results in output-voltage ringing.

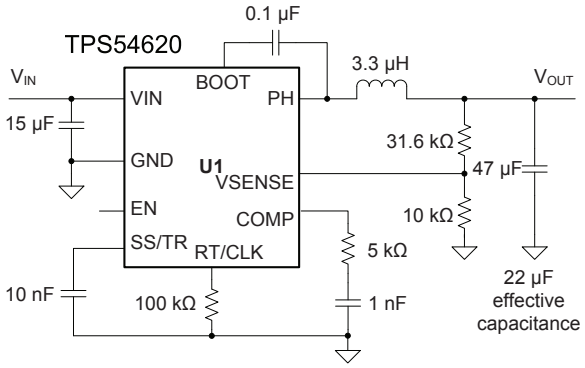


Figure 62. *A synchronous buck regulator exhibits poor transient performance.*

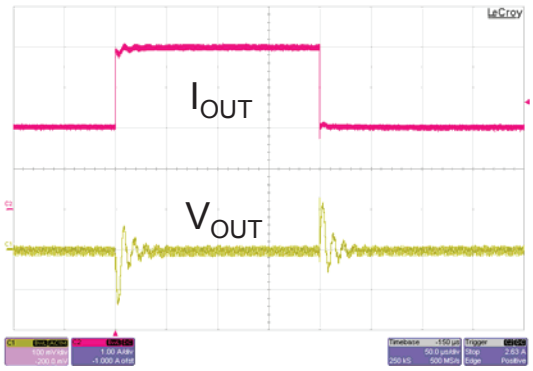
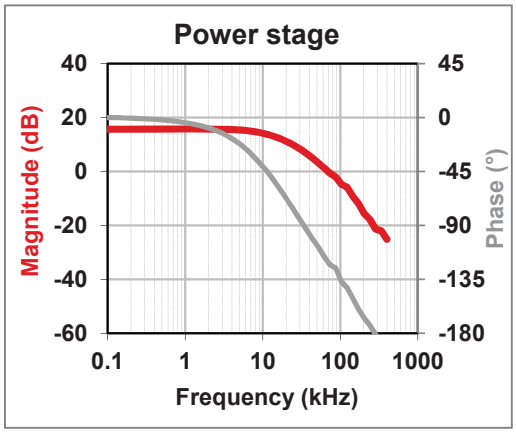
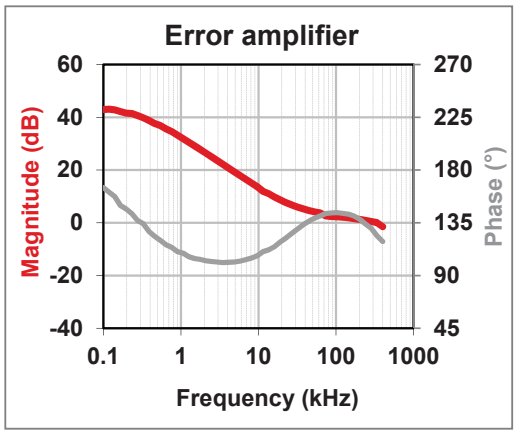


Figure 63. *An underdamped transient response indicates low phase margin.*

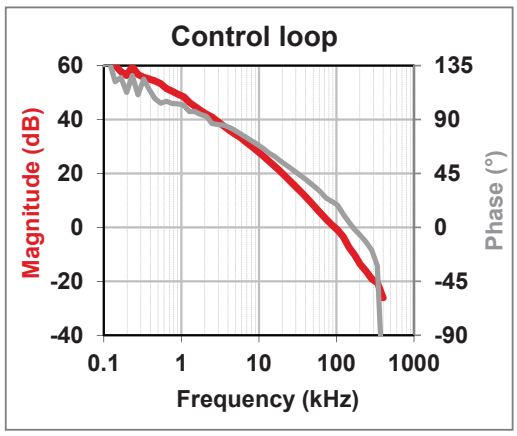
By observing the frequency response in **Figure 64**, you can analyze the performance. In **Figure 64a**, the phase is headed toward –180 degrees, indicating relatively high internal slope compensation. In **Figure 64b**, the error-amplifier zero appears to be a bit high and the mid-band gain is around 3 dB. In **Figure 64c**, the crossover frequency is 95 kHz, with only 20 degrees of phase margin.



(a)



(b)



(c)

Figure 64. *The power-stage (a) and error-amplifier (b) plots sum to produce the control-loop plot (c), showing high bandwidth and low phase margin.*

Switching regulator with revised compensation

Adjusting the compensation network of the error amplifier achieves well-damped performance. **Figure 65** shows the revised circuit, while **Figure 66** shows the improved transient response.

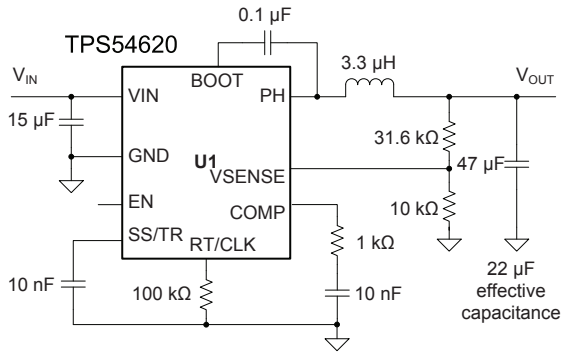


Figure 65. Adjusting only two compensation components improved the performance.

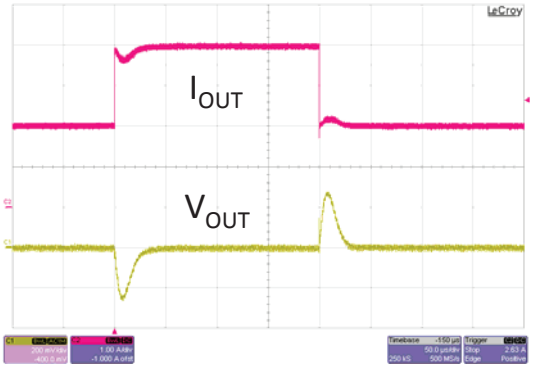
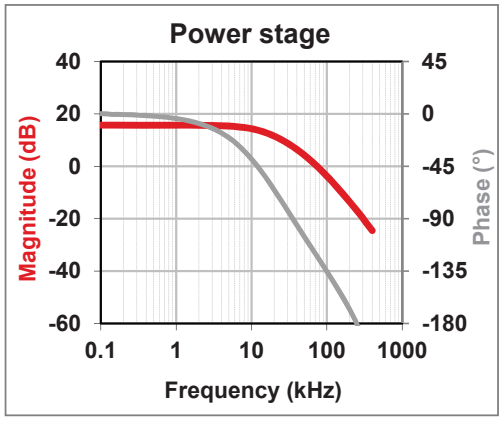
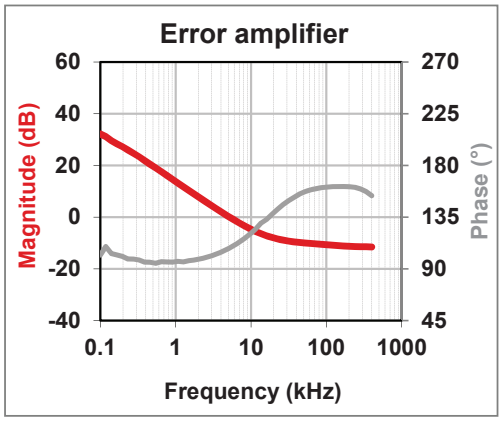


Figure 66. A critically damped transient response indicates good phase margin.

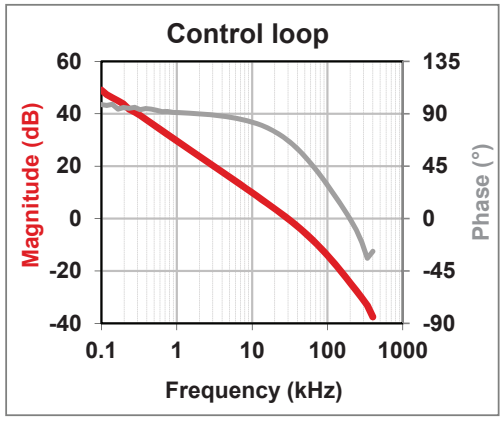
By observing the frequency response in **Figure 67**, you can analyze the performance. In **Figure 67a**, there is no external adjustment for slope compensation. All power-stage components are the same. In **Figure 67b**, decreasing R_{COMP} lowers the mid-band gain, which will lower the crossover frequency. Increasing C_{COMP} to move the error-amplifier zero to a lower frequency increases the phase margin at crossover. In **Figure 67c,** the crossover frequency is now 30 kHz, with 67 degrees of phase margin.



(a)



(b)



(c)

Figure 67. By leaving the power stage (a) as is and adjusting the error-amplifier (b) response, the control loop (c) exhibits acceptable gain and phase margin.

Summary

This paper covered CCM operation of voltage- and current-mode converters. Standard linear feedback amplifiers for nonisolated and isolated converters enable a wide range of compensation techniques. We hope that you can use the design examples of popular topologies we have given here.

To summarize the compensation design method simply:

- Identify the poles and zeros of the power stage.
- Cancel the power stage poles and zeros with zeros and poles in the error amplifier.
- Adjust the gain for best performance.

Additional information

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A021014

Printed in U.S.A. by (Printer, City, State)

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